Compal Confidential

Fortworth20 EDW10 Schematic Document

Intel Protability Processor with ATi RC300ML + IXP150

2004-03-16

REV: 0.2

Compal Electronics, Inc.		
Title: Cover Sheet		
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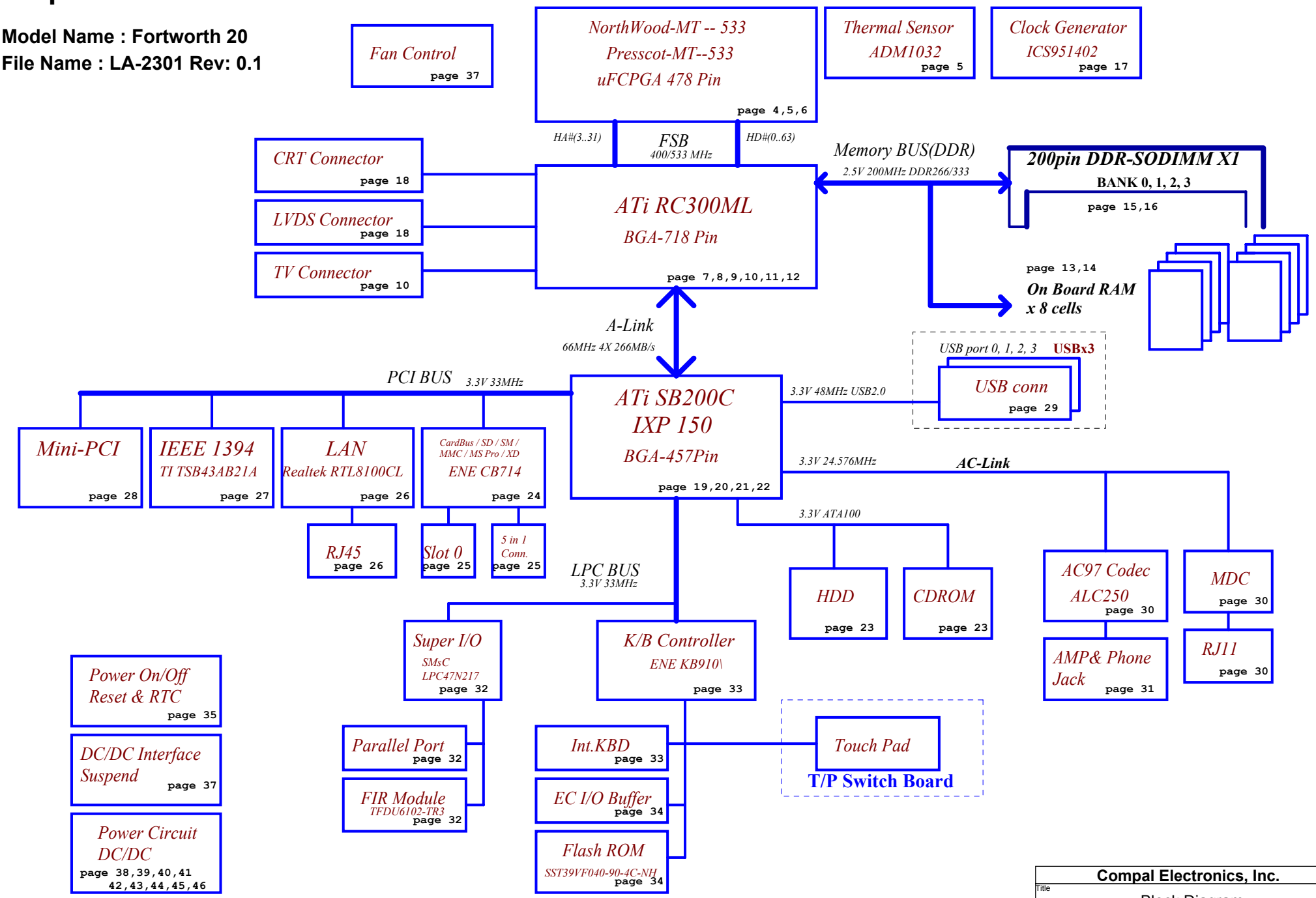
Model Name : Fortworth 20
File Name : LA-2301 Rev: 0.1

Block Diagram



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Title: Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V rail for Processor VID	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON*	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
5 in 1	AD20	2	B
Mini-PCI	AD18	3	C/D

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16)	1010 000X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b
ALC250	0000 000X b

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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Title: Notes

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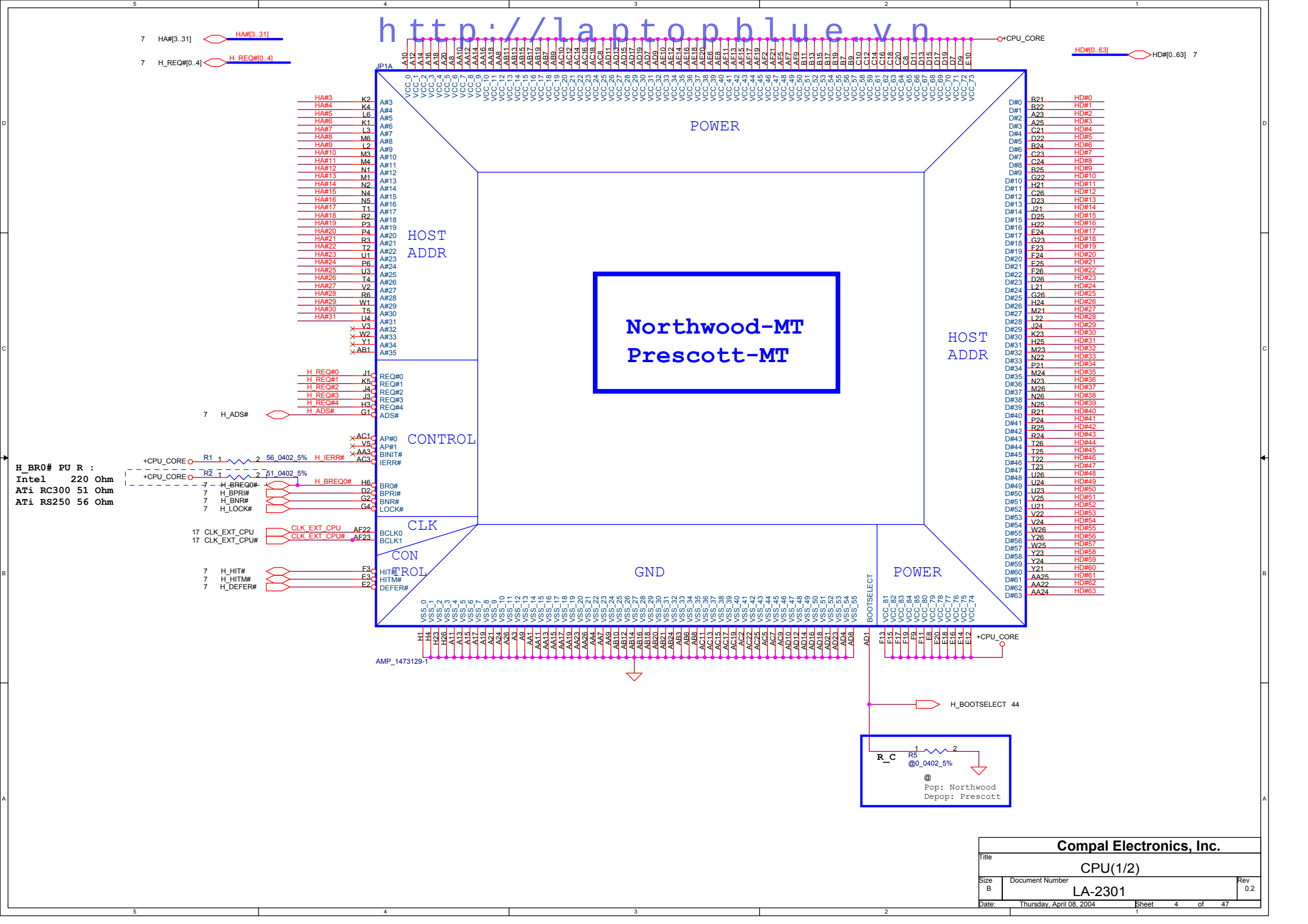

Compal Electronics, Inc.	
Title	CPU(1/2)
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Northwood-MT
Prescott-MT

GTL Reference Voltage

1. < 1.5" from the CPU Ball.
2. 220P cap. has to be closed to the ball as possible.
3. Intel: 0.63VCC.
   ATi: 0.66VCC.

+CPU_CORE
R12 51.1_0603_1% 15mil
+GTLVREF1
C2 220P_0402_50V7K
C3 1U_0603_10V6K
R16 86.6_0603_1%

Pop: Northwood Imp: 50 Ohm
Depop: Prescott Imp:60 Ohm
R_G R18 @0_0402_5%

+CPU_CORE
R19 56_0402_5%
R20 56_0402_5%
R21 56_0402_5%
R22 56_0402_5%
R23 56_0402_5%
R24 56_0402_5%
R25 56_0402_5%
R26 300_0402_5%
R27 56_0402_5%
CPU_GHI# 20

for mobile CPU

R34 51_0402_5%

Intel 852GME RDDP 56Ohm.
ATi RC300 51Ohm
ATi RS250 56 Ohm

+CPU_CORE
H_FERR# R11 56_0402_1%
H_PWRGD R13 300_0402_1%
H_THERMTRIP# R14 56_0402_1%
H_RESET# R15 51_0402_5%
C1 @10P_0402_50V8J@22_0402_5%
R17

H_INTR C4 180P_0402_50V8J
H_NMI C5 180P_0402_50V8J
H_CPUSLP# C6 180P_0402_50V8J
H_SMI# C7 180P_0402_50V8J
H_STPCLK# C8 180P_0402_50V8J
H_IGNNE# C9 180P_0402_50V8J
H_A20M# C10 180P_0402_50V8J
H_INIT# C11 180P_0402_50V8J

Place within 1.5" from CPU

GND
H_SKTOCC# R10 0_0402_5%

JP1B

CONTROL
H_RS#0 F1
H_RS#1 G5
H_RS#2 F4
H_TRDY# J6
RS#0
RS#1
RS#2
RSP#
TRDY#

LEGACY
H_A20M# C6
H_FERR# B6
H_IGNNE# B2
H_SMI# B5
H_PWRGD AB23
H_STPCLK# Y4
H_INTR D1
H_NMI E5
H_INIT# W5
H_RESET# AB25
A20M#
FERR#
IGNNE#
SMI#
PWRGOOD
STPCLK#
LINT0
LINT1
INIT#
RESET#

MISC
H_DBSY# H5
H_DRDY# H2
BSEL0 AD6
BSEL1 AD5
DBSY#
DRDY#
BSEL0
BSEL1

THERMAL
H_THERMDA B3
H_THERMDC C4
H_THERMTRIP# A2
THERMDA
THERMDC
THERMTRIP#

MISC
ITP_BPM#0 AC6
ITP_BPM#1 AB5
ITP_BPM#2 AC4
ITP_BPM#3 Y6
ITP_BPM#4 AA5
ITP_BPM#5 AB4
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5

RP1 1K_1206_8P4R_5%
ITP_TCK D4
ITP_TDI C1
ITP_TMS F7
ITP_TRST# E6

ITP
TCK
TDI
TDO
TMS
TRST#

MISC
VCCIOPLL
VCCA
VCCSENSE
VSSSENSE
VCCVIDLB
VSSA

+CPU_CORE
LQG21F4R7N00_0805 L1
LQG21F4R7N00_0805 L2
C12 33U_D2_8M_R35
+VCCIOPLL AD20
+VCCA AE23
VCCSENSE A5
VSSSENSE A4
+VCCVIDLB AE3
+CPU_VID R35 0_0603_5%
VSSA AD22
25mil

R25 ->
Pop: Prescott
Depop: Northwood

ITP CLK
ITP_CLK0 AC26
ITP_CLK1 AD26
COMP0 L24
COMP1 P1
R36 61.9_0603_1% COMP0
R37 61.9_0603_1% COMP1
width= 10mil

51.1 Ohm for Northwood,
61.9 Ohm for Prescott

GROUND

REF
OPTIMIZED/COMPAT#
DP#0 J26
DP#1 K25
DP#2 K26
DP#3 L25
GTLREF0 AA21
GTLREF1 AA6
GTLREF2 F20
GTLREF3 F6
AE26
+GTLVREF1

ITP
TESTHI0 AD24
TESTHI1 AA2
TESTHI2 AC21
TESTHI3 AC20
TESTHI4 AC24
TESTHI5 AC23
TESTHI6 AA20
TESTHI7 AB22
TESTHI8 U6
TESTHI9 W4
TESTHI10 Y3
TESTHI11 A6
TESTHI12 AD25
CPU_GHI#
H_DPSLPR#

DATA
DSTBN#0 E22
DSTBN#1 K22
DSTBN#2 R22
DSTBN#3 W22
DSTBP#0 F21
DSTBP#1 J23
DSTBP#2 P23
DSTBP#3 W23
H_DSTBN#0 7
H_DSTBN#1 7
H_DSTBN#2 7
H_DSTBN#3 7
H_DSTBP#0 7
H_DSTBP#1 7
H_DSTBP#2 7
H_DSTBP#3 7

ADDR
ADSTB#0 L5
ADSTB#1 R5
H_ADSTB#0 7
H_ADSTB#1 7

DATA
DBI#0 E21
DBI#1 G25
DBI#2 P26
DBI#3 V21
DBR# AE25
H_DBI#0 7
H_DBI#1 7
H_DBI#2 7
H_DBI#3 7
NC: W/O ITP

MISC
PROCHOT# C3
MCERR# V6
SLP# AB26
H_PROCHOT# 43
H_CPUSLP# 19
NC1 A22
NC2 A7
NC3 AE25
NC4 AF24
NC5 AF21

GROUND
MISC

AMP_1473129-1

+3VS
RP2 10K_1206_8P4R_5%
R40 10K_0402_5%
R41 10K_0402_5%
CPU_VID0 44
CPU_VID1 44
CPU_VID2 44
CPU_VID3 44
CPU_VID4 44
CPU_VID5 44

+CPU_VID
25mil
C13 0.1U_0402_10V6K
Pop: Prescott
Depop: Northwood
R38 680_0402_5%
H_VID_PWRGD 35

CPU Temperature Sensor

+3VS
R39 200_0402_5%
+3VS_THMSEN
C14 0.1U_0402_10V6K
R42 10K_0402_5%
C15 @2200P_0603_50V7K
10mil
10mil
H_THERMDA
H_THERMDC
U1
D+ VDD1
D- ALERT#
SCLK THERM#
SDATA GND
30,33 EC_SMC2
30,33 EC_SMD2
ADM1032ARM_RM8

+3VS
R86 4.7K_0402_5%
H_DPSLPR#
Q4 MMBT3904_SOT23
R93 4.7K_0402_5%
17,19,44 PM_STPCPU#
Q3 MMBT3904_SOT23

Compal Electronics, Inc.			
Title: CPU(2/2)			
Size: B	Document Number: LA-2301		Rev: 0.2
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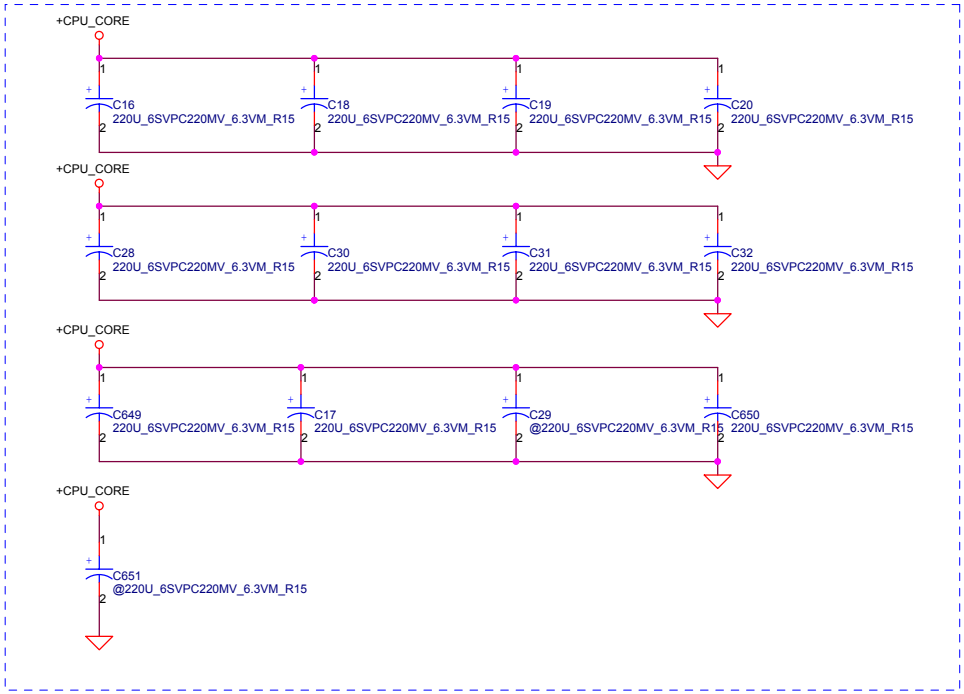
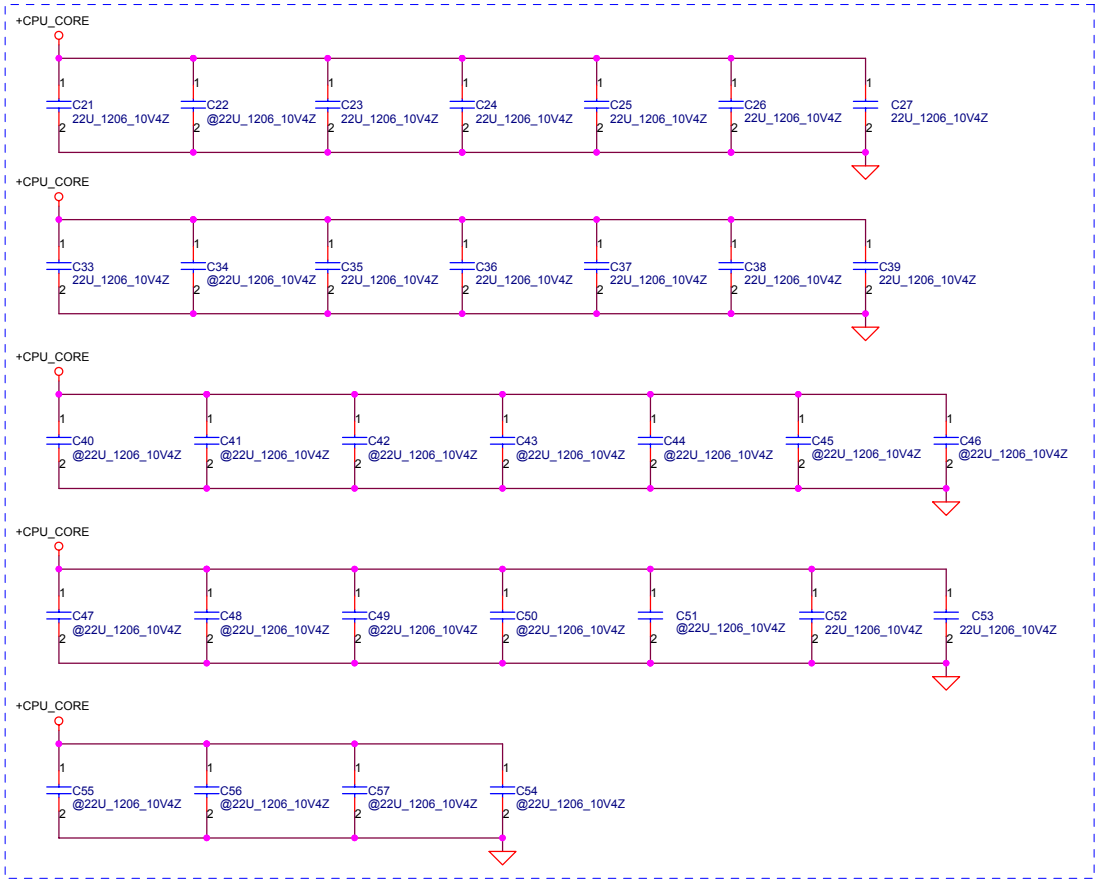
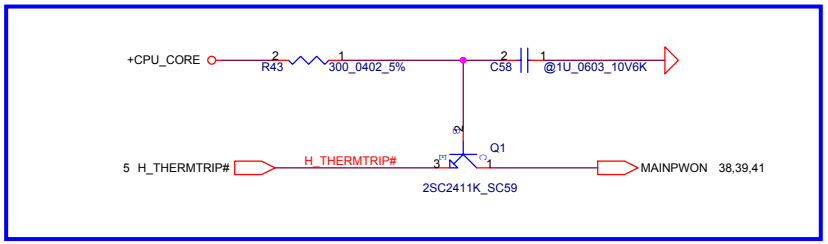




Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Sanyo : SGA27221300 (220uF, 13m Ohm)



Compal Electronics, Inc.		
Title: CPU Decoupling		
Size: E	Document Number: LA-2301	Rev: 0.2
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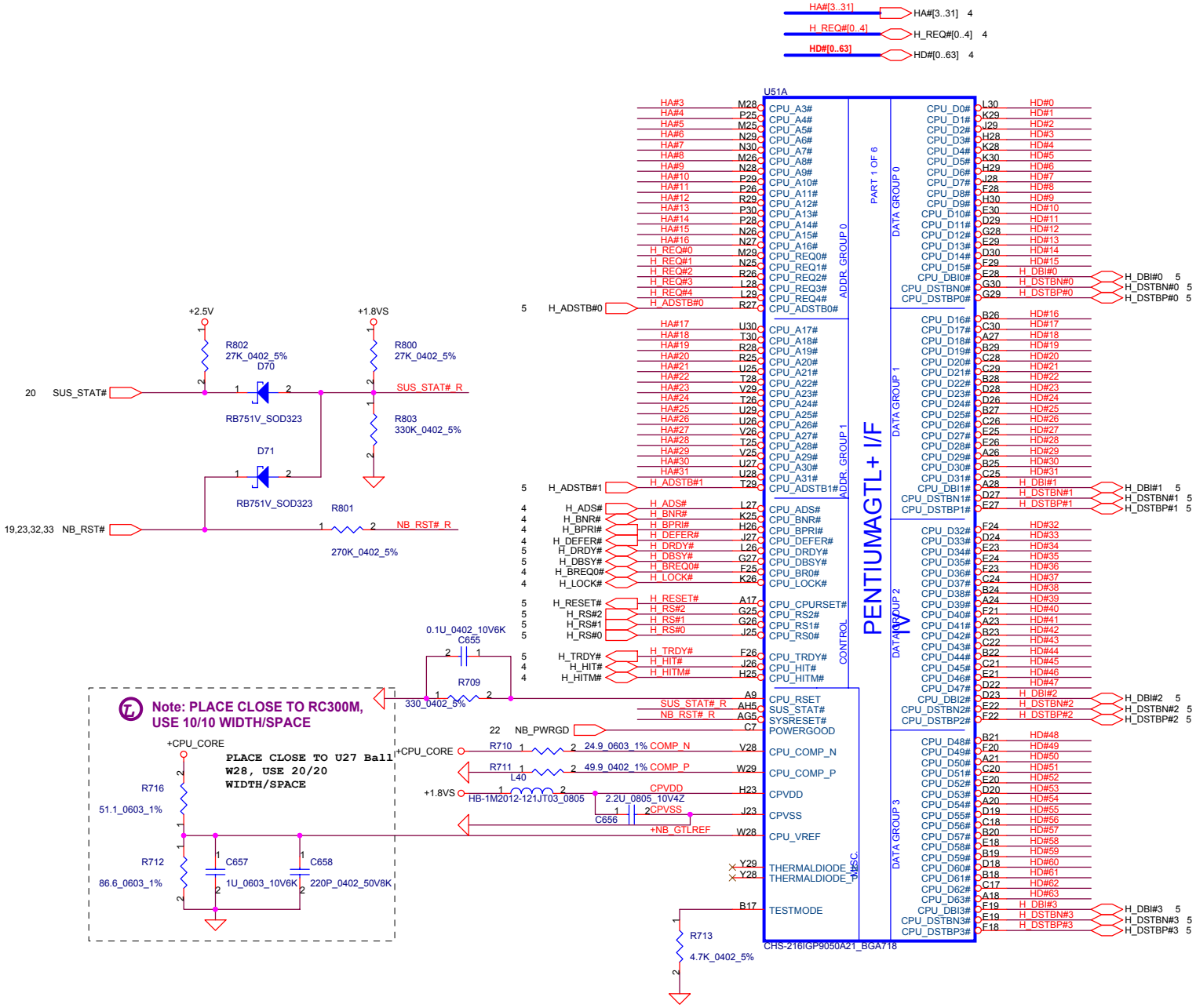

Compal Electronics, Inc.		
Title: ATi RC300ML-HOST(1/5)		
Size: E	Document Number: LA-2301	Rev: 0.2
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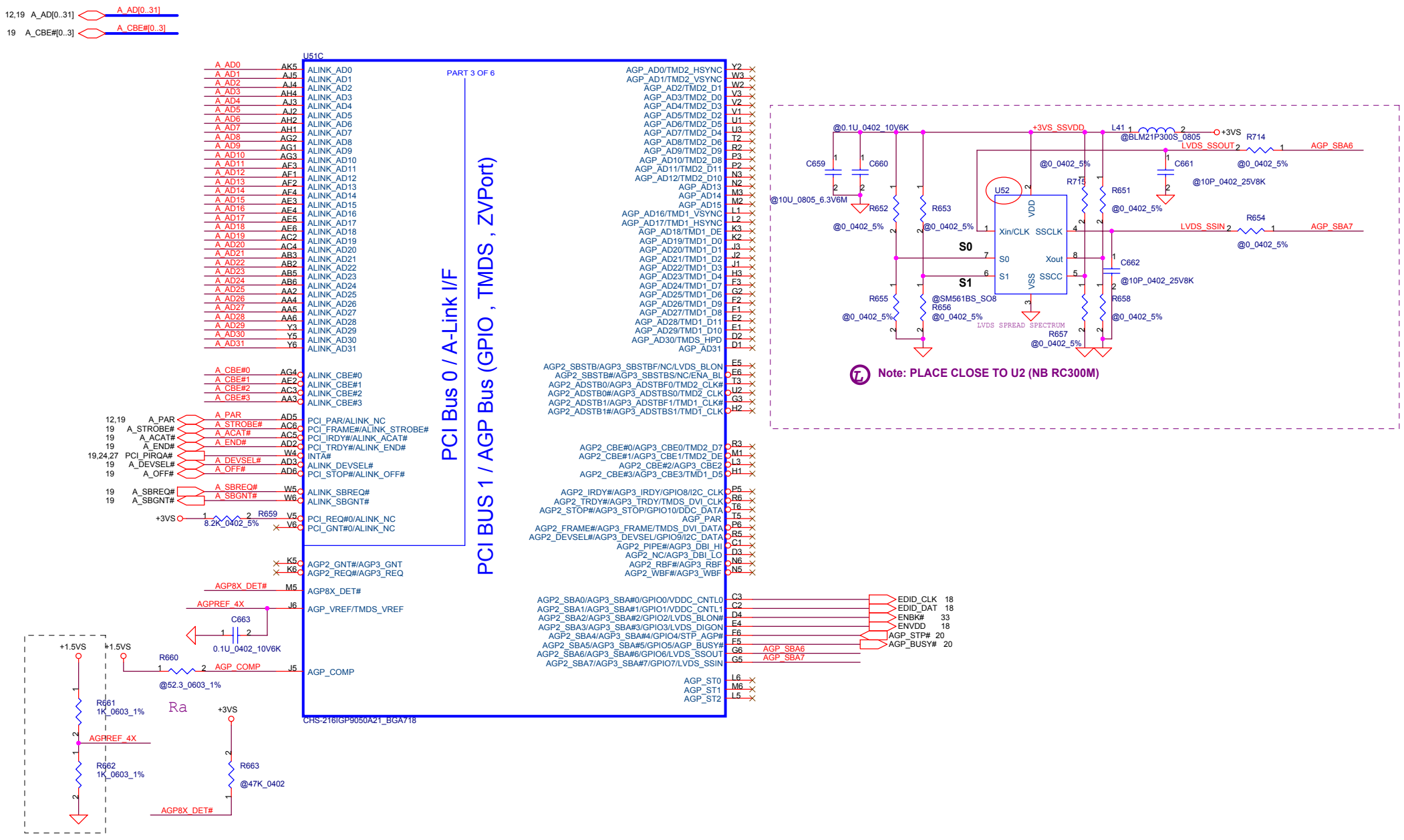

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Title	ATi RC300ML-A-LINK/AGP(2/5)
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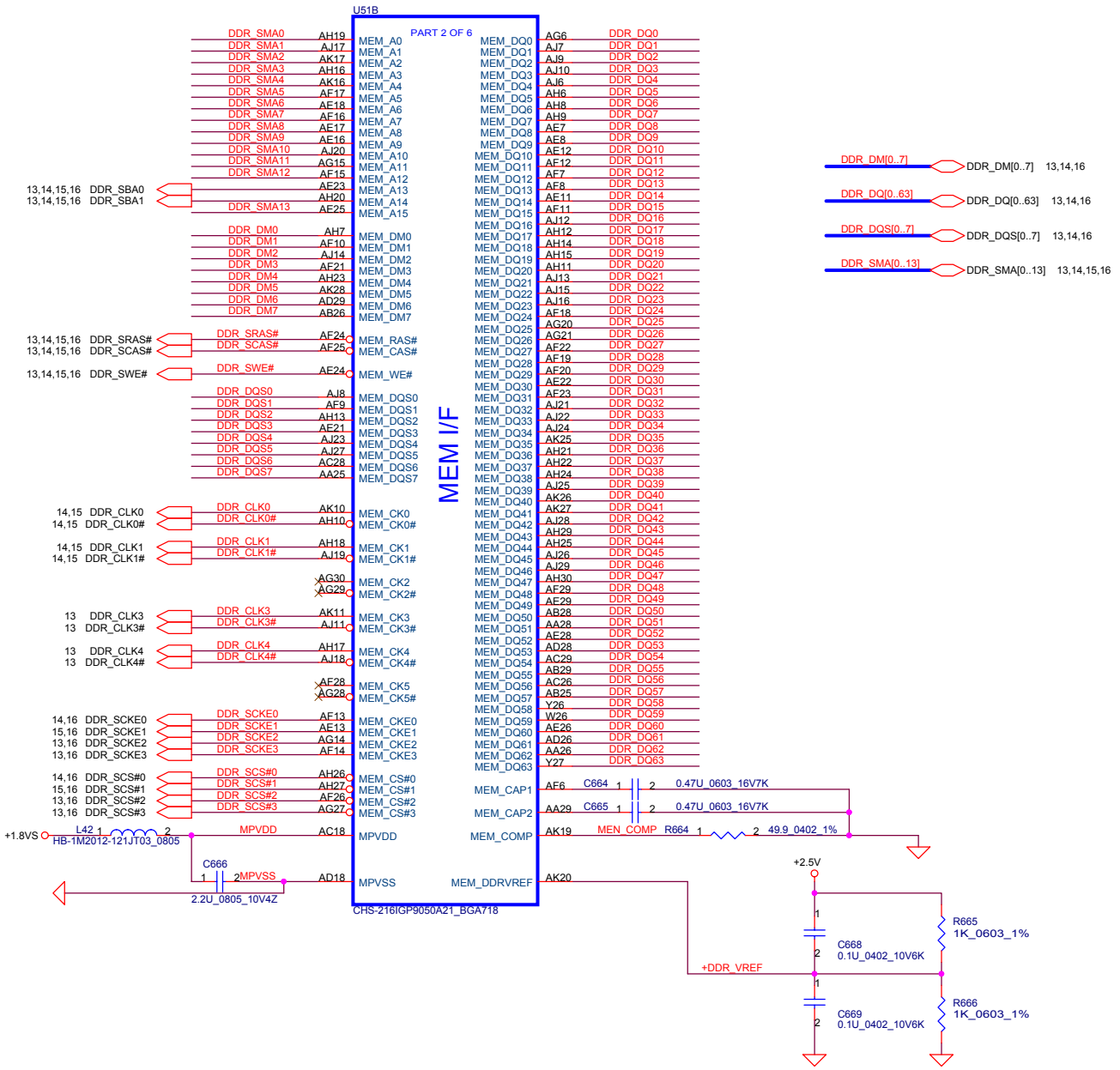

Compal Electronics, Inc.		
Title: ATi RC300ML-DDR(3/5)		
Size: E	Document Number: LA-2301	Rev: 0.2
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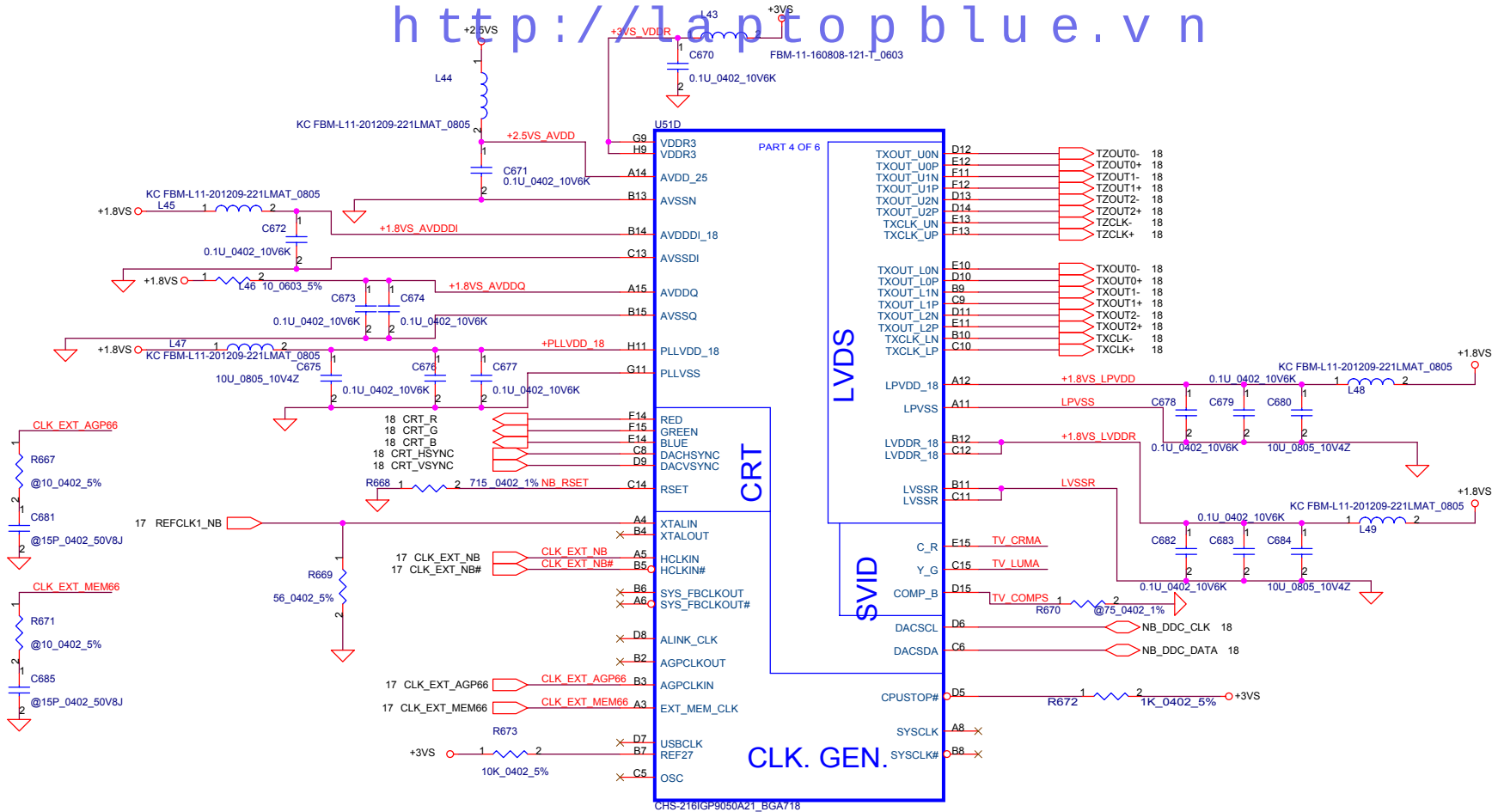

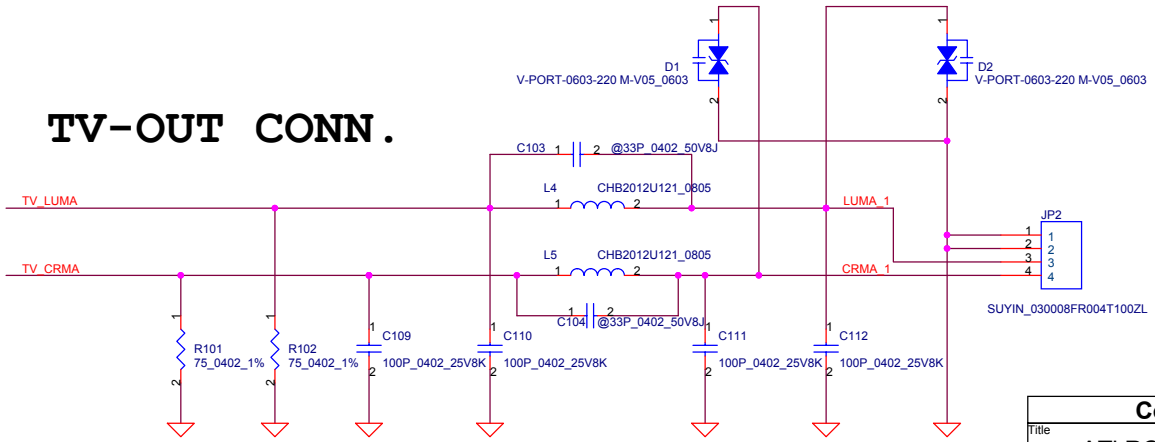

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Title	ATi RC300ML-VEDIO(4/5)
Size: E	Document Number: LA-2301
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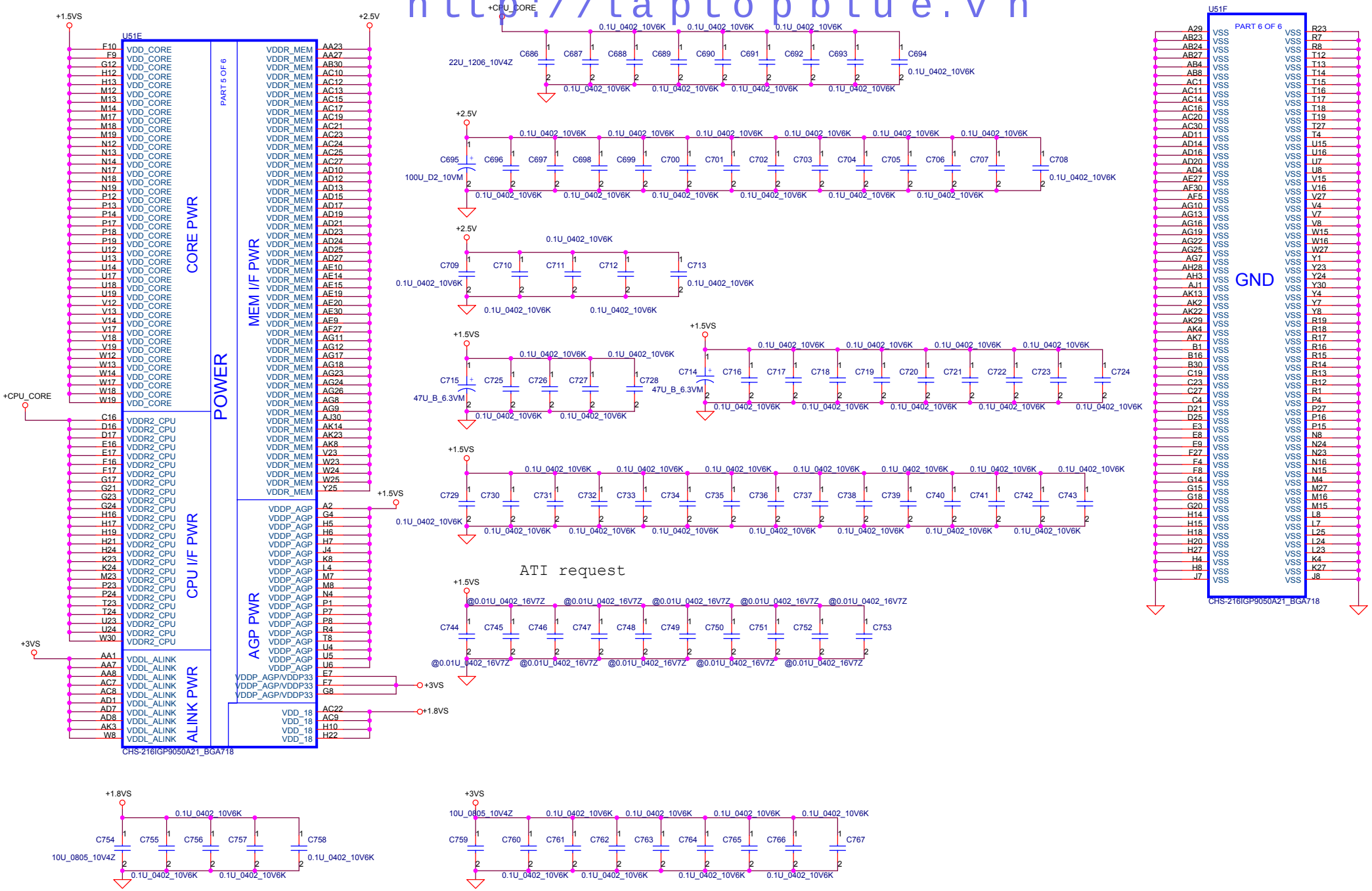

Compal Electronics, Inc.		
Title: ATi RC300ML-Power(5/5)		
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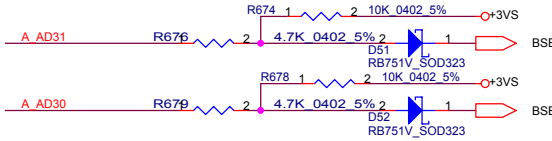
A_CBE#[0..3] — A_CBE#[0..3] 8,19

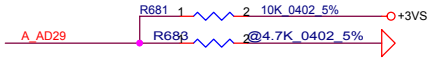
8,19 A_AD[0..31] — A_AD[0..31]



A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

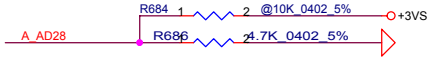
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ



A_AD29: STRAP CONFIGURATION

DEFAULT:1

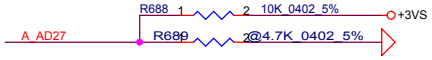
0: REDUCEDE SET
1: FULL SET(internal Pull high)



A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0

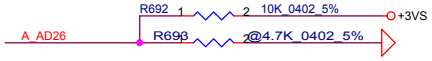
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#

DEFAULT: 1

0: TEST MODE
1: NORMAL MODE



A_AD26 : ENABLE IOQ

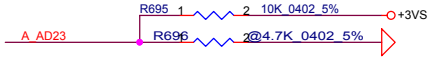
DEFAULT: 1

0: IOQ=1
1: IOQ=12

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

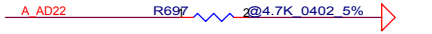
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

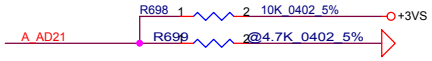
0: TEST MODE
1: NORMAL(internal Pull high)



A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

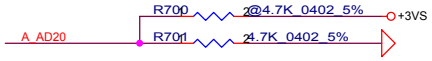
0:PCICLK OUT
1: OSC CLK OUT



A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1

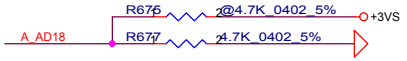
0: DISABLE
1: ENABLE



A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

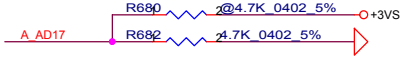
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

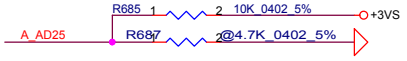
0: DISABLE
1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

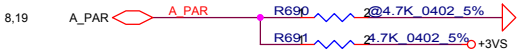


A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17--DON'T CARE



PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

Compal Electronics, Inc.		
Title: ATi RC300ML-SYS. CONFIG.		
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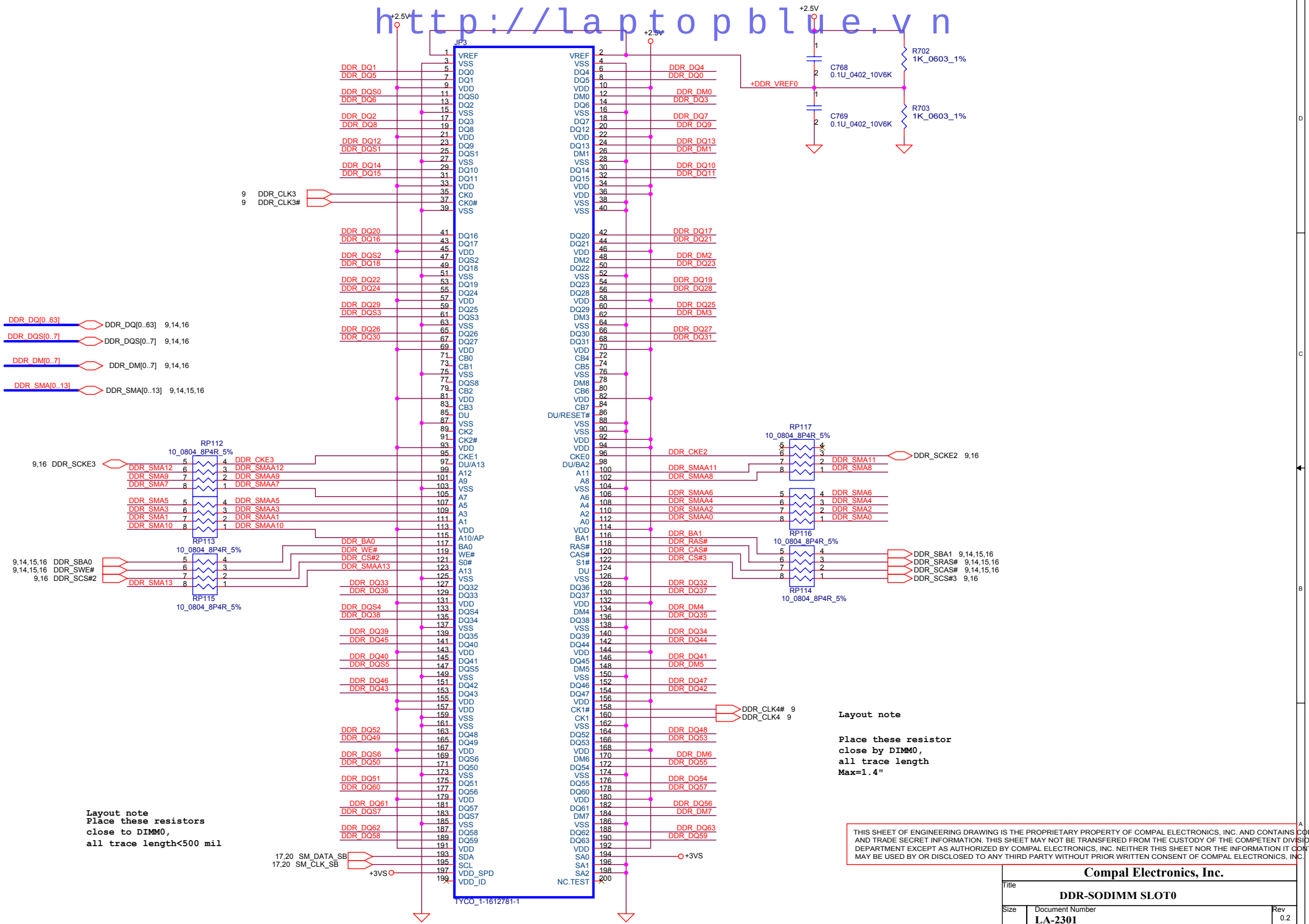

Compal Electronics, Inc.	
Title	DDR-SODIMM SLOT0
Size	Document Number: LA-2301 — Rev: 0.2
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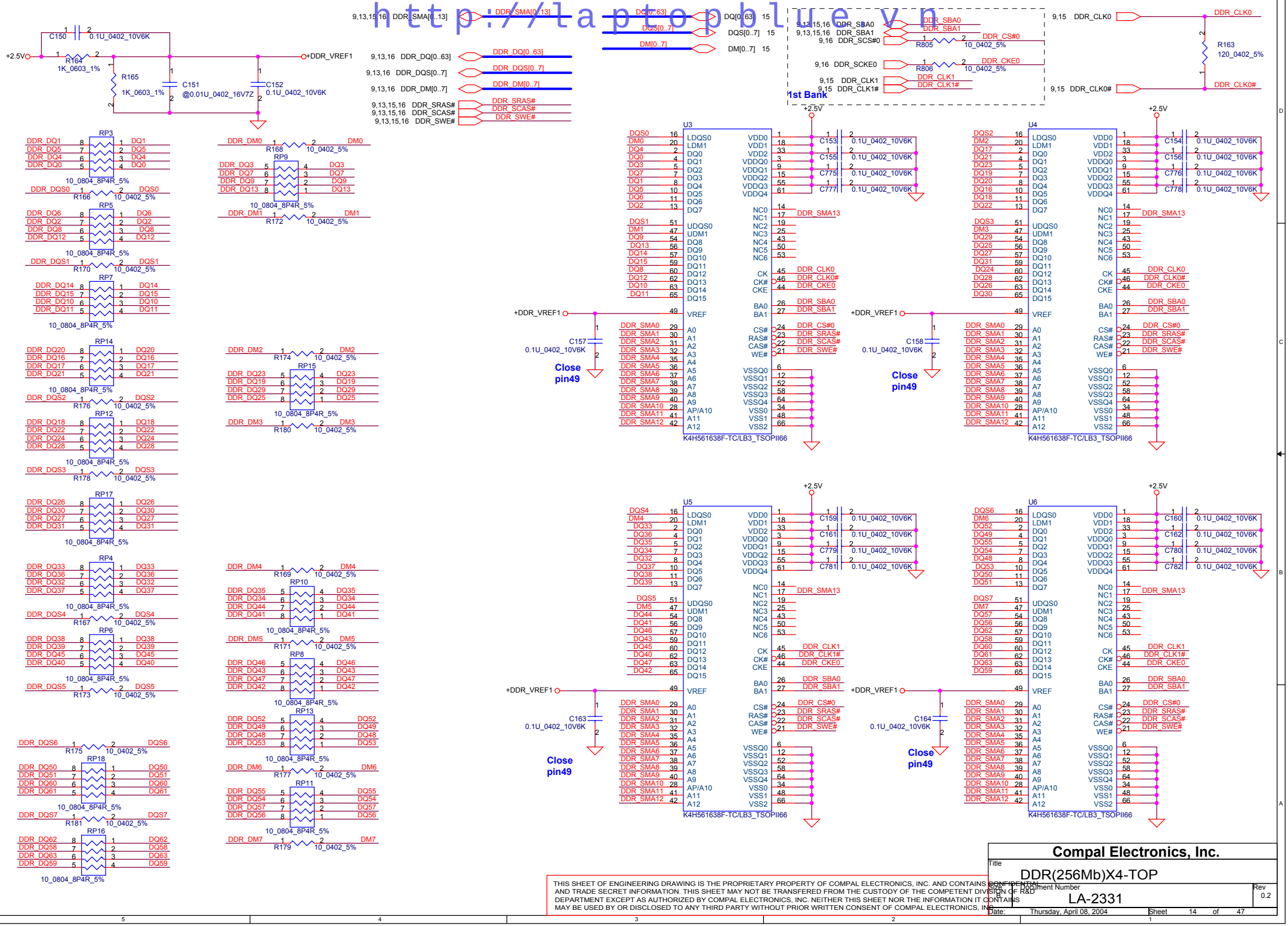

Compal Electronics, Inc.		
Title: DDR(256Mb)X4-TOP		
Size: E	Document Number: LA-2331	Rev: 0.2
Date: Thursday, April 08, 2004	Sheet 14 of 47	

9,13,14,16 DDR_SMA[0..13] — DDR_SMA[0..13]

14 DQ[0..63] — DQ[0..63]

14 DQS[0..7] — DQS[0..7]

14 DM[0..7] — DM[0..7]

9,13,14,16 DDR_SRAS# — DDR_SRAS#

9,13,14,16 DDR_SCAS# — DDR_SCAS#

9,13,14,16 DDR_SWE# — DDR_SWE#

9,13,14,16 DDR_SBA0 — DDR_SBA0

9,13,14,16 DDR_SBA1 — DDR_SBA1

9,16 DDR_SCS#1 — R807 1 2 DDR_CS#1 10_0402_5%

9,16 DDR_SCKE1 — R808 1 2 DDR_CKE1 10_0402_5%

9,14 DDR_CLK0 — DDR_CLK0

9,14 DDR_CLK0# — DDR_CLK0#

2nd Bank

9,14 DDR_CLK1 — DDR_CLK1

R182 120_0402_5%

9,14 DDR_CLK1# — DDR_CLK1#

U8

DQS3	16	LDQS0	VDD0	1	C166 0.1U_0402_10V6K
DM3	20	LDM1	VDD1	18	C168 0.1U_0402_10V6K
DQ30	2	DQ0	VDD2	33	C784 0.1U_0402_10V6K
DQ26	4	DQ1	VDDQ0	3	C786 0.1U_0402_10V6K
DQ28	5	DQ2	VDDQ1	9	
DQ24	7	DQ3	VDDQ2	15	
DQ31	8	DQ4	VDDQ3	55	
DQ27	10	DQ5	VDDQ4	61	
DQ25	11	DQ6			
DQ29	13	DQ7	NC0	14	
			NC1	17	DDR_SMA13
DQS2	51	UDQS0	NC2	19	
DM2	47	UDM1	NC3	25	
DQ22	54	DQ8	NC4	43	
DQ18	56	DQ9	NC5	50	
DQ16	57	DQ10	NC6	53	
DQ20	59	DQ11			
DQ19	60	DQ12	CK	45	DDR_CLK0
DQ23	62	DQ13	CK#	46	DDR_CLK0#
DQ21	63	DQ14	CKE	44	DDR_CKE1
DQ17	65	DQ15			
			BA0	26	DDR_SBA0
	49	VREF	BA1	27	DDR_SBA1
DDR_SMA0	29	A0	CS#	24	DDR_CS#1
DDR_SMA1	30	A1	RAS#	23	DDR_SRAS#
DDR_SMA2	31	A2	CAS#	22	DDR_SCAS#
DDR_SMA3	32	A3	WE#	21	DDR_SWE#
DDR_SMA4	35	A4			
DDR_SMA5	36	A5	VSSQ0	6	
DDR_SMA6	37	A6	VSSQ1	12	
DDR_SMA7	38	A7	VSSQ2	52	
DDR_SMA8	39	A8	VSSQ3	58	
DDR_SMA9	40	A9	VSSQ4	64	
DDR_SMA10	28	AP/A10	VSS0	34	
DDR_SMA11	41	A11	VSS1	48	
DDR_SMA12	42	A12	VSS2	66	

K4H561638F-TC/LB3_TSOPII66

+2.5V — C171 0.1U_0402_10V6K — +DDR_VREF1

DDR_CLK0 — C172 @1.5P_0402_50V8C — DDR_CLK0#

Close to U8 pin5 and 6.

U7

DQS1	16	LDQS0	VDD0	1	C165 0.1U_0402_10V6K
DM1	20	LDM1	VDD1	18	C167 0.1U_0402_10V6K
DQ11	2	DQ0	VDD2	33	C783 0.1U_0402_10V6K
DQ10	4	DQ1	VDDQ0	3	C785 0.1U_0402_10V6K
DQ12	5	DQ2	VDDQ1	9	
DQ8	7	DQ3	VDDQ2	15	
DQ15	8	DQ4	VDDQ3	55	
DQ14	10	DQ5	VDDQ4	61	
DQ13	11	DQ6			
DQ9	13	DQ7	NC0	14	
			NC1	17	DDR_SMA13
DQS0	51	UDQS0	NC2	19	
DM0	47	UDM1	NC3	25	
DQ2	54	DQ8	NC4	43	
DQ6	56	DQ9	NC5	50	
DQ5	57	DQ10	NC6	53	
DQ1	59	DQ11			
DQ7	60	DQ12	CK	45	DDR_CLK0
DQ3	62	DQ13	CK#	46	DDR_CLK0#
DQ0	63	DQ14	CKE	44	DDR_CKE1
DQ4	65	DQ15			
			BA0	26	DDR_SBA0
	49	VREF	BA1	27	DDR_SBA1
DDR_SMA0	29	A0	CS#	24	DDR_CS#1
DDR_SMA1	30	A1	RAS#	23	DDR_SRAS#
DDR_SMA2	31	A2	CAS#	22	DDR_SCAS#
DDR_SMA3	32	A3	WE#	21	DDR_SWE#
DDR_SMA4	35	A4			
DDR_SMA5	36	A5	VSSQ0	6	
DDR_SMA6	37	A6	VSSQ1	12	
DDR_SMA7	38	A7	VSSQ2	52	
DDR_SMA8	39	A8	VSSQ3	58	
DDR_SMA9	40	A9	VSSQ4	64	
DDR_SMA10	28	AP/A10	VSS0	34	
DDR_SMA11	41	A11	VSS1	48	
DDR_SMA12	42	A12	VSS2	66	

K4H561638F-TC/LB3_TSOPII66

+2.5V — C170 0.1U_0402_10V6K — +DDR_VREF1

Close pin49

DDR_CLK0 — C169 @1.5P_0402_50V8C — DDR_CLK0#

Close to U7 pin5 and 6.

U10

DQS7	16	LDQS0	VDD0	1	C174 0.1U_0402_10V6K
DM7	20	LDM1	VDD1	18	C176 0.1U_0402_10V6K
DQ59	2	DQ0	VDD2	33	C788 0.1U_0402_10V6K
DQ63	4	DQ1	VDDQ0	3	C790 0.1U_0402_10V6K
DQ61	5	DQ2	VDDQ1	9	
DQ60	7	DQ3	VDDQ2	15	
DQ58	8	DQ4	VDDQ3	55	
DQ62	10	DQ5	VDDQ4	61	
DQ56	11	DQ6			
DQ57	13	DQ7	NC0	14	
			NC1	17	DDR_SMA13
DQS6	51	UDQS0	NC2	19	
DM6	47	UDM1	NC3	25	
DQ51	54	DQ8	NC4	43	
DQ50	56	DQ9	NC5	50	
DQ53	57	DQ10	NC6	53	
DQ48	59	DQ11			
DQ54	60	DQ12	CK	45	DDR_CLK1
DQ55	62	DQ13	CK#	46	DDR_CLK1#
DQ49	63	DQ14	CKE	44	DDR_CKE1
DQ52	65	DQ15			
			BA0	26	DDR_SBA0
	49	VREF	BA1	27	DDR_SBA1
DDR_SMA0	29	A0	CS#	24	DDR_CS#1
DDR_SMA1	30	A1	RAS#	23	DDR_SRAS#
DDR_SMA2	31	A2	CAS#	22	DDR_SCAS#
DDR_SMA3	32	A3	WE#	21	DDR_SWE#
DDR_SMA4	35	A4			
DDR_SMA5	36	A5	VSSQ0	6	
DDR_SMA6	37	A6	VSSQ1	12	
DDR_SMA7	38	A7	VSSQ2	52	
DDR_SMA8	39	A8	VSSQ3	58	
DDR_SMA9	40	A9	VSSQ4	64	
DDR_SMA10	28	AP/A10	VSS0	34	
DDR_SMA11	41	A11	VSS1	48	
DDR_SMA12	42	A12	VSS2	66	

K4H561638F-TC/LB3_TSOPII66

+2.5V — C180 0.1U_0402_10V6K — +DDR_VREF1

DDR_CLK1 — C179 @1.5P_0402_50V8C — DDR_CLK1#

Close to U10 pin5 and 6.

U9

DQS5	16	LDQS0	VDD0	1	C173 0.1U_0402_10V6K
DM5	20	LDM1	VDD1	18	C175 0.1U_0402_10V6K
DQ42	2	DQ0	VDD2	33	C787 0.1U_0402_10V6K
DQ47	4	DQ1	VDDQ0	3	C789 0.1U_0402_10V6K
DQ40	5	DQ2	VDDQ1	9	
DQ45	7	DQ3	VDDQ2	15	
DQ43	8	DQ4	VDDQ3	55	
DQ46	10	DQ5	VDDQ4	61	
DQ41	11	DQ6			
DQ44	13	DQ7	NC0	14	
			NC1	17	DDR_SMA13
DQS4	51	UDQS0	NC2	19	
DM4	47	UDM1	NC3	25	
DQ39	54	DQ8	NC4	43	
DQ38	56	DQ9	NC5	50	
DQ37	57	DQ10	NC6	53	
DQ32	59	DQ11			
DQ34	60	DQ12	CK	45	DDR_CLK1
DQ35	62	DQ13	CK#	46	DDR_CLK1#
DQ36	63	DQ14	CKE	44	DDR_CKE1
DQ33	65	DQ15			
			BA0	26	DDR_SBA0
	49	VREF	BA1	27	DDR_SBA1
DDR_SMA0	29	A0	CS#	24	DDR_CS#1
DDR_SMA1	30	A1	RAS#	23	DDR_SRAS#
DDR_SMA2	31	A2	CAS#	22	DDR_SCAS#
DDR_SMA3	32	A3	WE#	21	DDR_SWE#
DDR_SMA4	35	A4			
DDR_SMA5	36	A5	VSSQ0	6	
DDR_SMA6	37	A6	VSSQ1	12	
DDR_SMA7	38	A7	VSSQ2	52	
DDR_SMA8	39	A8	VSSQ3	58	
DDR_SMA9	40	A9	VSSQ4	64	
DDR_SMA10	28	AP/A10	VSS0	34	
DDR_SMA11	41	A11	VSS1	48	
DDR_SMA12	42	A12	VSS2	66	

K4H561638F-TC/LB3_TSOPII66

+2.5V — C178 0.1U_0402_10V6K — +DDR_VREF1

Close pin49

DDR_CLK1 — C177 @1.5P_0402_50V8C — DDR_CLK1#

Close to U9 pin5 and 6.

Compal Electronics, Inc.

Title: DDR(256Mb)X4-BTN

Size: E — Document Number: LA-2331 — Rev: 0.2

Date: Thursday, April 08, 2004 — Sheet 15 of 47

9,13,14,15 DDR_SMA[0..13] — DDR_SMA[0..13]
9,13,14,15 DDR_SCKE[0..3] — DDR_SCKE[0..3]
9,13,14 DDR_DQ[0..63] — DDR_DQ[0..63]
9,13,14 DDR_DQS[0..7] — DDR_DQS[0..7]
9,13,14 DDR_DM[0..7] — DDR_DM[0..7]

+1.25VS

DDR_SCKE1 — 33_0402_5% — R203 — C185 0.1U_0402_10V6K
DDR_SCKE0 — 33_0402_5% — R202
DDR_SCKE2 — 33_0402_5% — R201 — C188 0.1U_0402_10V6K

RP46 (33_0804_8P4R_5%)
DDR_SMA8 — C193 0.1U_0402_10V6K
DDR_SMA11
DDR_SMA6
DDR_SMA4 — C194 0.1U_0402_10V6K

RP62 (33_0804_8P4R_5%)
DDR_SMA2 — C199 0.1U_0402_10V6K
DDR_SMA0
9,13,14,15 DDR_SBA1 — DDR_SBA1
9,13,14,15 DDR_SRAS# — DDR_SRAS# — C200 0.1U_0402_10V6K

RP43 (33_0804_8P4R_5%)
9,13,14,15 DDR_SCAS# — DDR_SCAS# — C205 0.1U_0402_10V6K
9,15 DDR_SCS#1 — DDR_SCS#1
9,14 DDR_SCS#0 — DDR_SCS#0
9,13 DDR_SCS#3 — DDR_SCS#3 — C206 0.1U_0402_10V6K

RP59 (33_0804_8P4R_5%)
DDR_SCKE3 — C211 0.1U_0402_10V6K
DDR_SMA12
DDR_SMA9 — C214 0.1U_0402_10V6K
DDR_SMA7

RP54 (33_0804_8P4R_5%)
DDR_SMA5 — C219 0.1U_0402_10V6K
DDR_SMA3
DDR_SMA1 — C222 0.1U_0402_10V6K
DDR_SMA10

RP51 (33_0804_8P4R_5%)
9,13,14,15 DDR_SBA0 — DDR_SBA0
9,13,14,15 DDR_SWE# — DDR_SWE# — C225 0.1U_0402_10V6K
9,13 DDR_SCS#2 — DDR_SCS#2
DDR_SMA13

+1.25VS

RP41 (56_0804_8P4R_5%)
DDR_DQ1 — C183 0.1U_0402_10V6K
DDR_DQ5
DDR_DQ4
DDR_DQ0 — C186 0.1U_0402_10V6K

RP44 (56_0804_8P4R_5%)
DDR_DM0 — C189 0.1U_0402_10V6K
DDR_DQS0
DDR_DQ6
DDR_DQ2 — C191 0.1U_0402_10V6K

RP47 (56_0804_8P4R_5%)
DDR_DQ3 — C195 0.1U_0402_10V6K
DDR_DQ7
DDR_DQ8
DDR_DQ12 — C197 0.1U_0402_10V6K

RP49 (56_0804_8P4R_5%)
DDR_DQ9 — C201 0.1U_0402_10V6K
DDR_DQ13
DDR_DM1
DDR_DQS1 — C203 0.1U_0402_10V6K

RP52 (56_0804_8P4R_5%)
DDR_DQ14 — C207 0.1U_0402_10V6K
DDR_DQ15
DDR_DQ10
DDR_DQ11 — C209 0.1U_0402_10V6K

RP55 (56_0804_8P4R_5%)
DDR_DQ20 — C212 0.1U_0402_10V6K
DDR_DQ16
DDR_DQ17
DDR_DQ21 — C215 0.1U_0402_10V6K

RP57 (56_0804_8P4R_5%)
DDR_DQS2 — C217 0.1U_0402_10V6K
DDR_DM2
DDR_DQ18
DDR_DQ22 — C220 0.1U_0402_10V6K

RP60 (56_0804_8P4R_5%)
DDR_DQ23 — C223 0.1U_0402_10V6K
DDR_DQ19
DDR_DQ24
DDR_DQ28 — C226 0.1U_0402_10V6K

RP63 (56_0804_8P4R_5%)
DDR_DQ29 — C228 0.1U_0402_10V6K
DDR_DQ25
DDR_DQS3
DDR_DM3 — C230 0.1U_0402_10V6K

RP65 (56_0804_8P4R_5%)
DDR_DQ26 — C232 0.1U_0402_10V6K
DDR_DQ30
DDR_DQ27
DDR_DQ31 — C234 0.1U_0402_10V6K

+1.25VS

RP50 (56_0804_8P4R_5%)
DDR_DQ33 — C184 0.1U_0402_10V6K
DDR_DQ36
DDR_DQ32
DDR_DQ37 — C187 0.1U_0402_10V6K

RP53 (56_0804_8P4R_5%)
DDR_DQS4 — C190 0.1U_0402_10V6K
DDR_DM4
DDR_DQ38
DDR_DQ39 — C192 0.1U_0402_10V6K

RP42 (56_0804_8P4R_5%)
DDR_DQ35 — C196 0.1U_0402_10V6K
DDR_DQ34
DDR_DQ45
DDR_DQ40 — C198 0.1U_0402_10V6K

RP45 (56_0804_8P4R_5%)
DDR_DQ44 — C202 0.1U_0402_10V6K
DDR_DQ41
DDR_DQS5
DDR_DM5 — C204 0.1U_0402_10V6K

RP48 (56_0804_8P4R_5%)
DDR_DQ46 — C208 0.1U_0402_10V6K
DDR_DQ43
DDR_DQ47
DDR_DQ42 — C210 0.1U_0402_10V6K

RP56 (56_0804_8P4R_5%)
DDR_DQ52 — C213 0.1U_0402_10V6K
DDR_DQ49
DDR_DQ48
DDR_DQ53 — C216 0.1U_0402_10V6K

RP58 (56_0804_8P4R_5%)
DDR_DM6 — C218 0.1U_0402_10V6K
DDR_DQS6
DDR_DQ50
DDR_DQ51 — C221 0.1U_0402_10V6K

RP61 (56_0804_8P4R_5%)
DDR_DQ55 — C224 0.1U_0402_10V6K
DDR_DQ54
DDR_DQ60
DDR_DQ61 — C227 0.1U_0402_10V6K

RP64 (56_0804_8P4R_5%)
DDR_DQ57 — C229 0.1U_0402_10V6K
DDR_DQ56
DDR_DM7
DDR_DQS7 — C231 0.1U_0402_10V6K

RP66 (56_0804_8P4R_5%)
DDR_DQ62 — C233 0.1U_0402_10V6K
DDR_DQ58
DDR_DQ63
DDR_DQ59 — C235 0.1U_0402_10V6K

+2.5V

C771 100U_D2_10VM — C236 100U_D2_10VM — C237 — C238 — C239 — C240 — C241 — C242 — C243 — C244 — C245 — C246
(C237–C246: 0.1U_0402_10V6K)

+2.5V

C772 100U_D2_10VM — C247 100U_D2_10VM — C248 — C249 — C250 — C251 — C252 — C253 — C254 — C255 — C256 — C257
(C248–C257: 0.1U_0402_10V6K)

Compal Electronics, Inc.		
Title: DDR-SODIMM Decoupling		
Size: E	Document Number: LA-2301	Rev: 0.2
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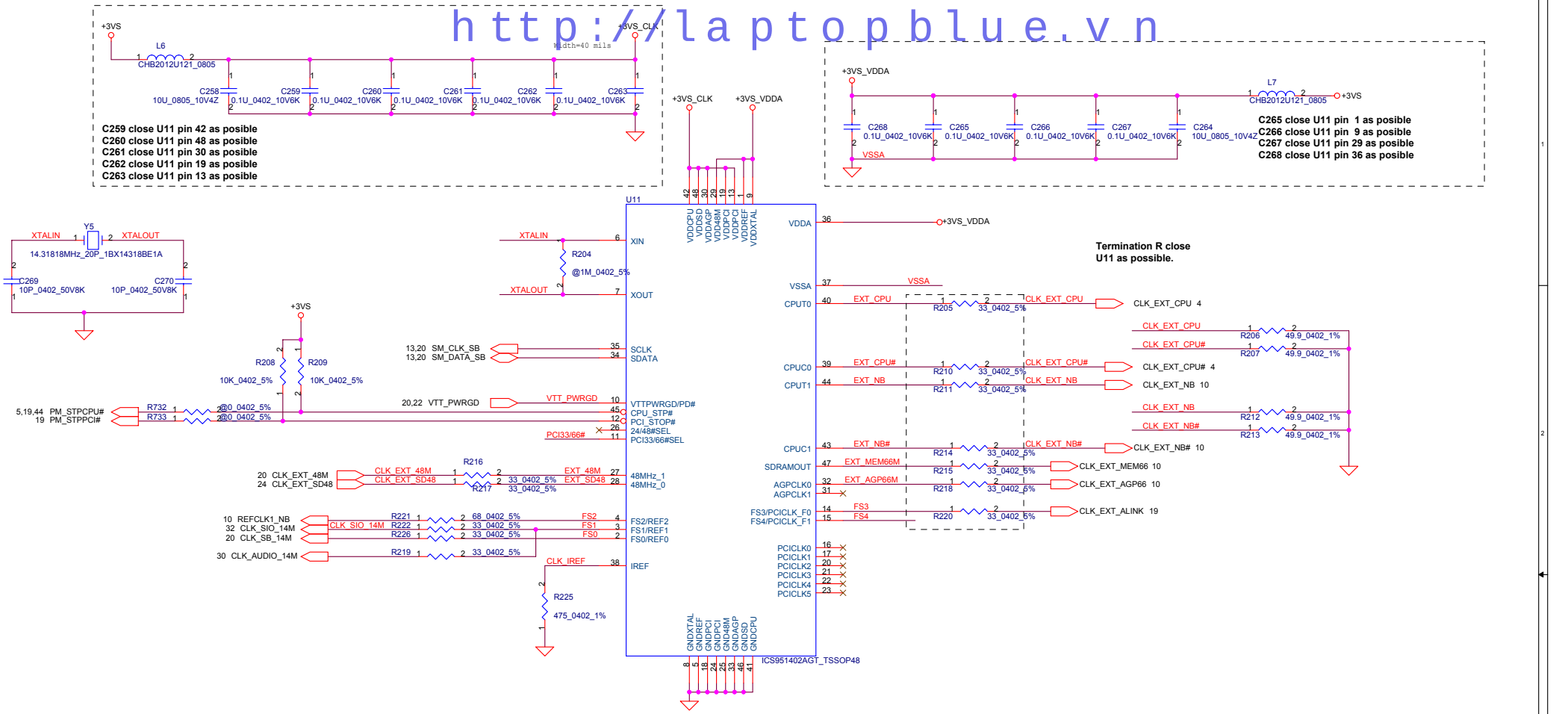

CLOCK FREQUENCY SELECT TABLE

	FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled
	0	0	0	1	0	200	200	
**	0	0	0	0	1	133	133	Spread OFF OR Center spread +/-0.3%
	0	0	0	0	0	100	100	

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

Compal Electronics, Inc.

Title: Clock Generator

Size: Document Number: LA-2301

Rev: 0.2

Date: Thursday, April 08, 2004

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SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

Width: 40mils

CRT Connector

Close to CRT connector

Compal Electronics, Inc.	
Title	LVDS, CRT& TV CONN
Size: E	Document Number: LA-2301
Rev	0.2
Date: Thursday, April 08, 2004	Sheet 18 of 47

Layout note:
Trace length of PCI_CLK_R +PCI_CLK_FB should be less than 200 mils.

U14A
SB150 SB
Part 1 of 3
CHS-215IXP150-11_BGA457

GPOC3#	GPOC2#	GPIO1			
RAM_SEL2	RAM_SEL1	RAM_SEL0	Size	Vendor	Cells
0	0	0	256M(16X16)	SAM	8
0	0	1	256M(16X16)	HYN	8
0	1	0	256M(16X16)	Elpida	8
0	1	1	256M(16X16)	Infienon	8
1	0	0	512M(32X16)	SAM	8
1	0	1	512M(32X16)	HYN	8
1	1	0	512M(32X16)	Elpida	8
1	1	1	512M(32X16)	Infienon	8

Add for EMI

Compal Electronics, Inc.

Title: IXP150(1/4)- PCI/CPU/LPC

Size: | Document Number: LA-2301 | Rev: 0.2

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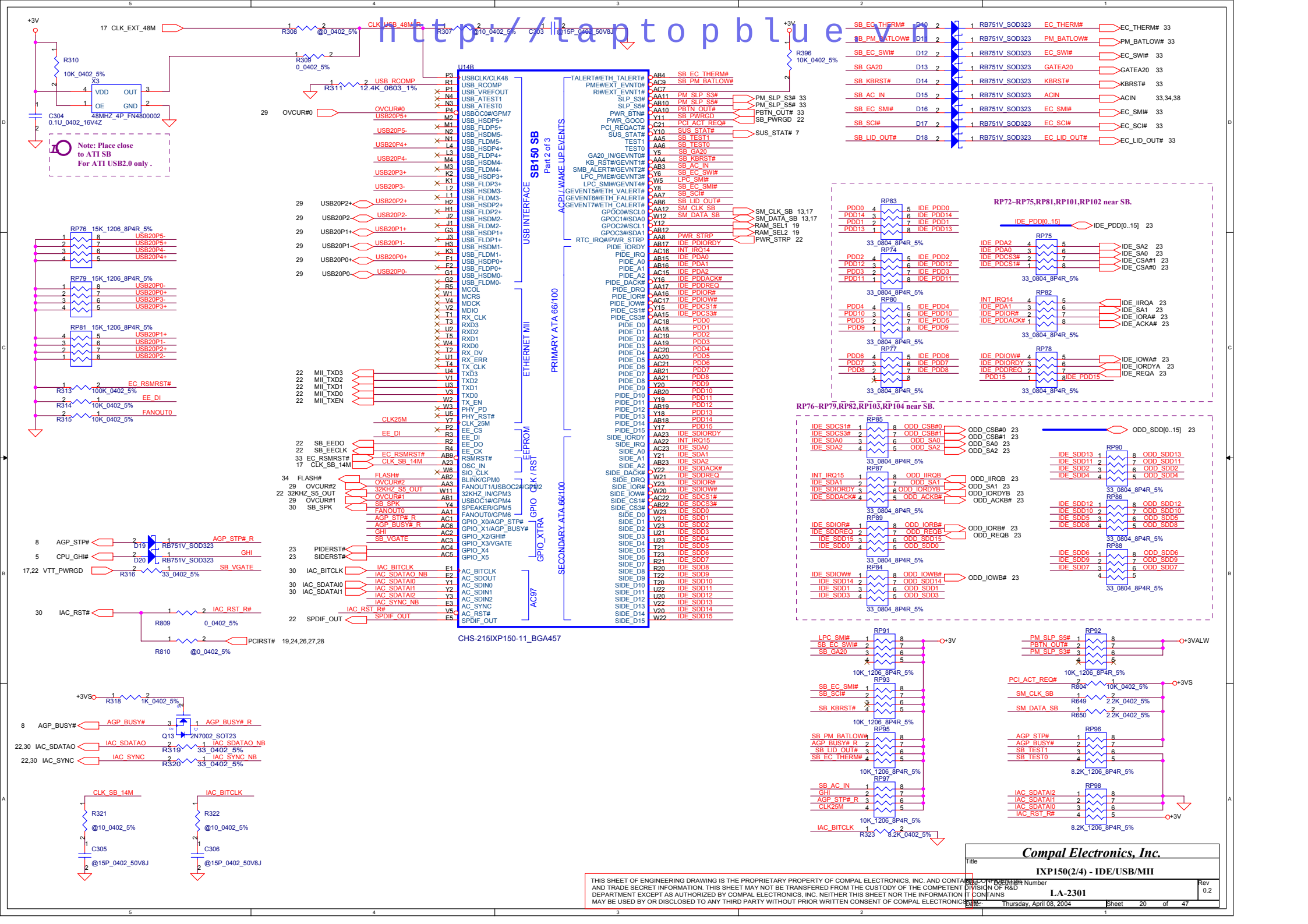

Compal Electronics, Inc.	
Title	IXP150(2/4) - IDE/USB/MII
Size	Document Number: LA-2301
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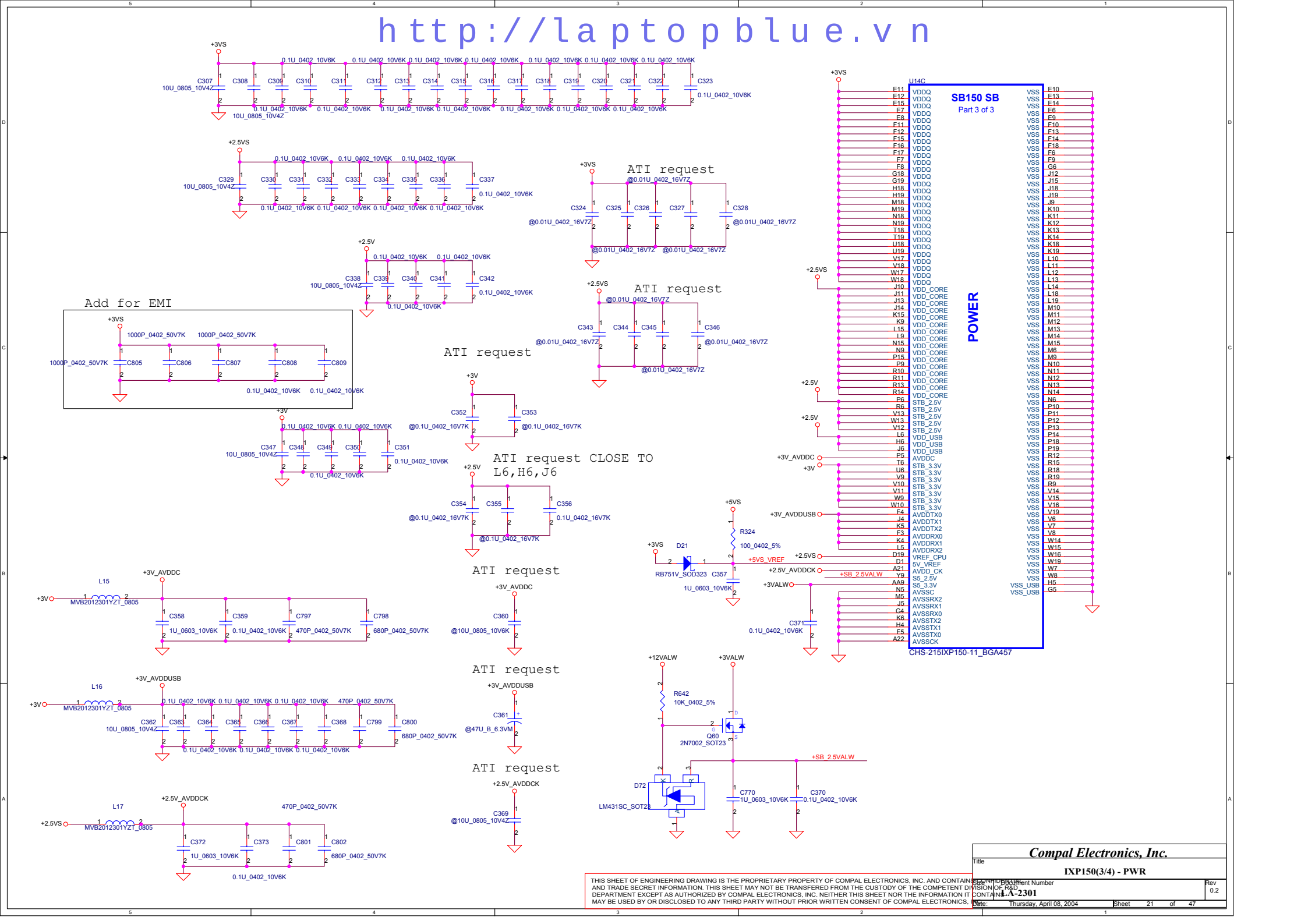

Compal Electronics, Inc.		
Title: IXP150(3/4) - PWR		
Size: A3	Document Number: LA-2301	Rev: 0.2
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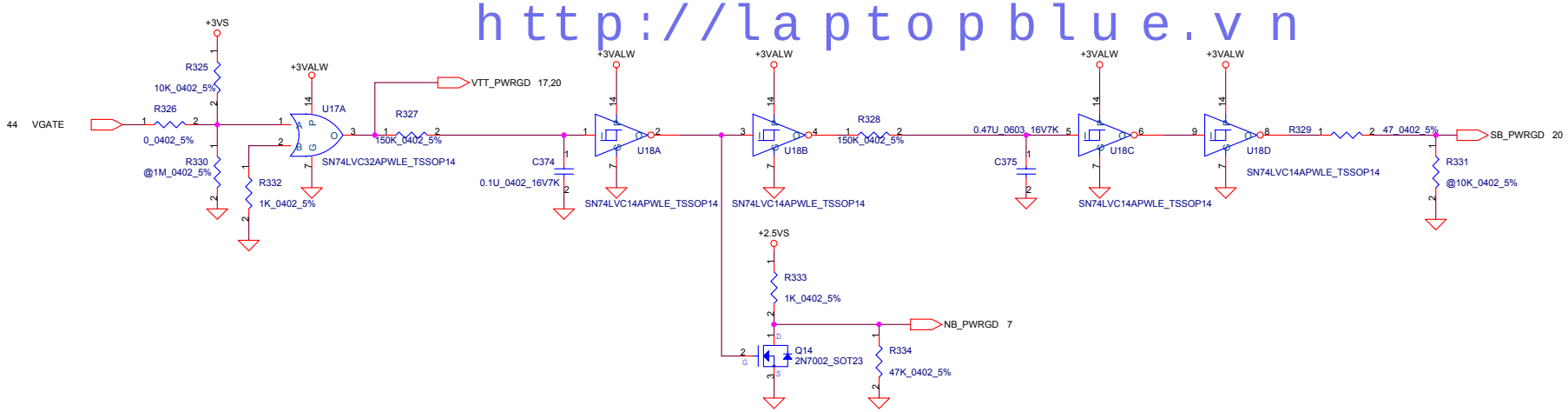
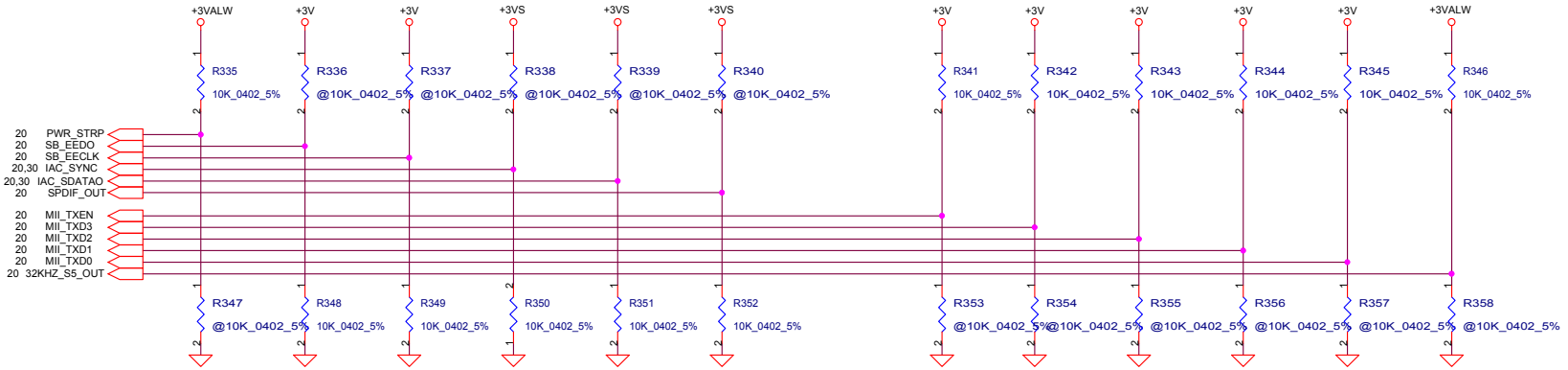
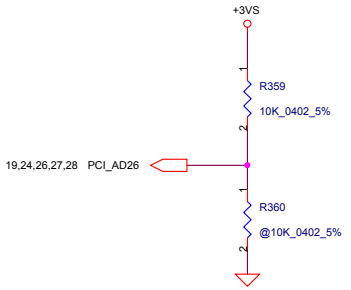




REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



Compal Electronics, Inc.

Title: IXP150(4/4) - STRAPS

Size: C | Document Number: LA-2301 | Rev: 0.2

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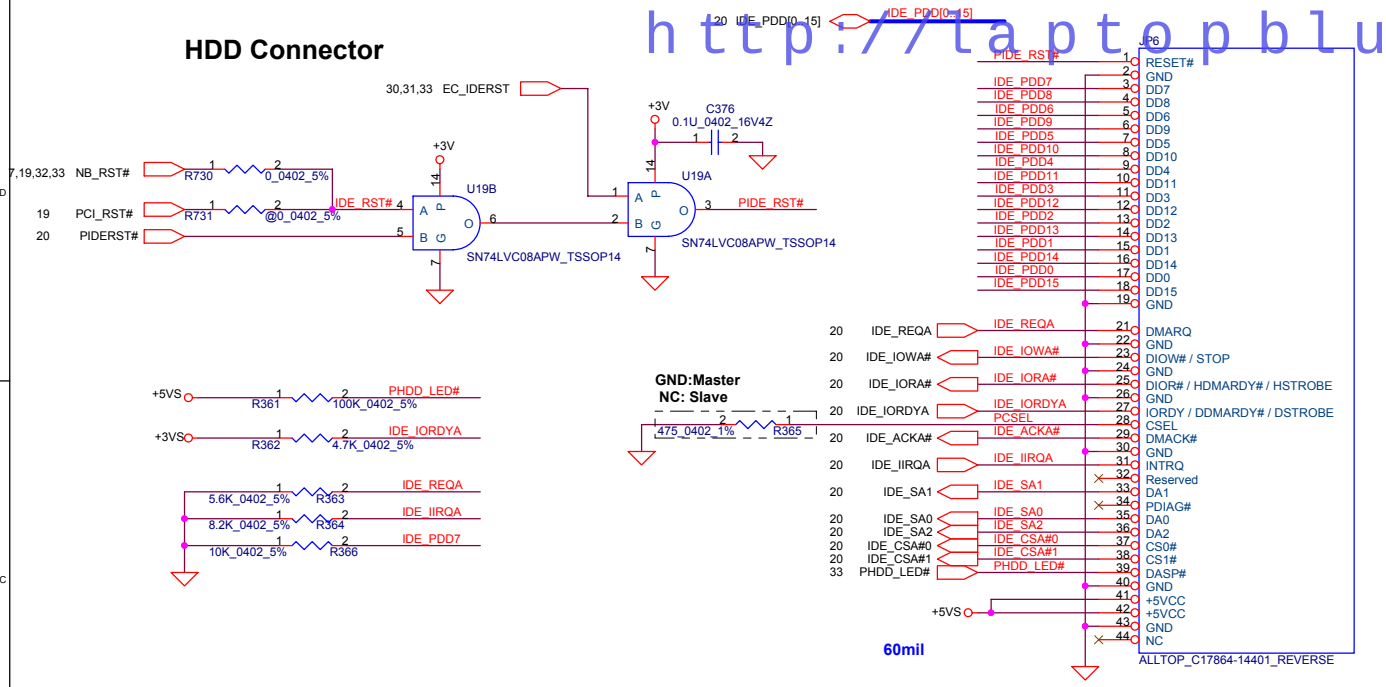
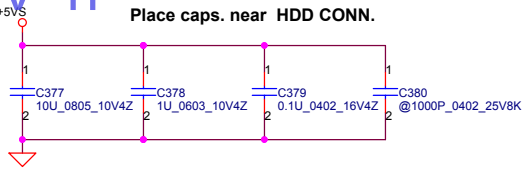
HDD Connector

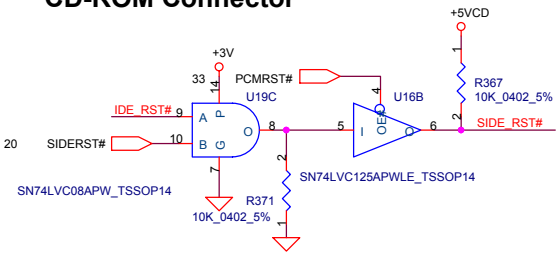


Place caps. near HDD CONN.

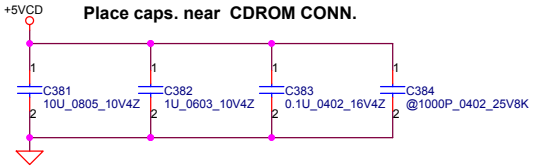


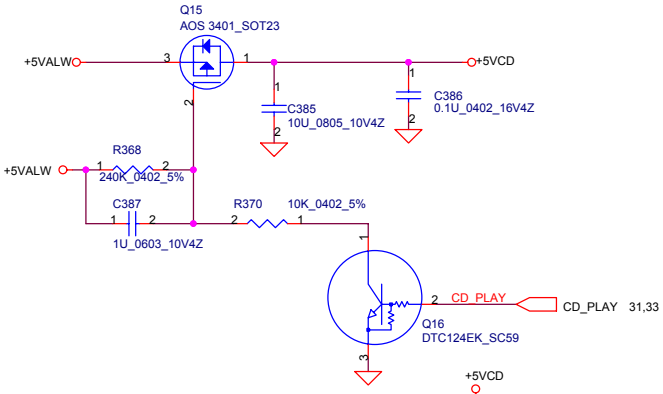
Net width should be 60mil wide

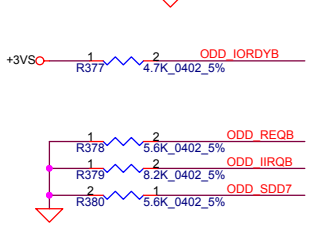
CD-ROM Connector

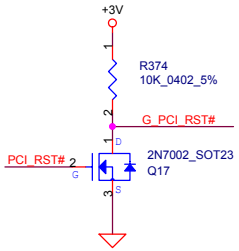


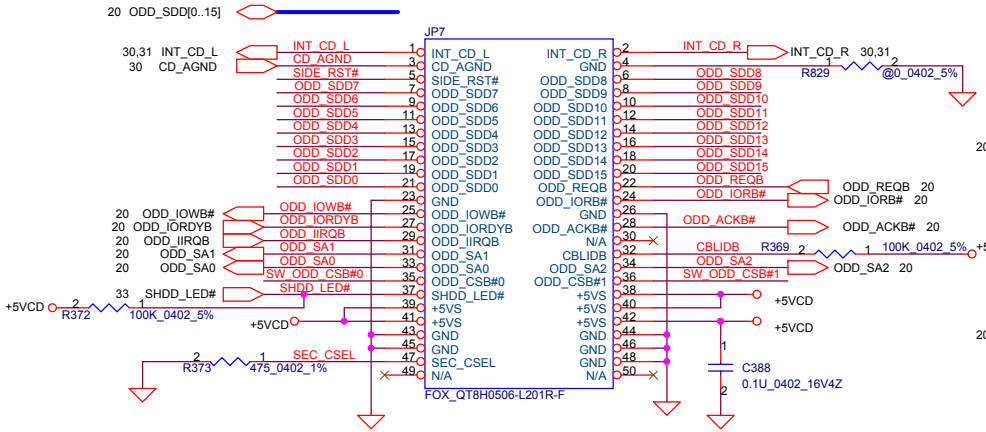
Place caps. near CDROM CONN.

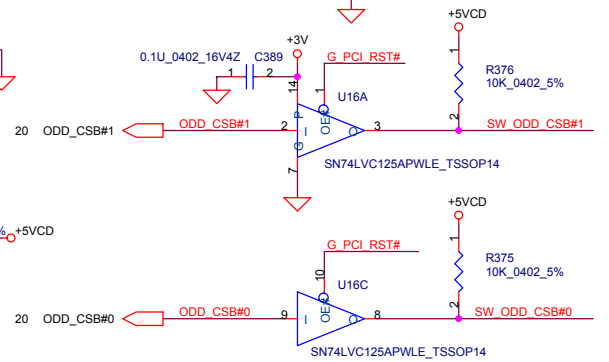




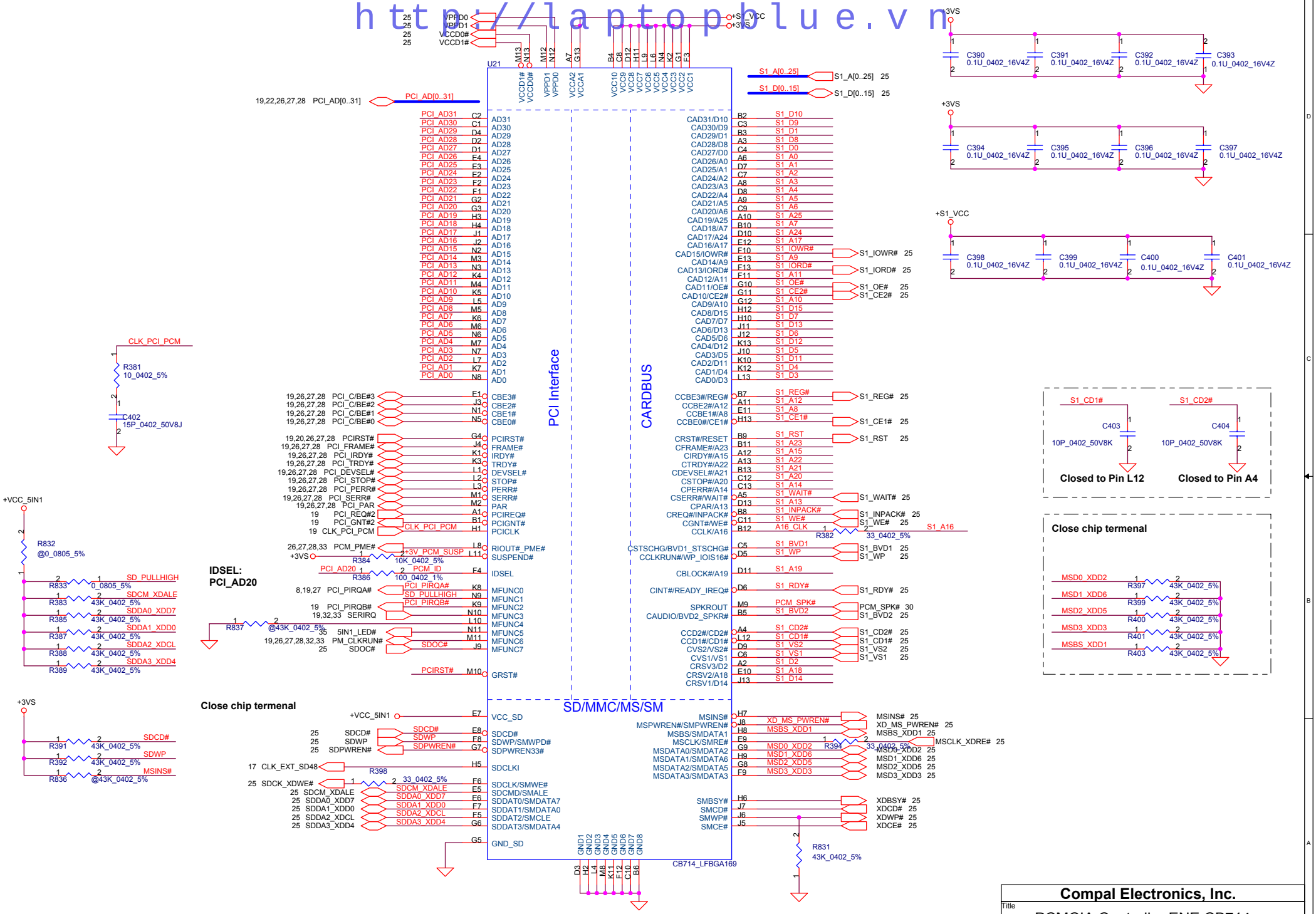








Compal Electronics, Inc.			
Title: IDE/CDROM CONN.			
Size: E	Document Number: LA-2301		Rev: 0.2
Date: Thursday, April 08, 2004	Sheet 23 of 47		



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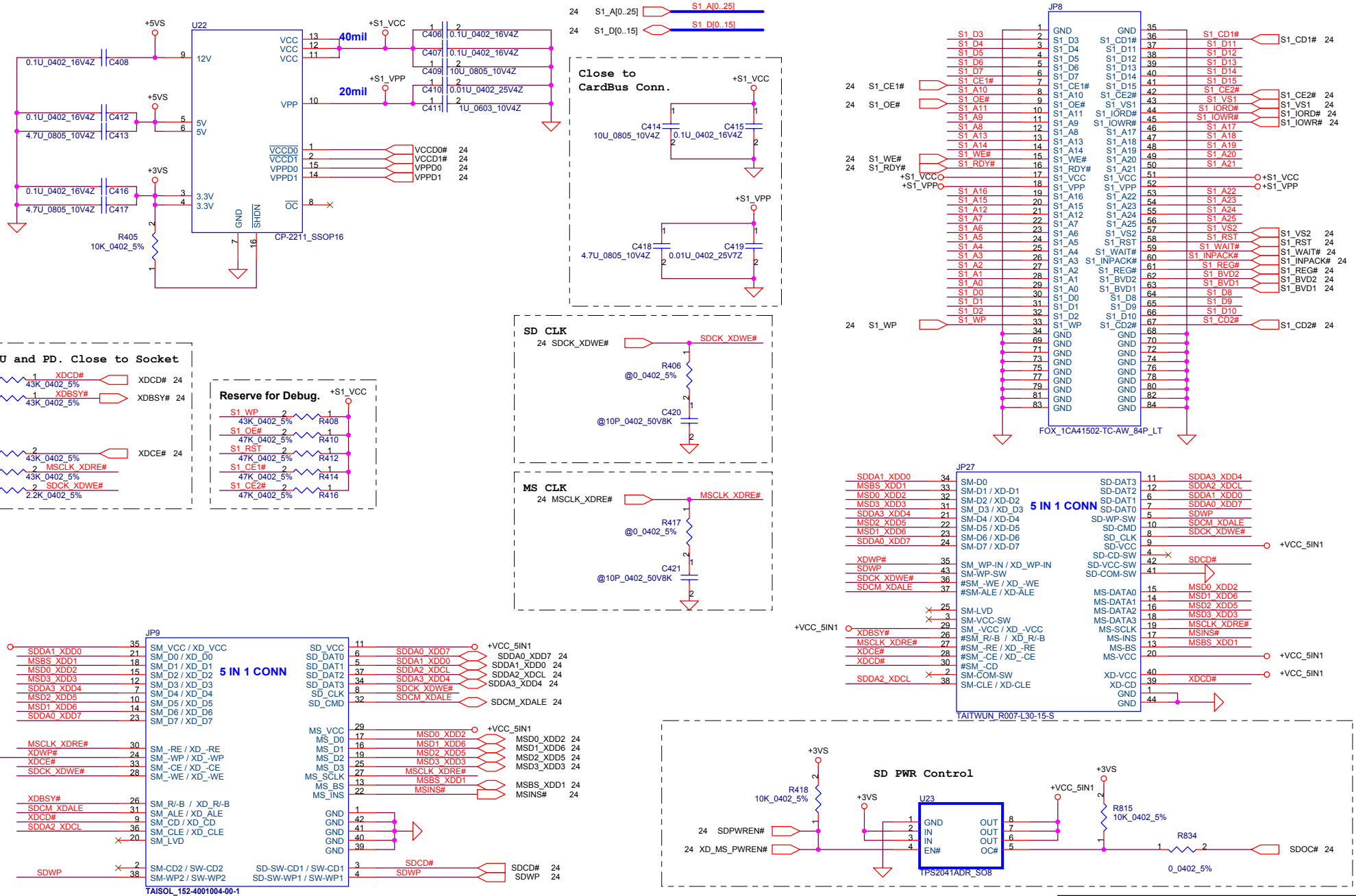
Compal Electronics, Inc.

Title	PCMCIA Controller ENE CB714		
Size: E	Document Number: LA-2301		Rev: 0.2
Date: Thursday, April 08, 2004	Sheet 24 of 47		

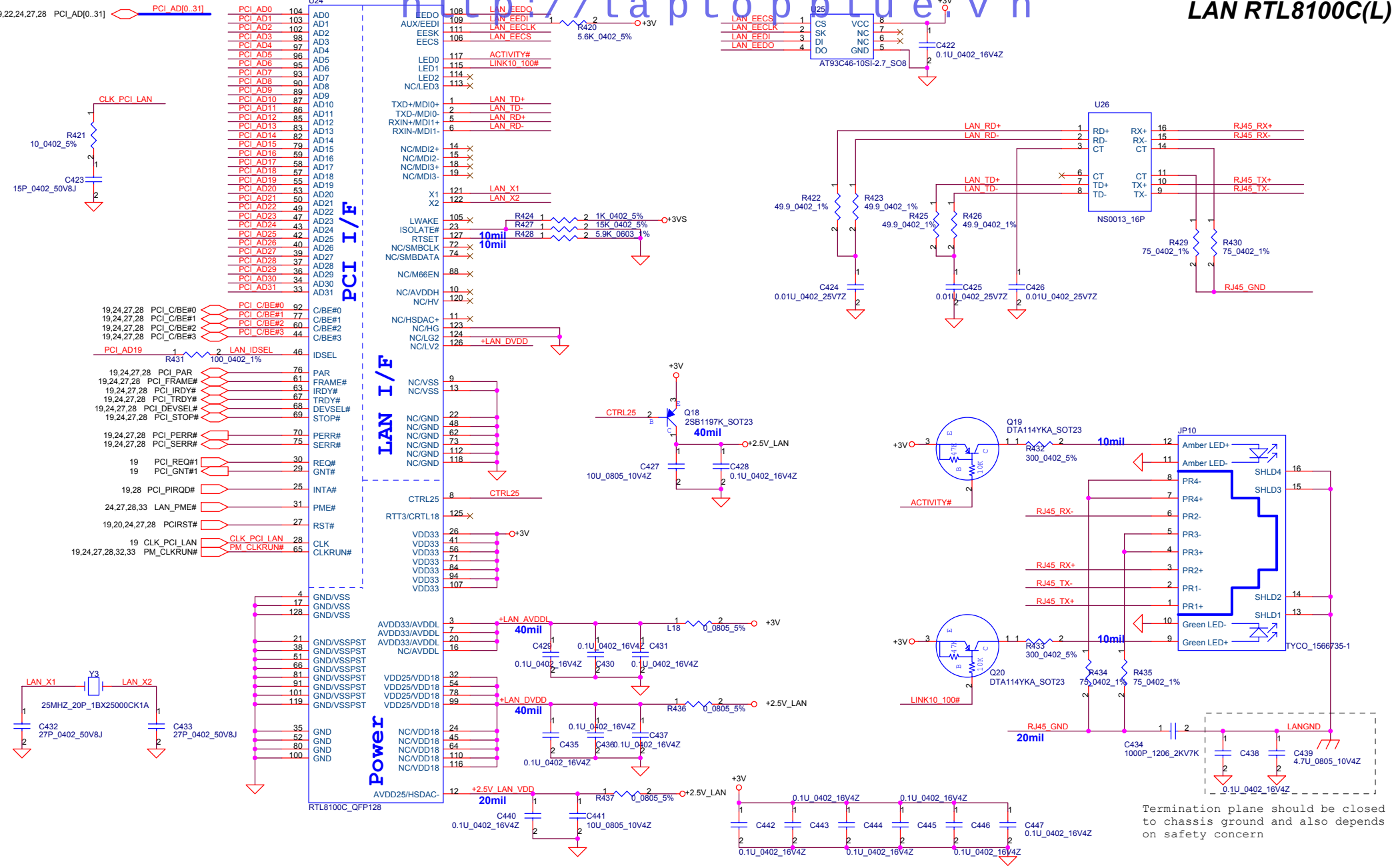
PCMCIA Power Controller

CardBus Socket



Compal Electronics, Inc.		
Title: PCMCIA Socket		
Size: C	Document Number: LA-2301	Rev: 0.2
Date: Thursday, April 08, 2004	Sheet 25 of 47	

LAN RTL8100C(L)

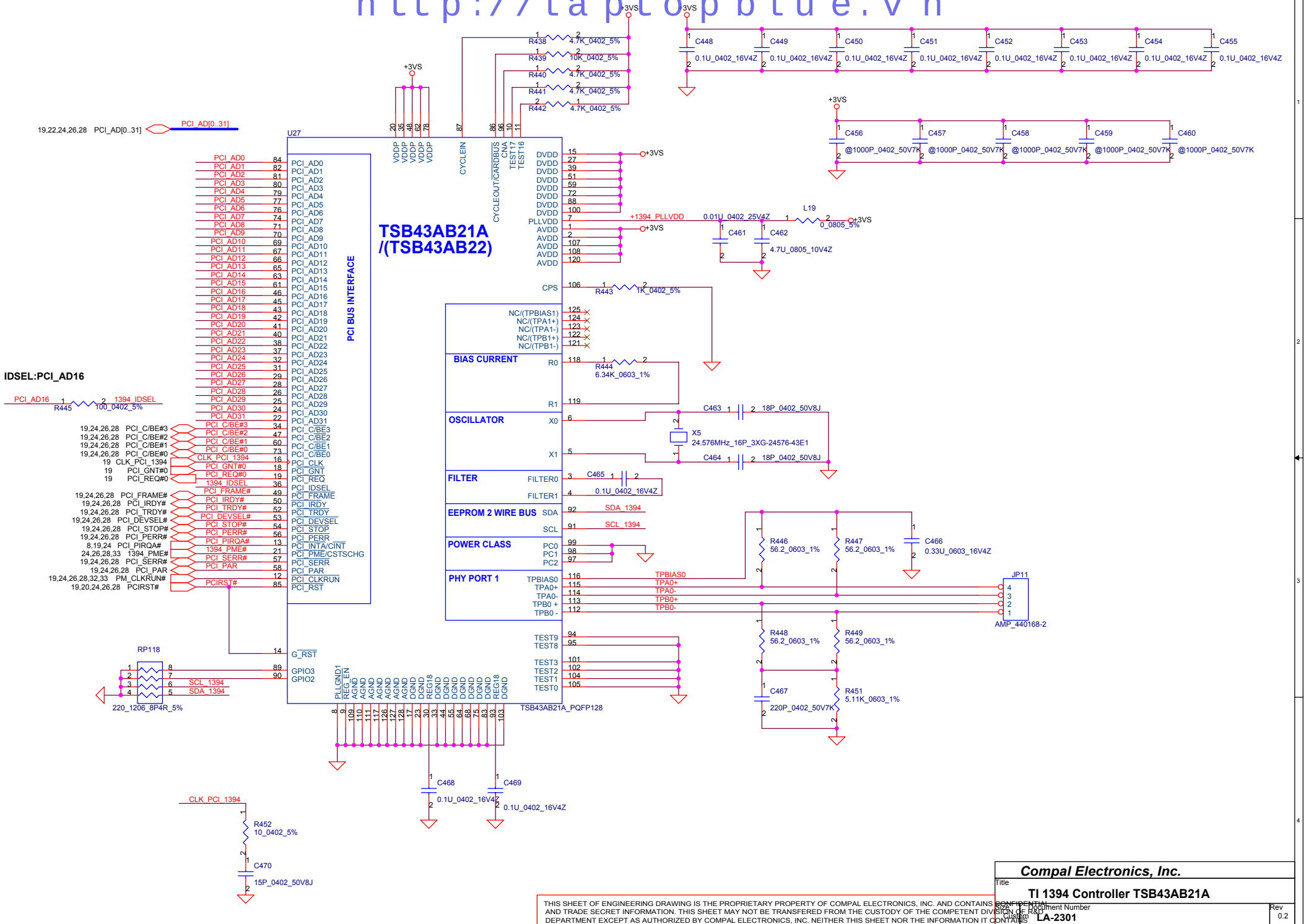


Compal Electronics, Inc.

Title: LAN REALTEK RTL8100CL

Size: C | Document Number: LA-2301 | Rev: 0.2

Date: Thursday, April 08, 2004 | Sheet 26 of 47



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Compal Electronics, Inc.

Title	TI 1394 Controller TSB43AB21A		
Size	Document Number		Rev
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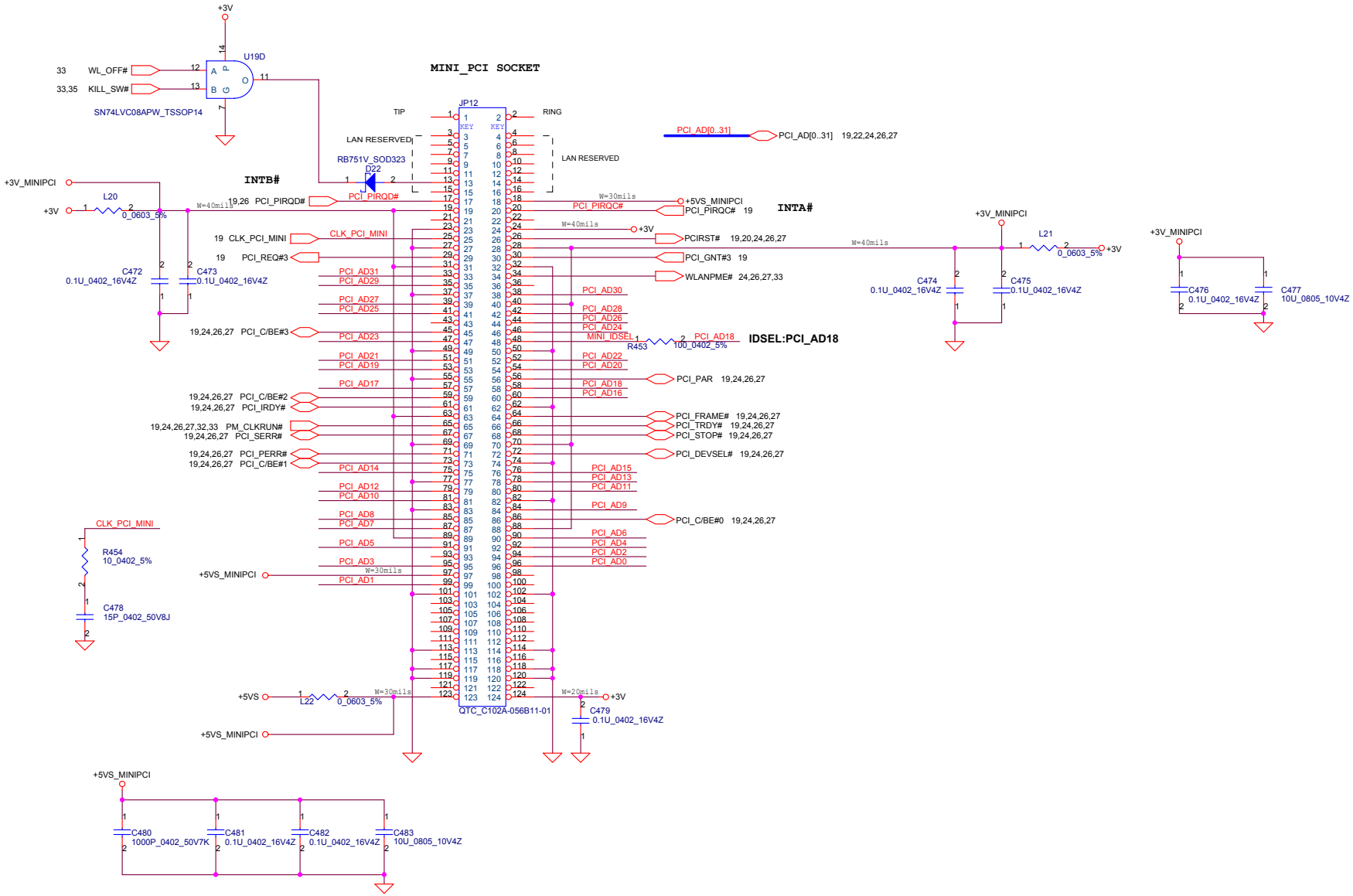
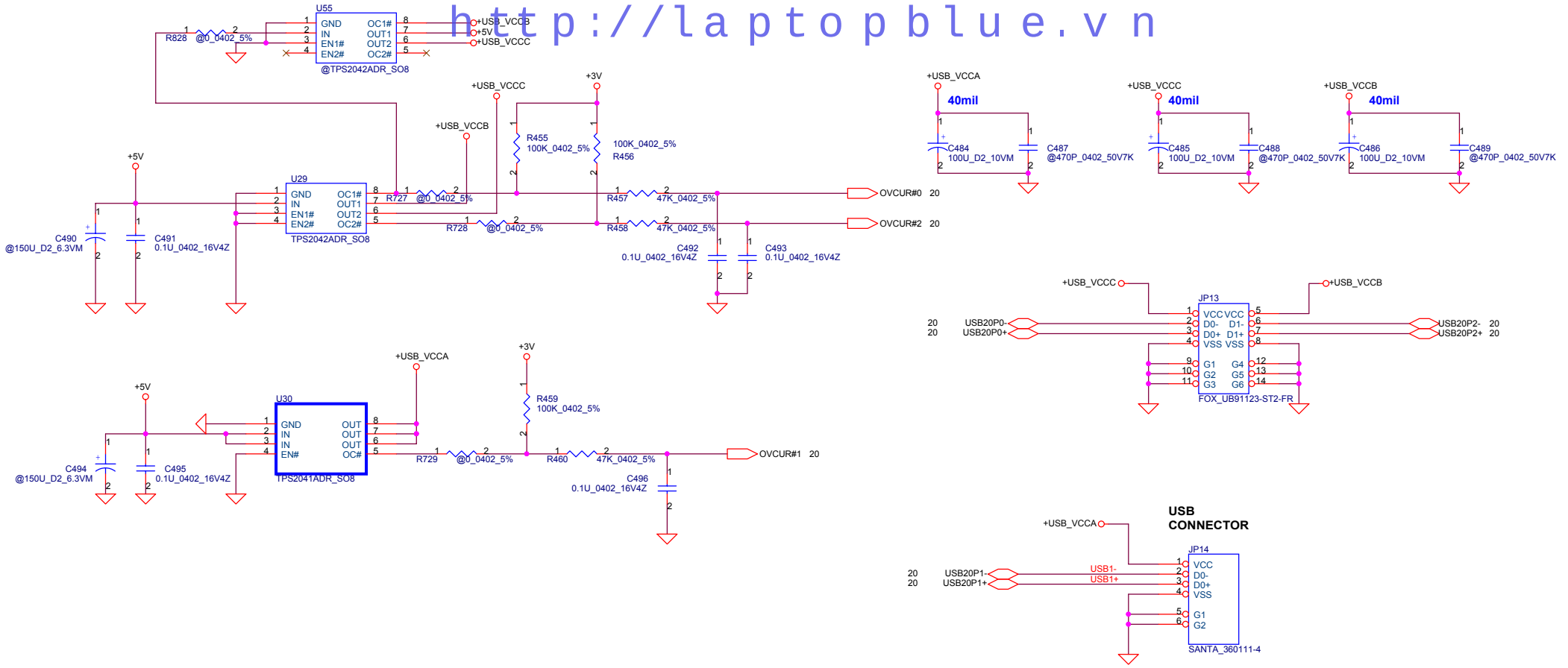
Date:	Thursday, April 08, 2004	Sheet 27 of 47	



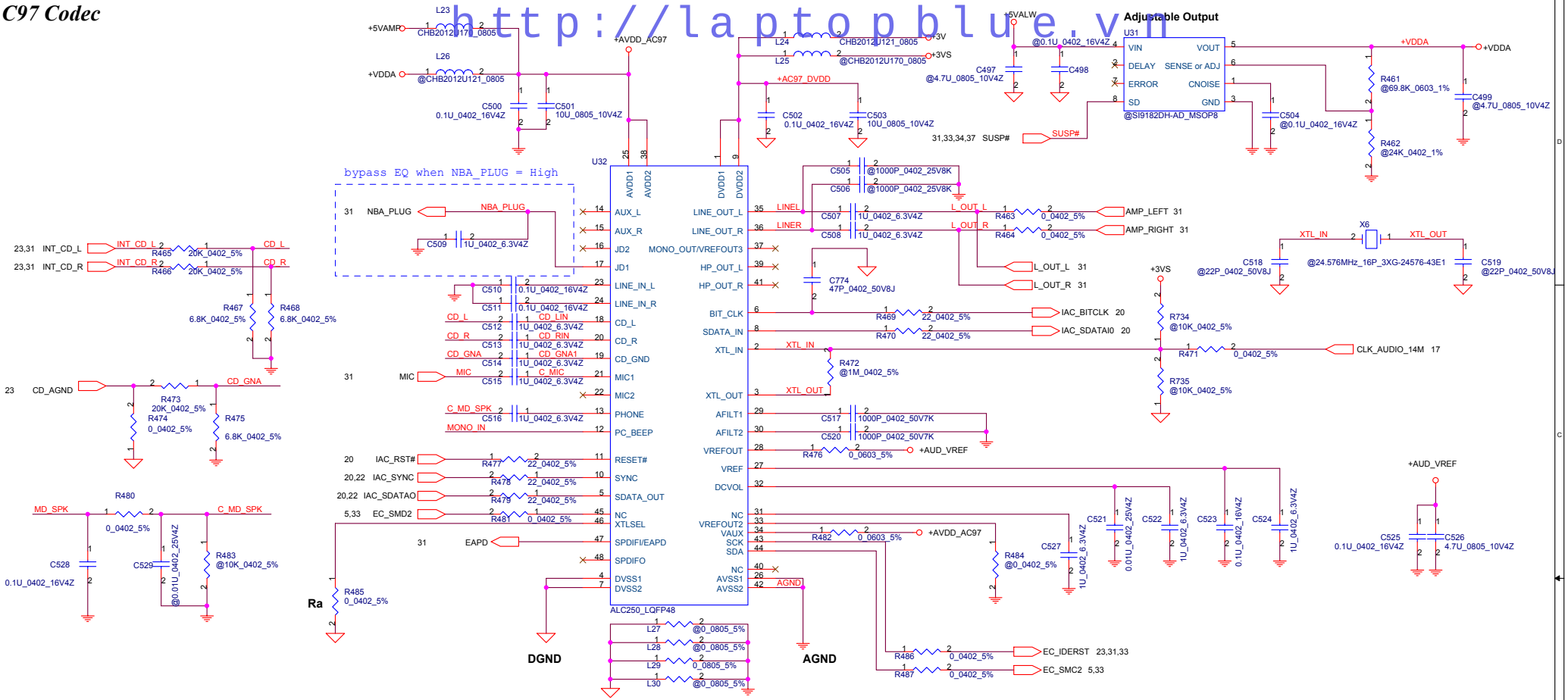
Compal Electronics, Ltd.

Title	Mini PCI Slot	
Size	Document Number	Rev
	LA-2301	0.2
Date:	Thursday, April 08, 2004	Sheet 28 of 47

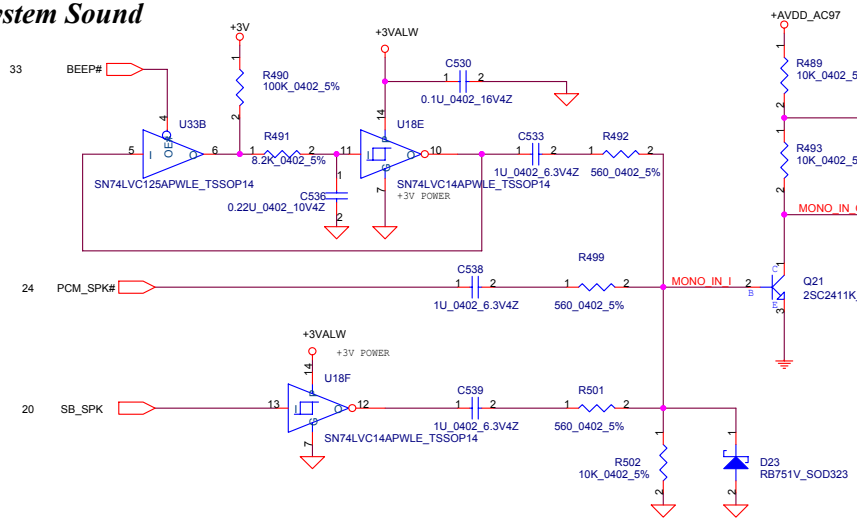


Compal Electronics, Inc.		
Title: USB/PCI-Debug		
Size: E	Document Number: LA-2301	Rev: 0.2
Date: Thursday, April 08, 2004	Sheet 29 of 47	

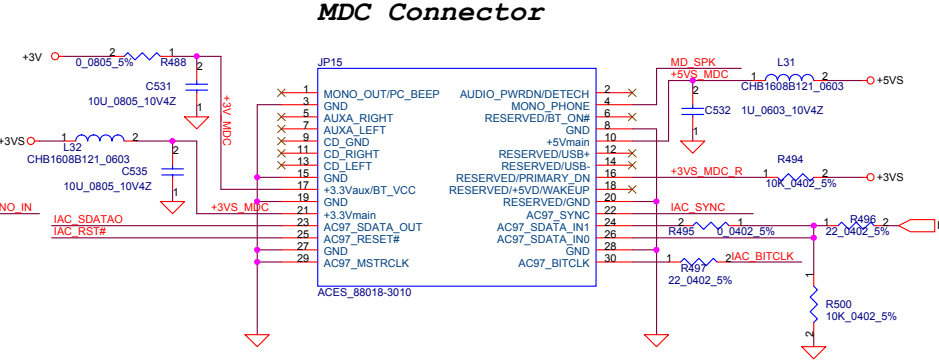
AC97 Codec



System Sound



MDC Connector



Compal Electronics, Ltd.		
Title: AC97 Codec ALC250		
Size:	Document Number: LA-2301	Rev: 0.2
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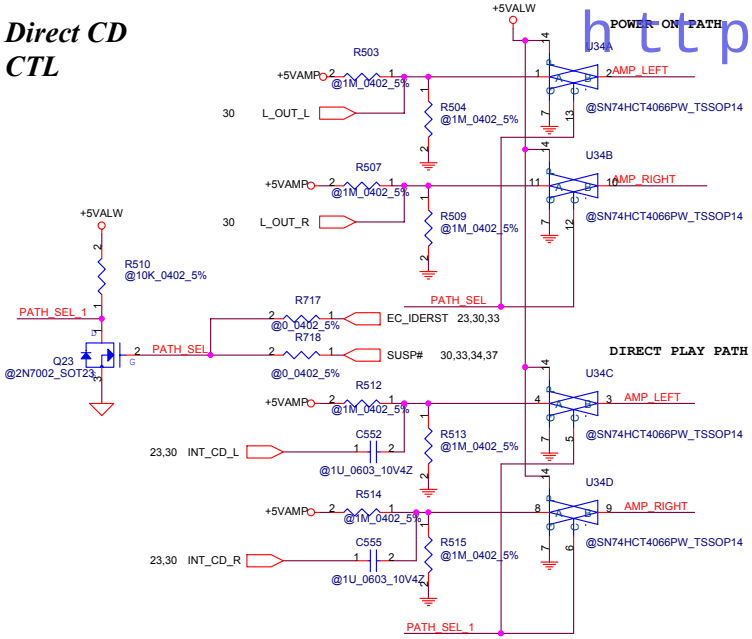
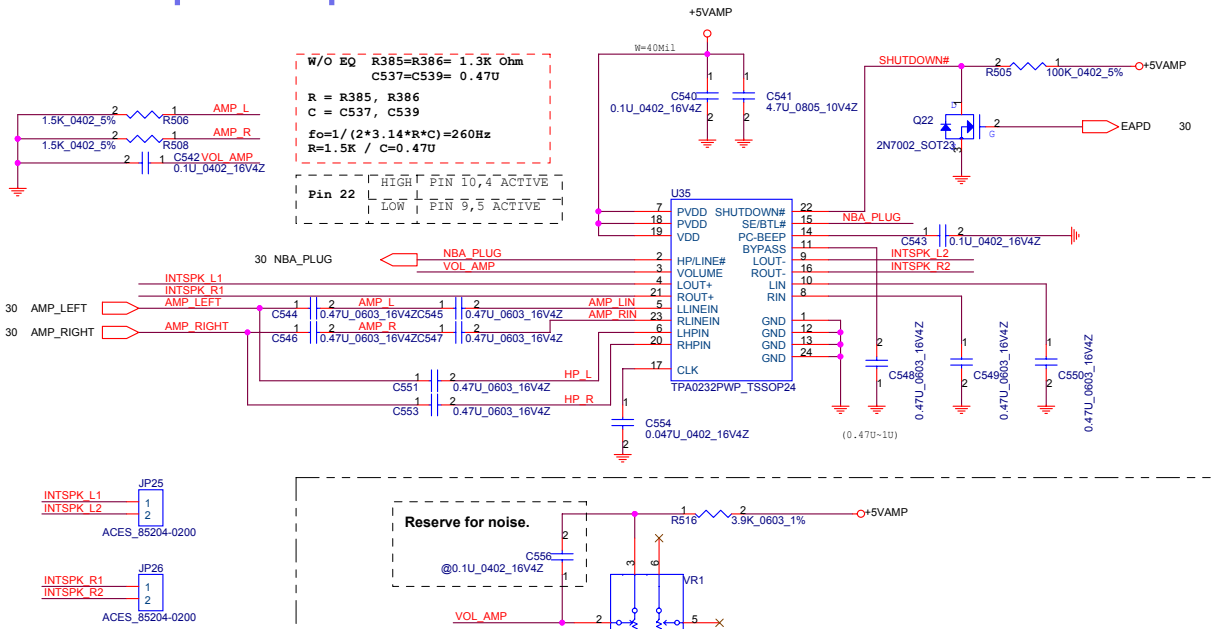
Direct CD CTL

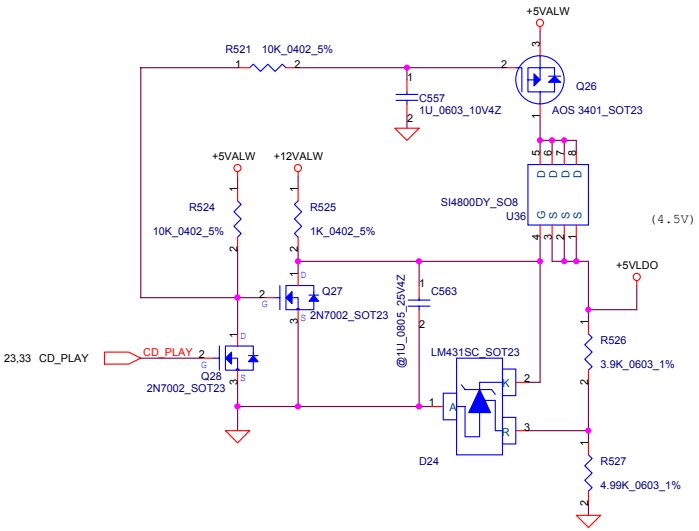


Audio AMP

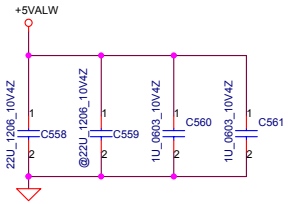


Regulator for AMP

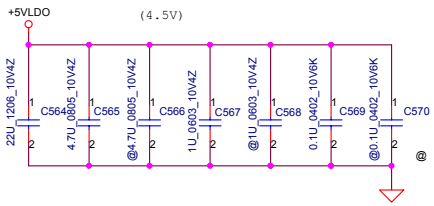
+5VALW TO +5VLDO



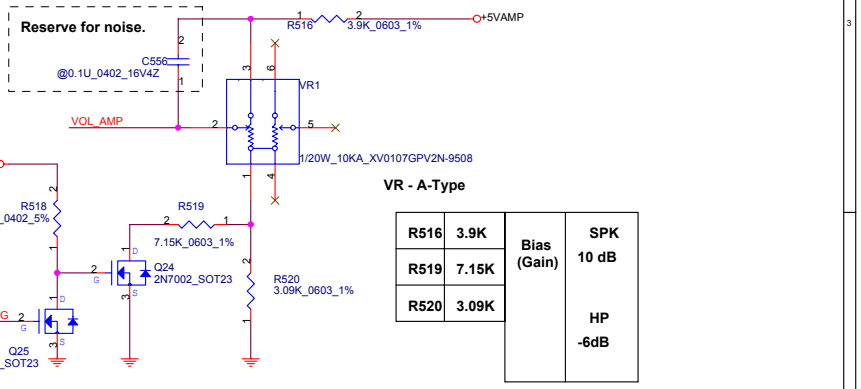
+5VALW DECOUPLING



+5VAMP DECOUPLING

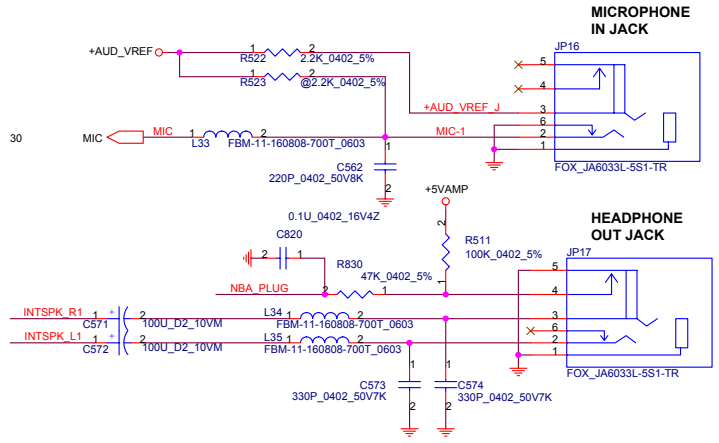


+5VALW TO +5VLDO



VR - A-Type

R516	3.9K	Bias (Gain)	SPK 10 dB
R519	7.15K		
R520	3.09K		HP -6dB



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Title: Audio AMP & JACK

Size: Custom | Document Number: LA-2301 | Rev: 0.2

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SUPER I/O SMsC LPC47N217

U37
LPC47N217_STQFP64

Serial Port for Debug

JP18
@E&T_96212-1011S

Parallel Port

FIR Module

L: R POP; FIR Enable
H: R De-POPFIR Disable

SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

Add for EMI

Compal Electronics, Ltd.

Title	LPC-Super I/O	
Size	Document Number	Rev
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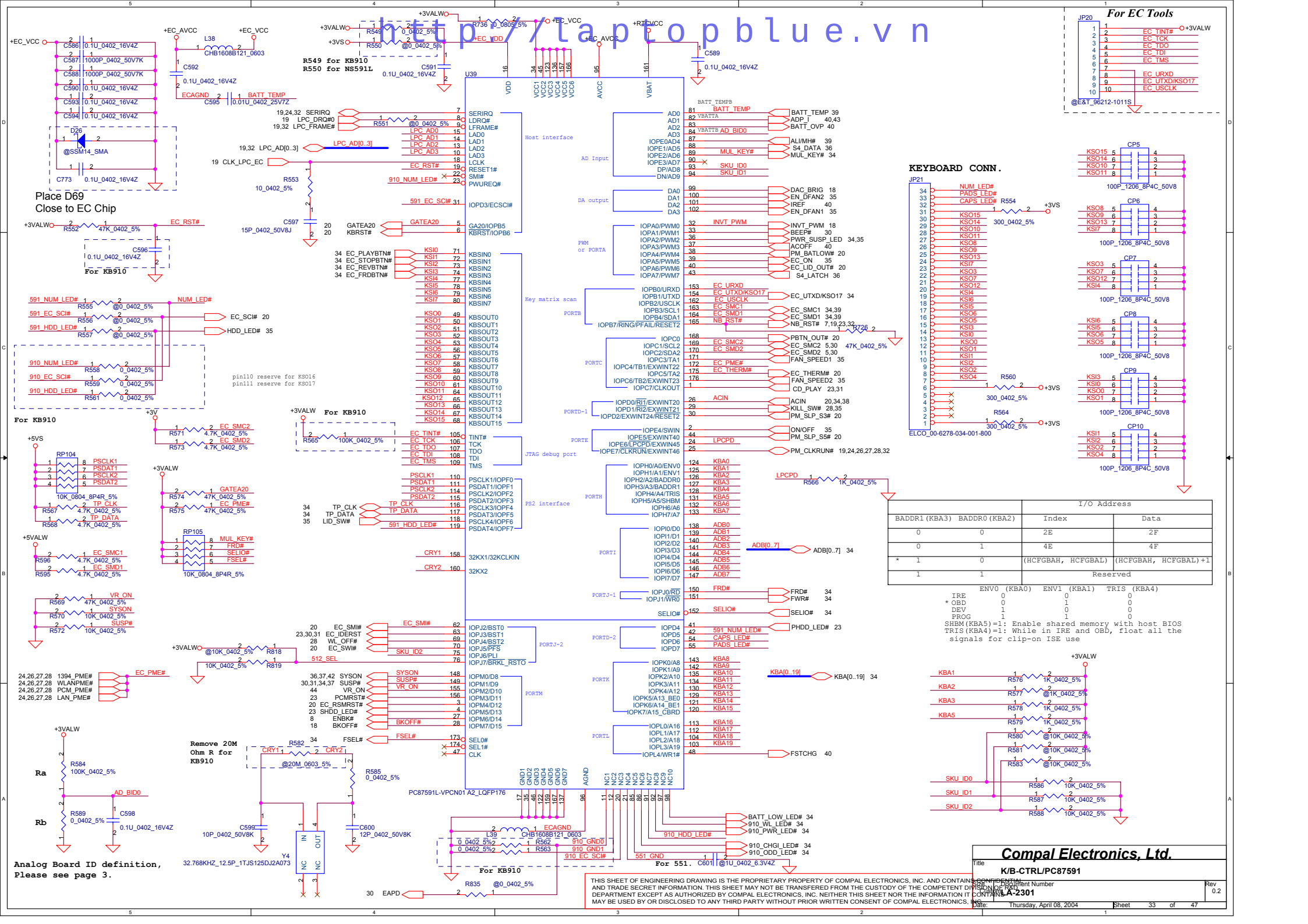
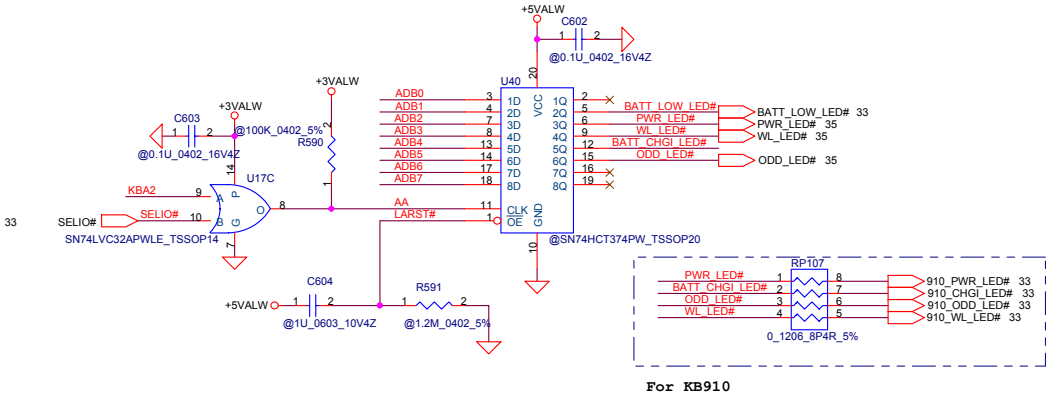
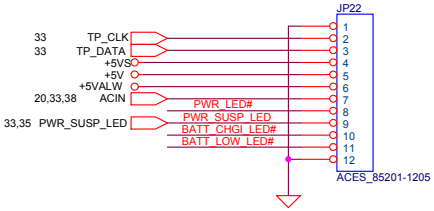


Extension IO

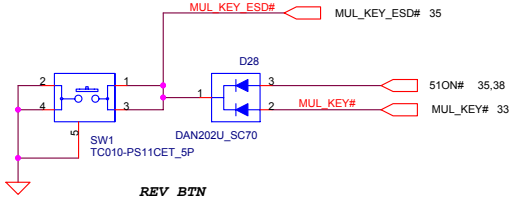


For KB910

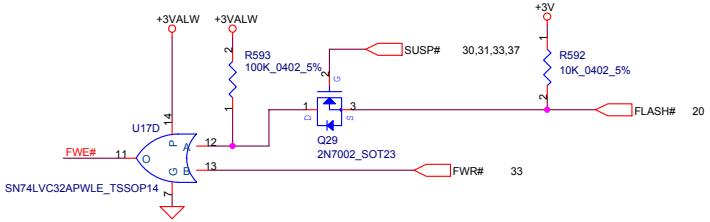
Touch Pad Connector



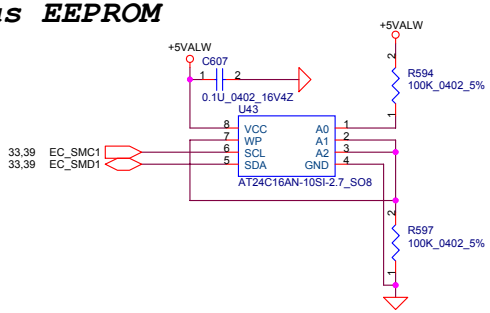
For MP3 / BUTTON LOCK / CD-PLAY



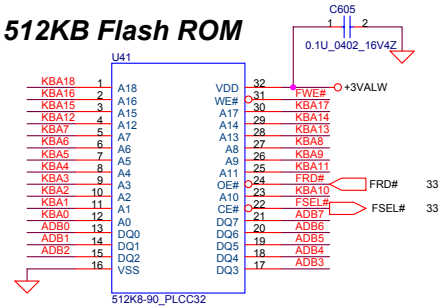
System BIOS



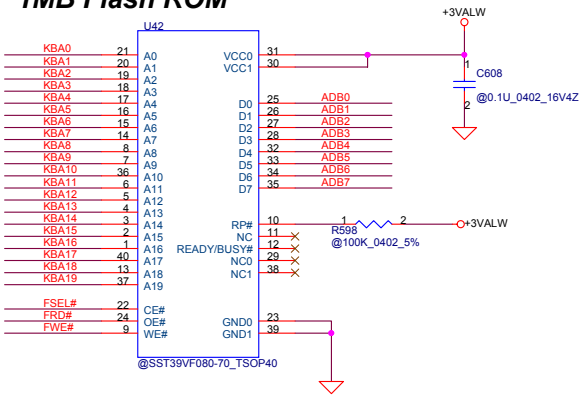
SMBus EEPROM



512KB Flash ROM



1MB Flash ROM

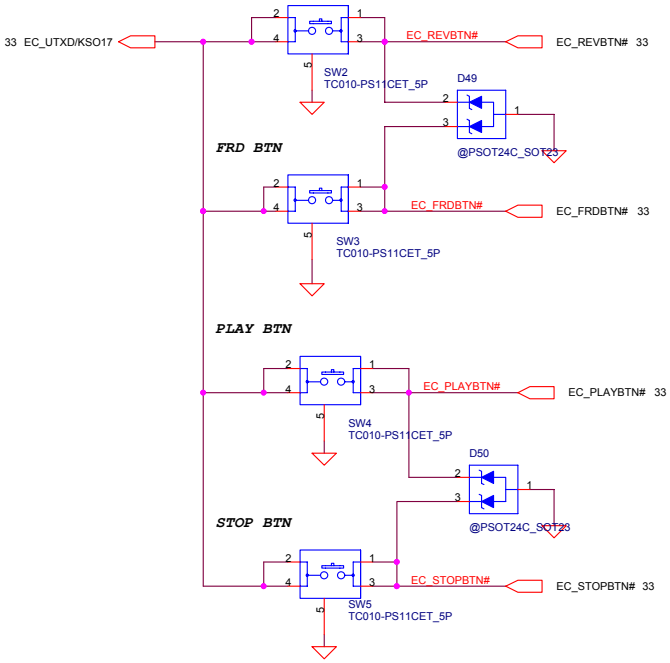


REV BTN

FRD BTN

PLAY BTN

STOP BTN



Compal Electronics, Ltd.

Title: BIOS & Ext.I/O

Size: A3 | Document Number: LA-2301 | Rev: 0.2

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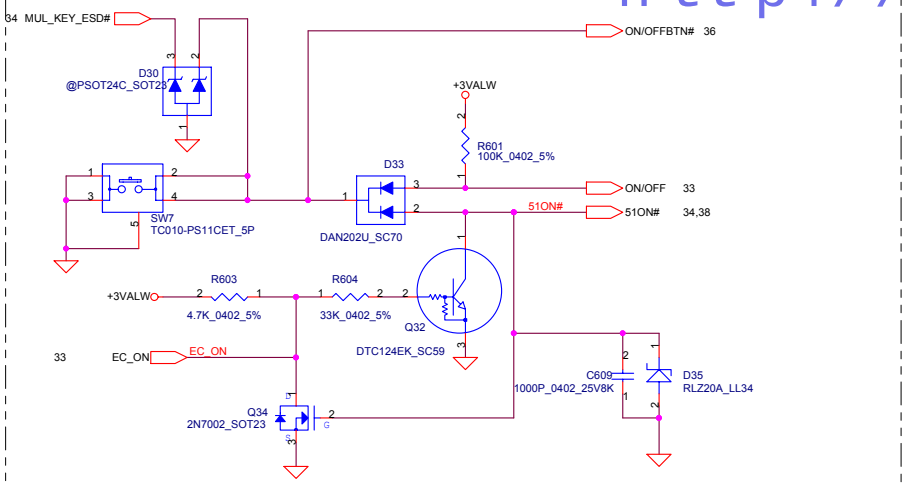
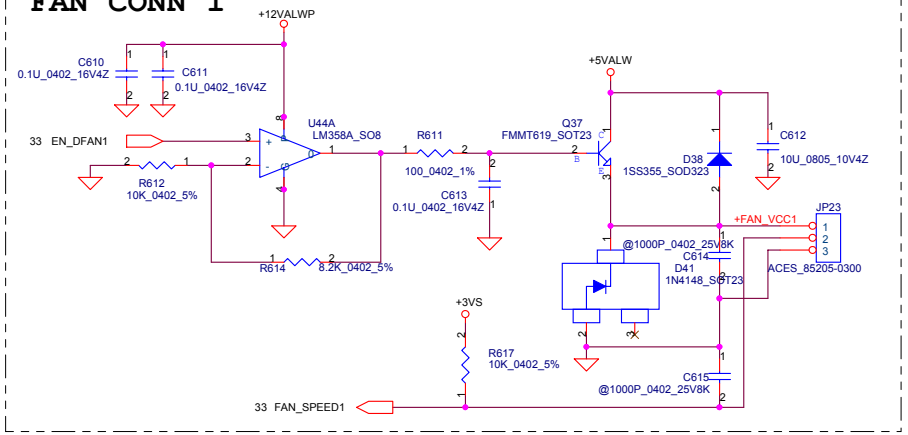
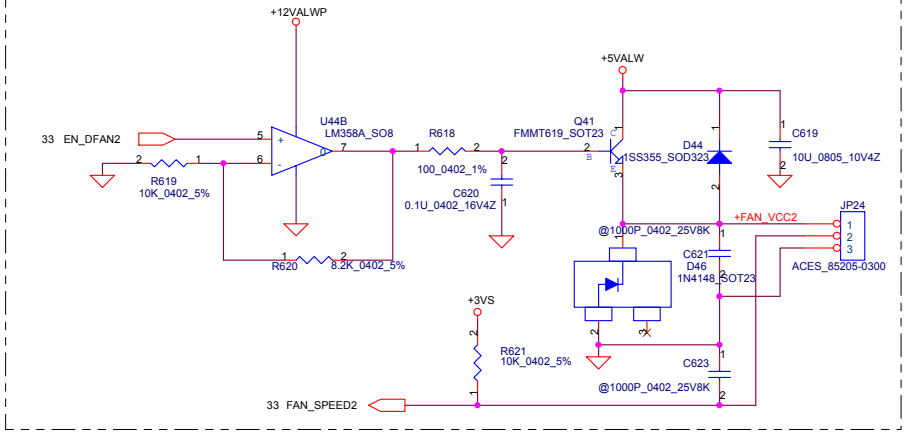
Power Button



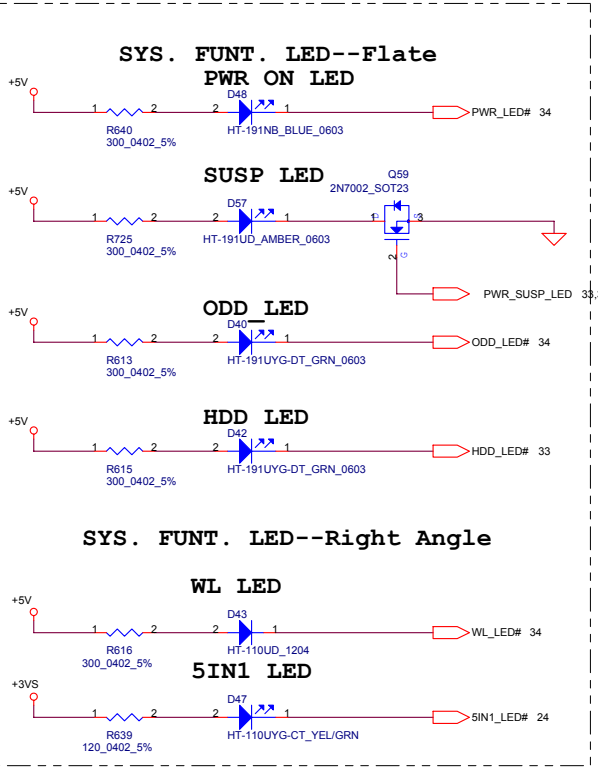
FAN CONN 1



FAN CONN 2

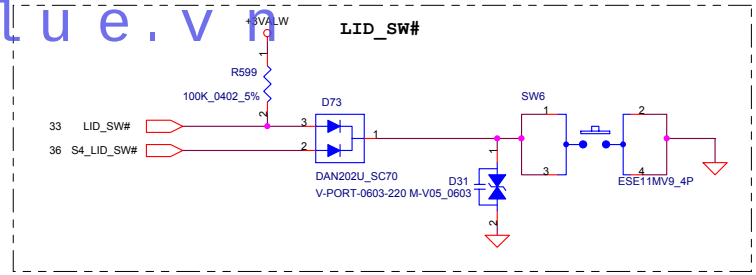


SYS. FUNT. LED--Flate

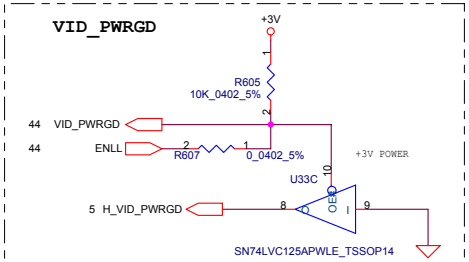


SYS. FUNT. LED--Right Angle

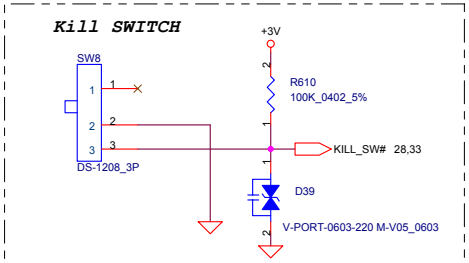
LID_SW#



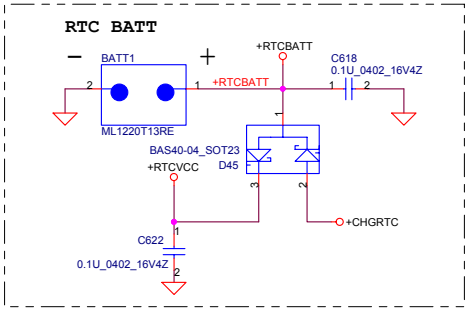
VID_PWRGD



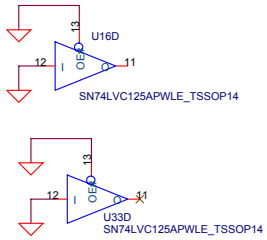
Kill SWITCH



RTC BATT



Compal Electronics, Ltd.	
Title	PWRGD/Fan/PWRBTN/TP/LID.
Size	Document Number: LA-2301
Rev	0.2
Date: Thursday, April 08, 2004	Sheet 35 of 47



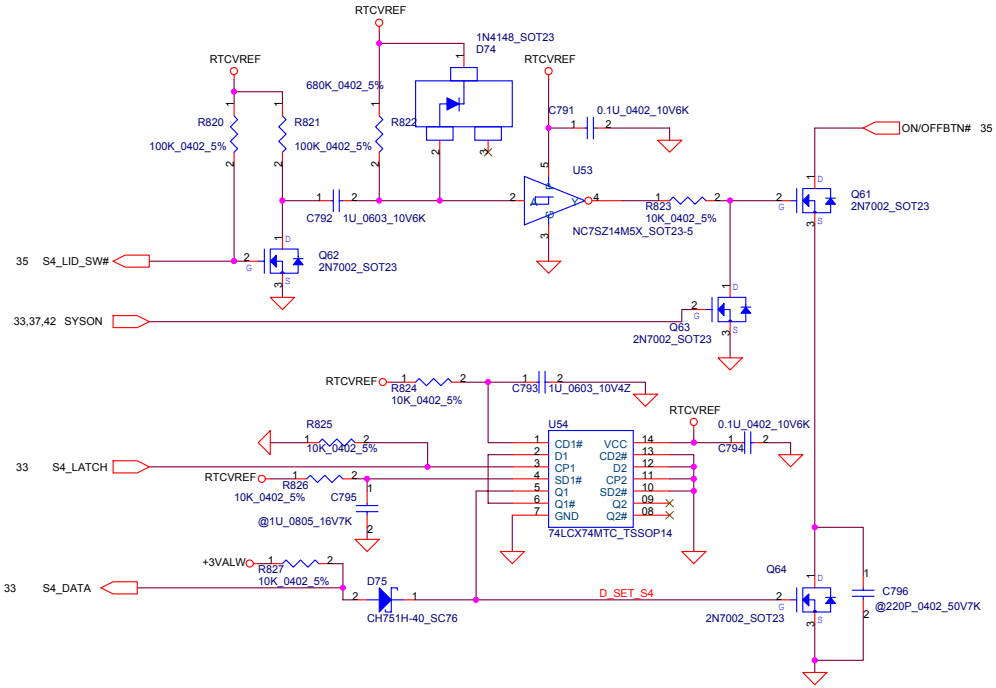
H20 H_S315D110 · H23 H_S315D110 · H21 H_S315D110 · H22 H_S315D110
H1 H_C394D177 · H4 H_C394D177 · H2 H_C394D177 · H3 H_C394D177
H24 H_S315D110 · H27 H_S315D110 · H25 H_S315D110 · H26 H_S315D110
H5 H_C315D91 · H8 H_C315D91 · H6 H_C315D91 · H7 H_C315D91
H28 H_S394D110 · H29 H_S394D110 · H33 H_C146D63
H9 H_C315D181 · H10 H_C315D181 · H11 H_C315D169
H34 H_C315D169 · H36 H_S394D110
H19 H_O224X146D146X67 · H32 H_S354D181 · H18 H_C276D169

FD1 FIDUCAL · FD2 FIDUCAL · FD3 FIDUCAL
FD4 FIDUCAL · FD5 FIDUCAL · FD6 FIDUCAL

CF1 SMD40M80 · CF2 SMD40M80 · CF3 SMD40M80 · CF4 SMD40M80 · CF5 SMD40M80 · CF6 SMD40M80
CF7 SMD40M80 · CF8 SMD40M80 · CF9 SMD40M80 · CF10 SMD40M80 · CF11 SMD40M80 · CF12 SMD40M80
CF13 SMD40M80 · CF14 SMD40M80

M1 H_O201X148D201X148N · M2 H_C79D79N · M3 H_O118X79D118X79N · M4 H_C148D148N
M5 H_C138D138N

Battery mode Hibernation



Compal Electronics, Ltd.

Title: ScrewHole
Size: Document Number: LA-2301
Rev: 0.2
Date: Thursday, April 08, 2004
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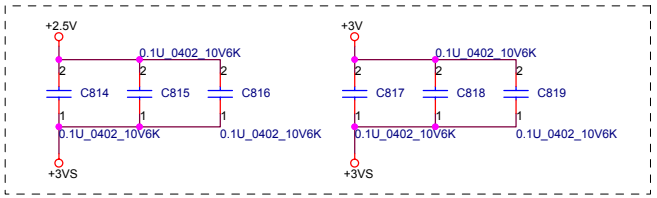
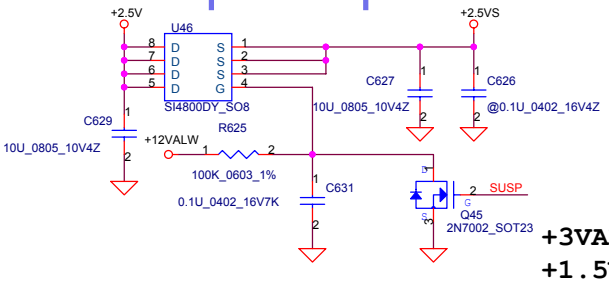
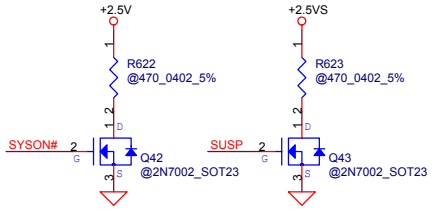
Add for EMI



+2.5V To +2.5VS Transfer

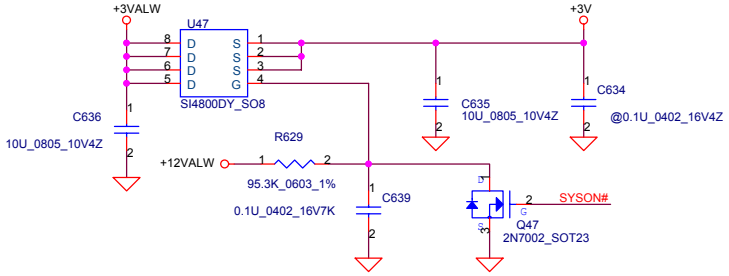


+2.5V & +2.5VS Discharge

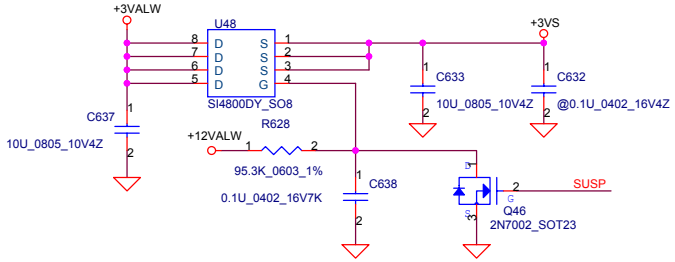


+3VALW AND +2.5VALW MUST RISING SAME TIME
+1.5V MUST DELAY AFTER +2.5V

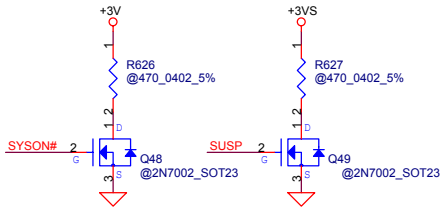
+3VALW To +3V Transfer



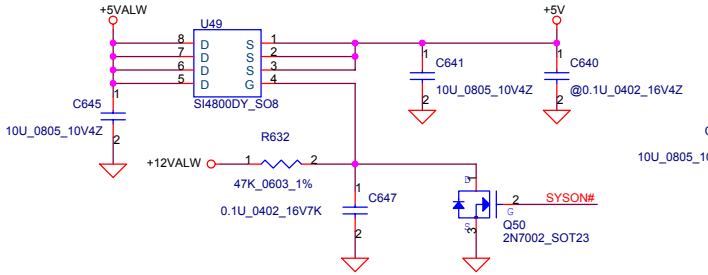
+3VALW To +3VS Transfer



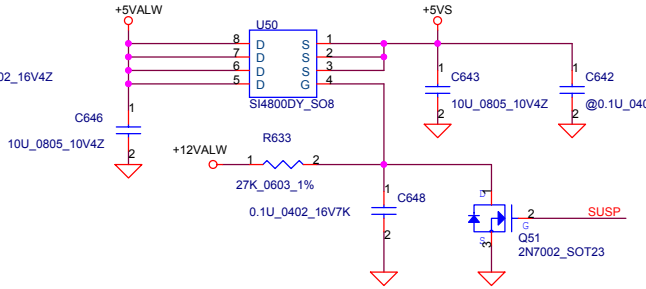
+3V & +3VS Discharge



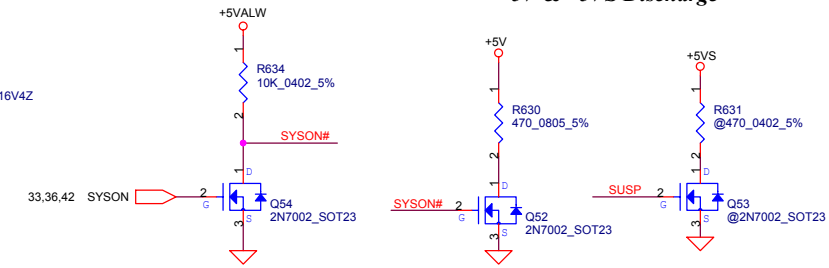
+5VALW To +5V Transfer



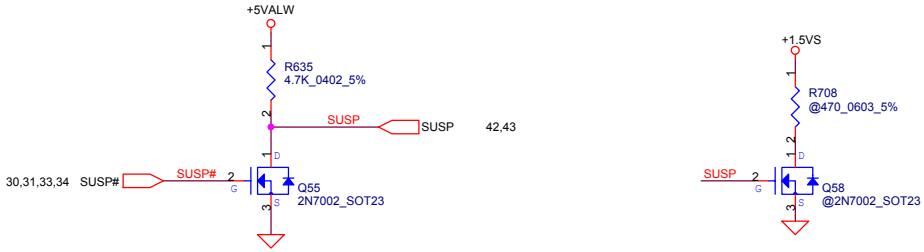
+5VALW To +5VS Transfer



+5V & +5VS Discharge



+1.5VS Discharge



Compal Electronics, Inc.		
Title: DC-DC Circuit Interface		
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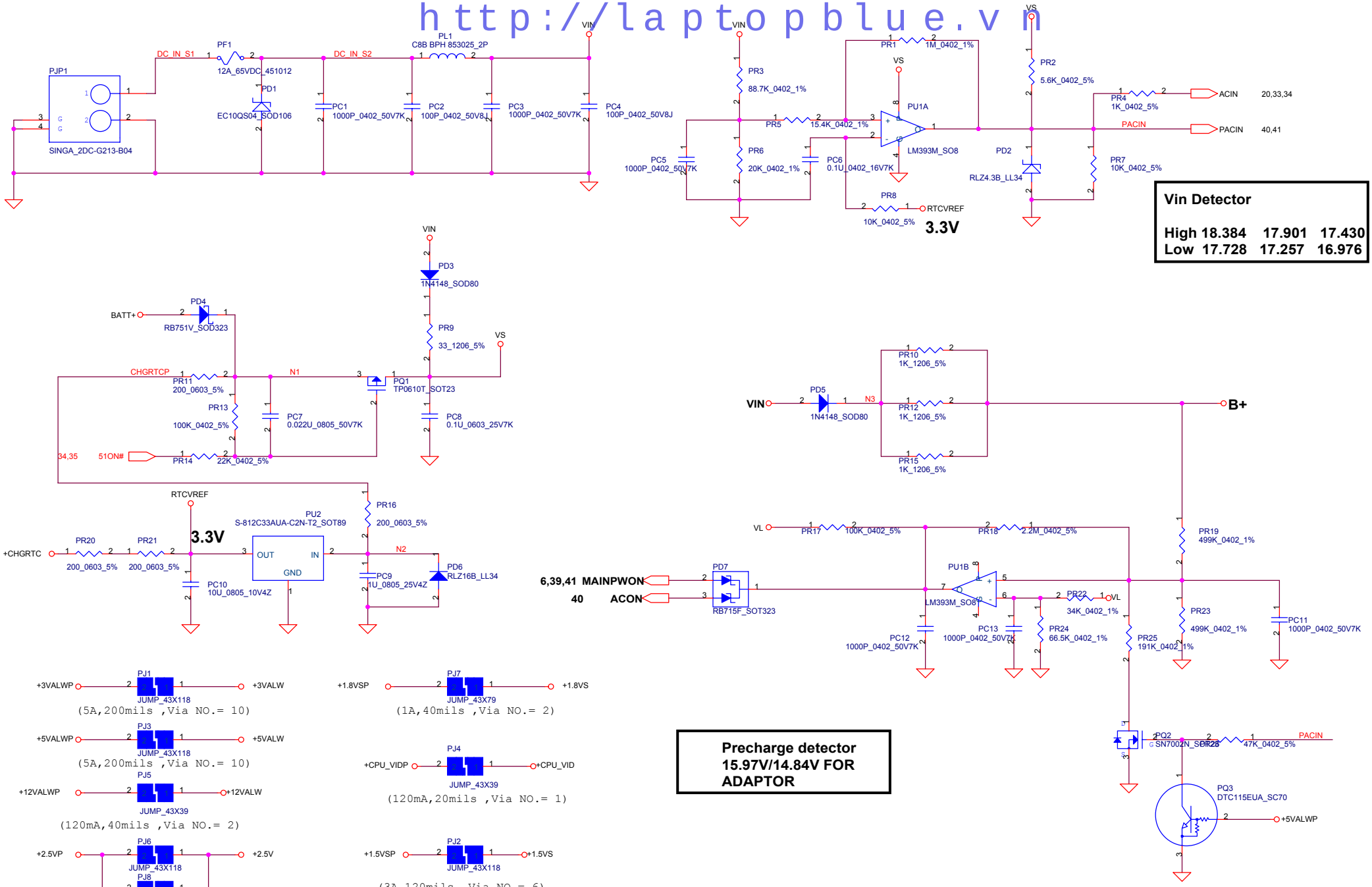

Compal Electronics, Inc.			
Title: DCIN & DETECTOR			
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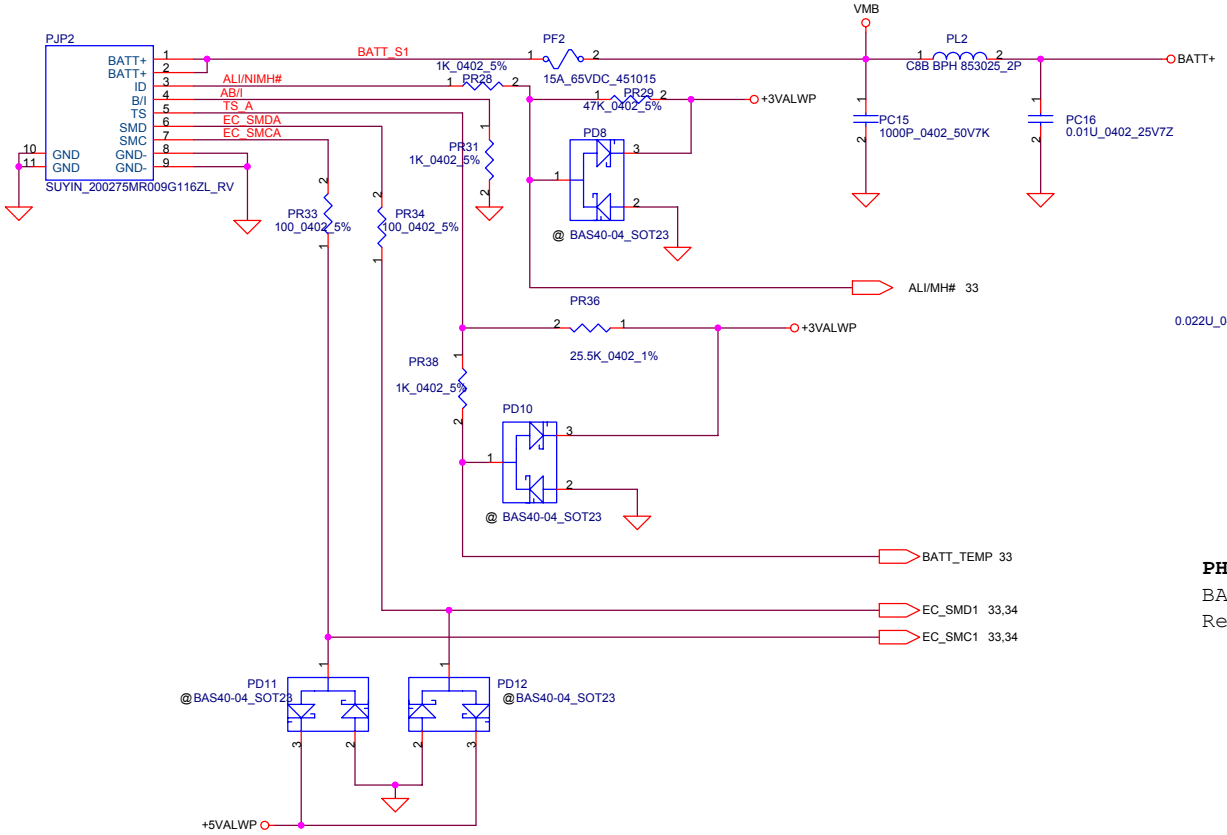
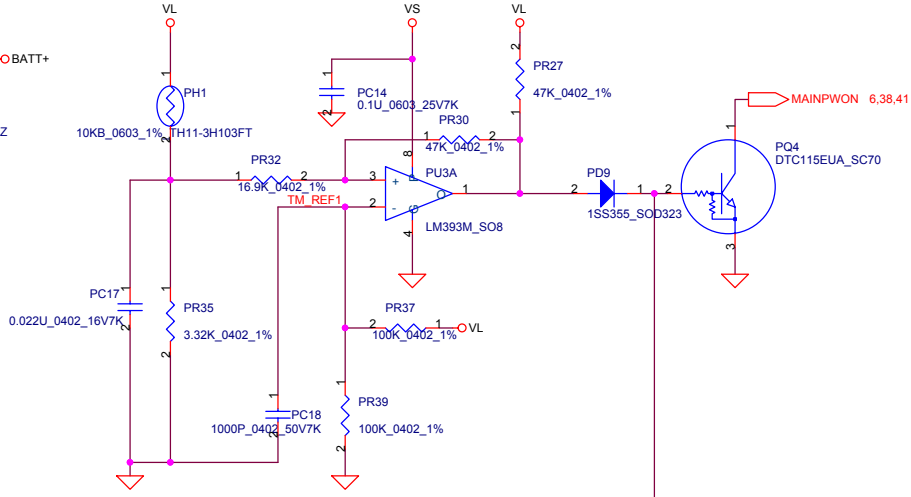
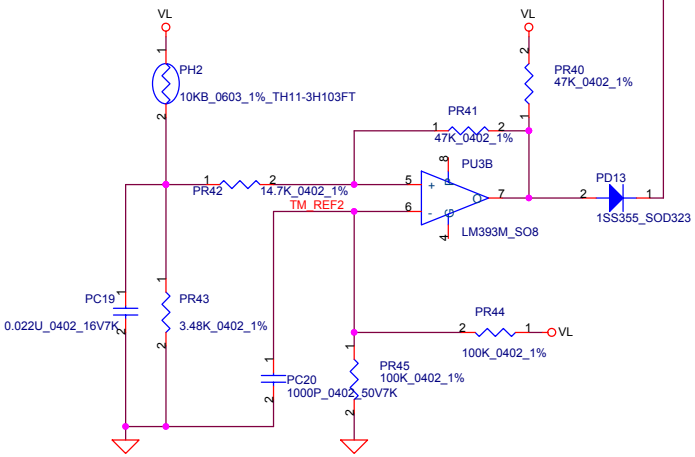
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



Compal Electronics, Inc.		
Title: BATTERY CONN / OTP		
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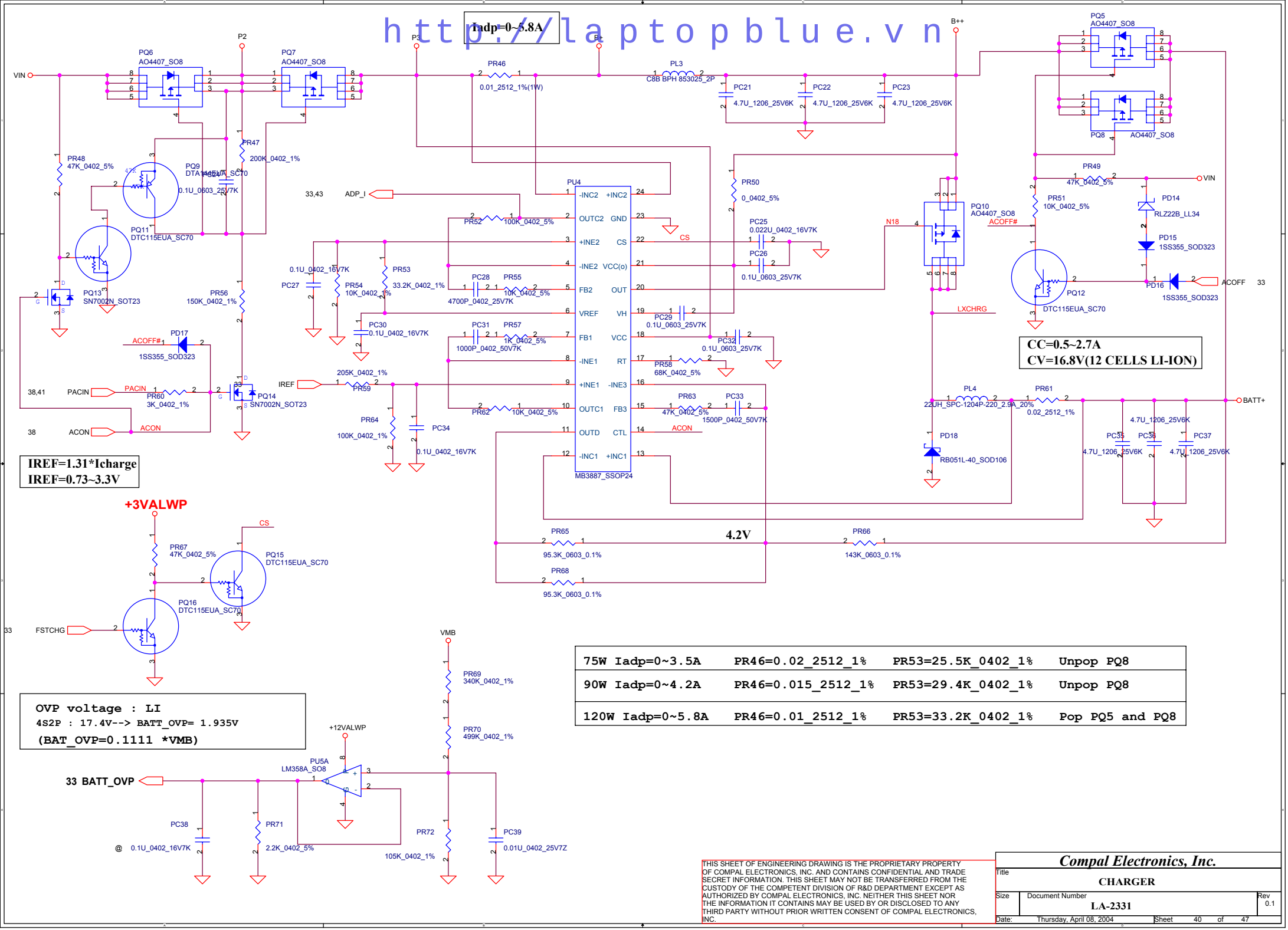

75W Iadp=0~3.5A	PR46=0.02_2512_1%	PR53=25.5K_0402_1%	Unpop PQ8
90W Iadp=0~4.2A	PR46=0.015_2512_1%	PR53=29.4K_0402_1%	Unpop PQ8
120W Iadp=0~5.8A	PR46=0.01_2512_1%	PR53=33.2K_0402_1%	Pop PQ5 and PQ8

Compal Electronics, Inc.
Title: CHARGER
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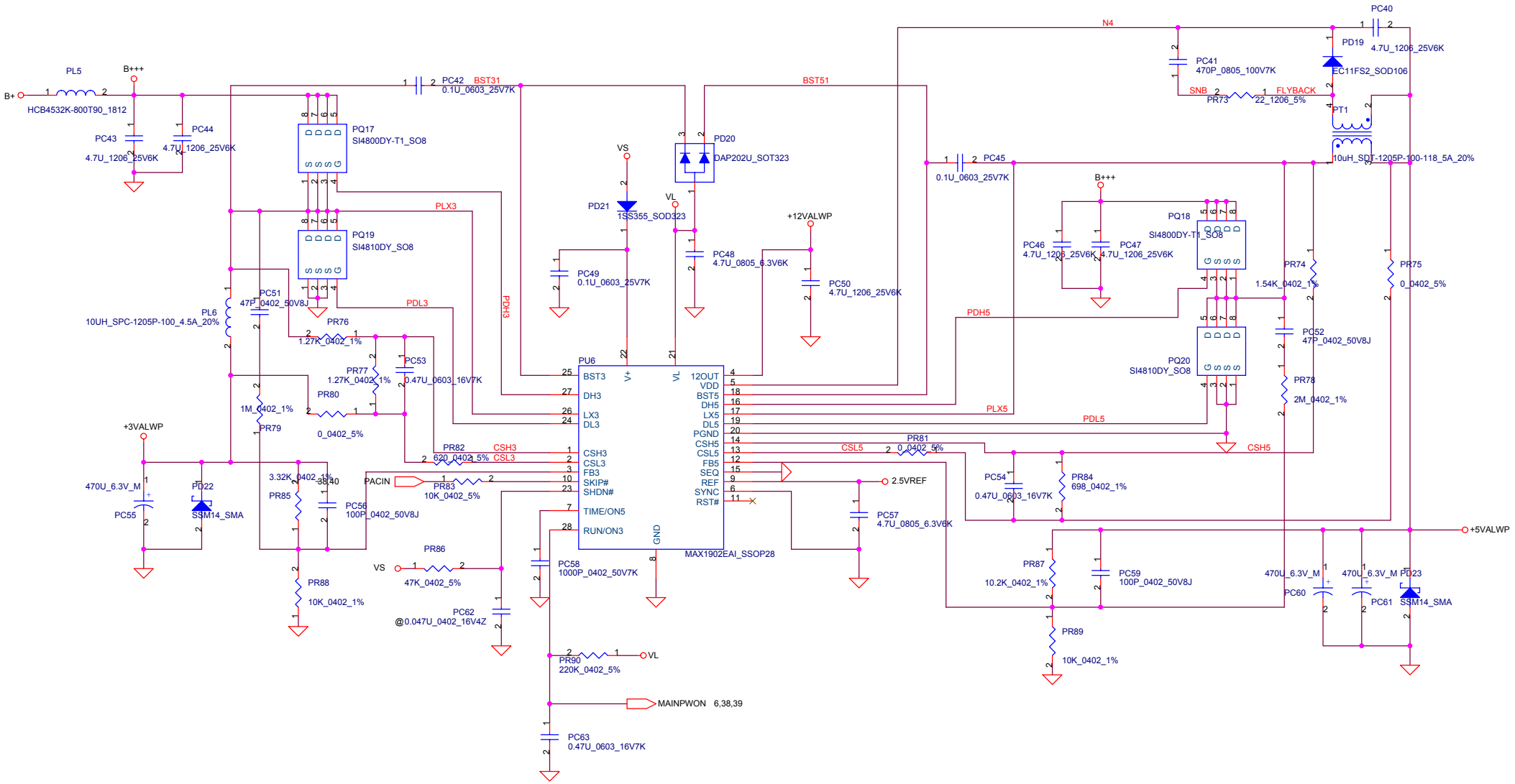

Compal Electronics, Inc.		
Title: 5V/3.3V/12V		
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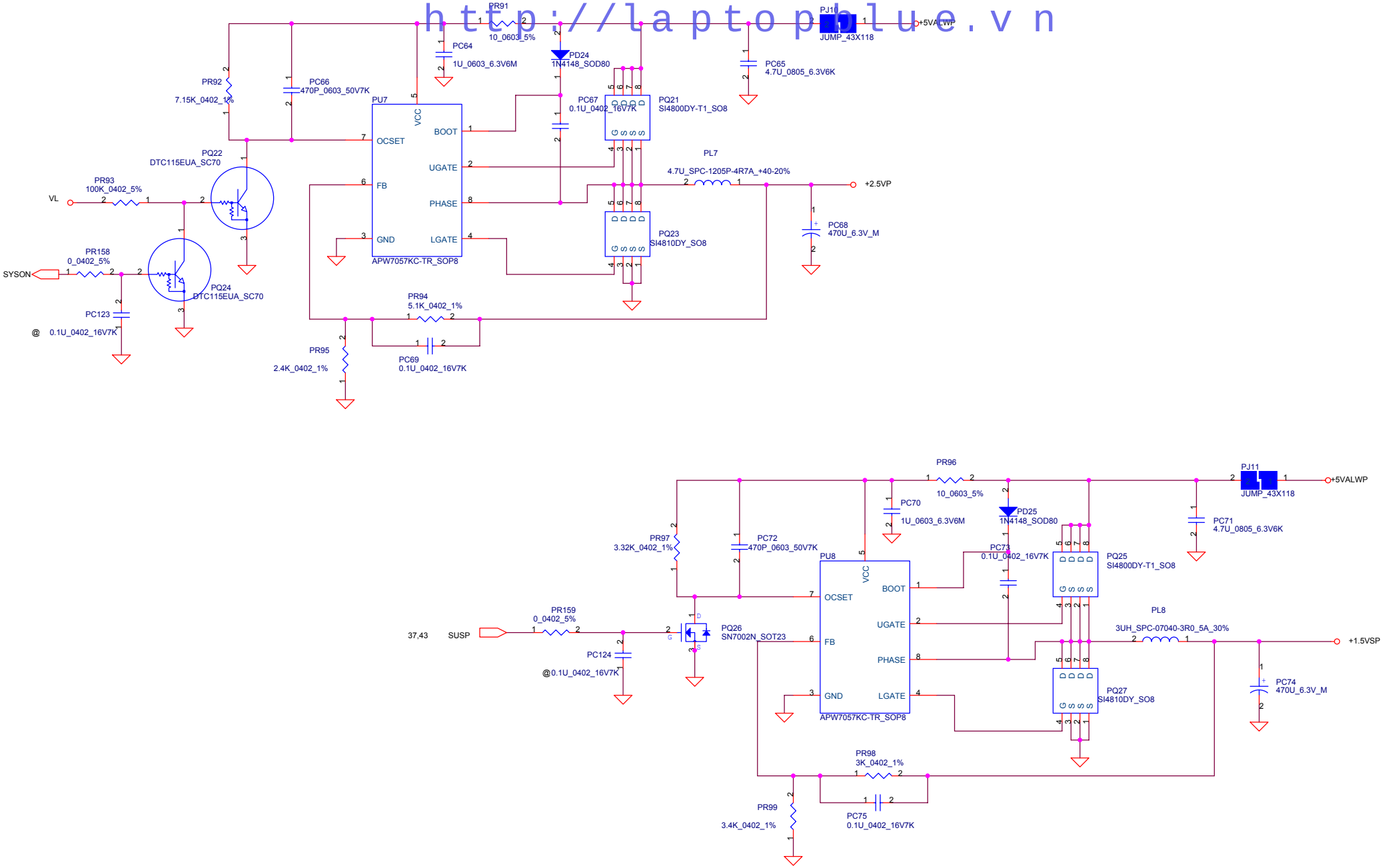

Compal Electronics, Inc.		
Title: 2.5V/1.5V		
Size	Document Number: LA-2331	Rev: 0.1
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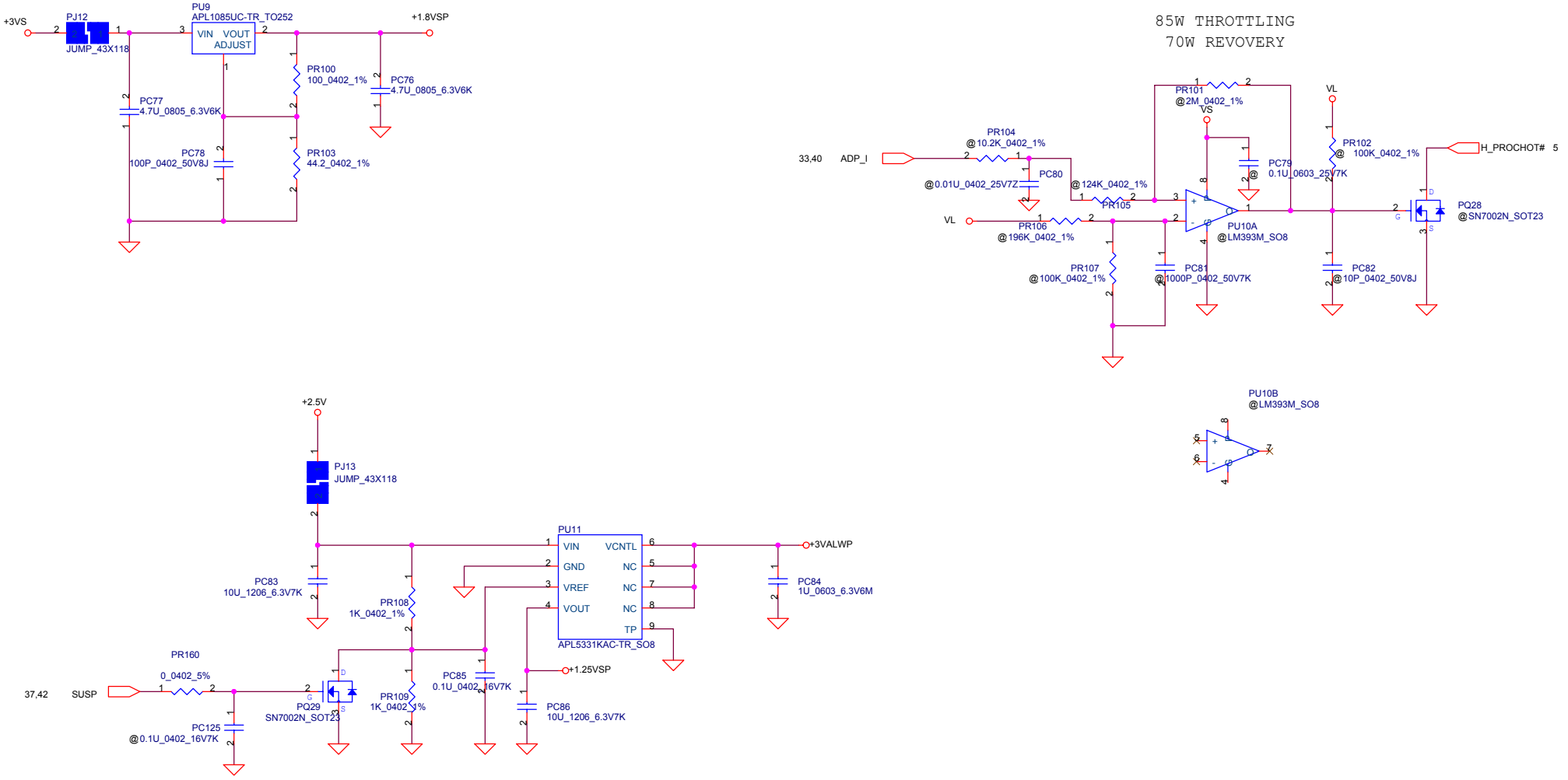

Compal Electronics, Inc.		
Title: 1.8V/1.25V/PROCHOT		
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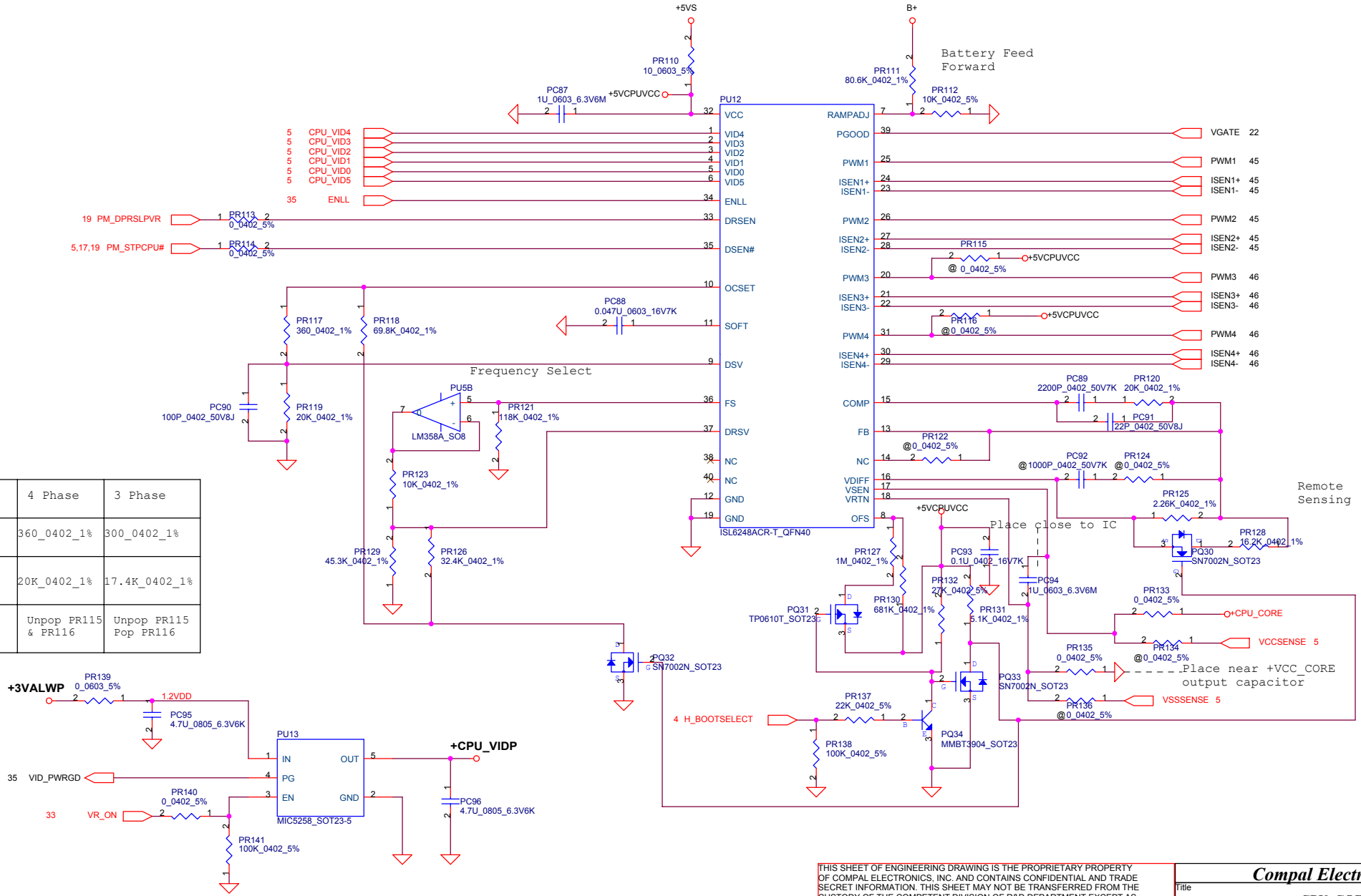

	4 Phase	3 Phase
PR117	360_0402_1%	300_0402_1%
PR119	20K_0402_1%	17.4K_0402_1%
Others	Unpop PR115 & PR116	Unpop PR115 Pop PR116

Compal Electronics, Inc.
Title: CPU_CORE (1)
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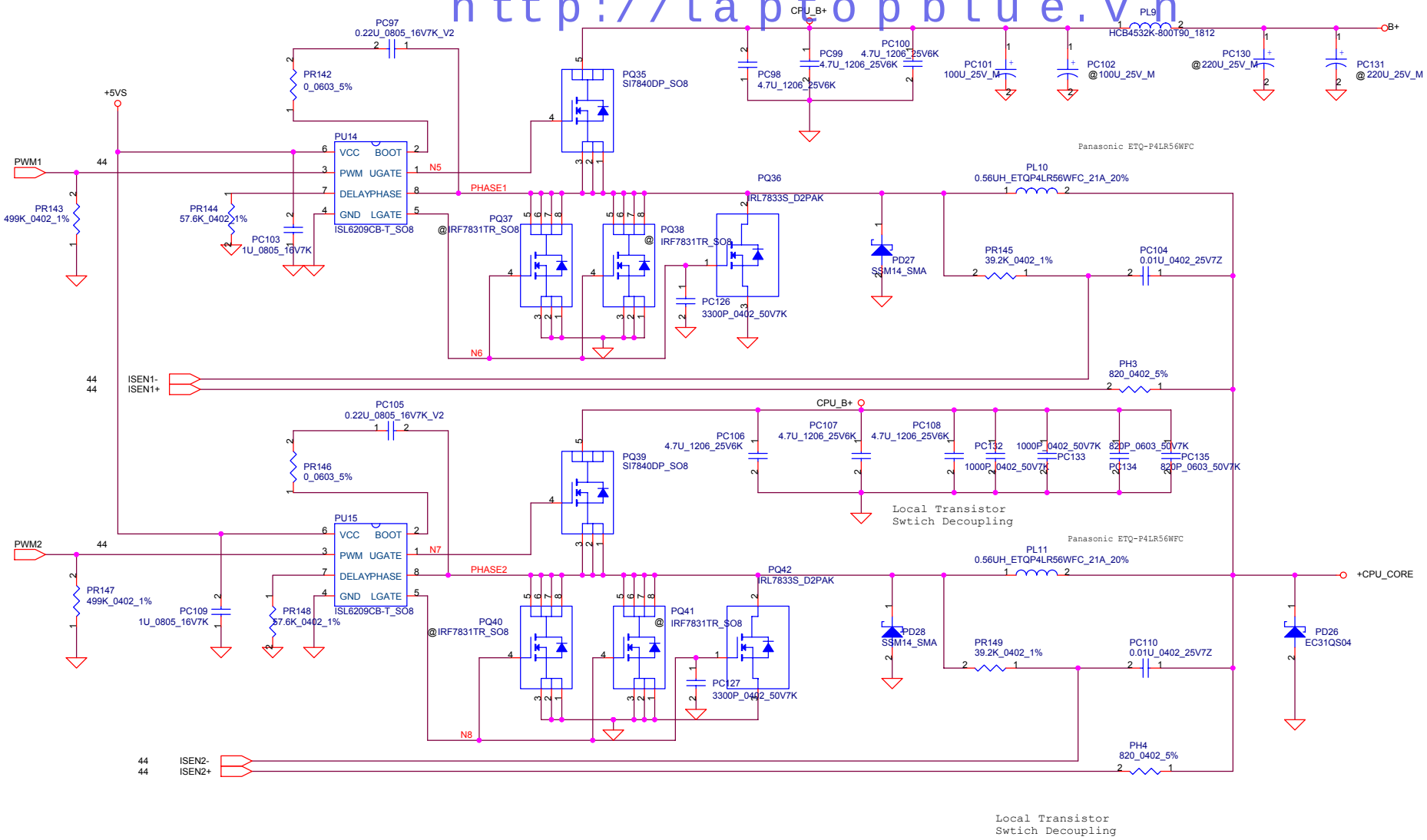

Compal Electronics, Inc.		
Title: CPU_CORE (2)		
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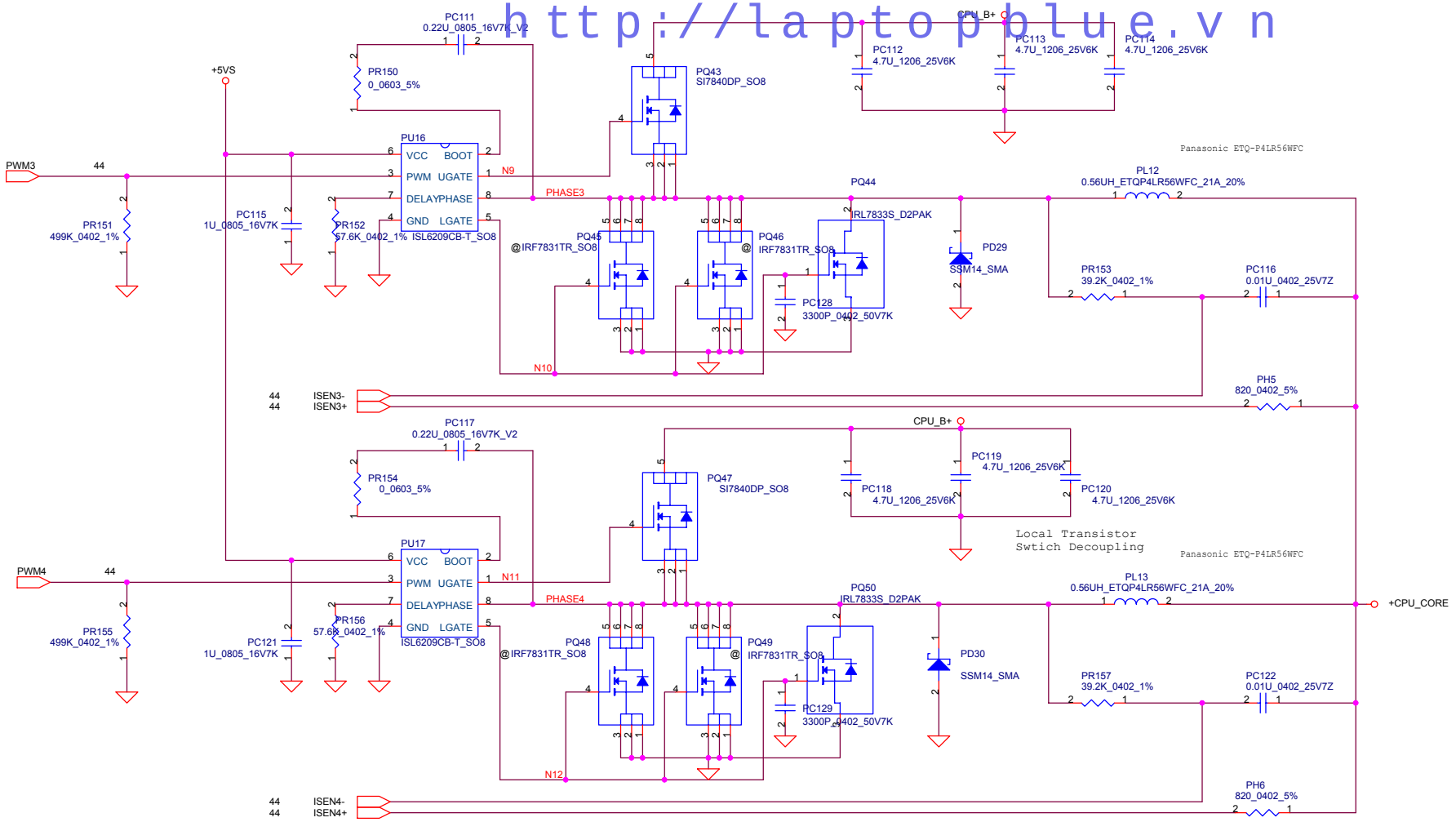

Compal Electronics, Inc.	
Title	CPU_CORE (2)
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Date	Page	Description	Location
03/10	P.14,15	Add 16 Cap in on board DDR chip VDD pin	ADD C775 ~ C790
03/10	P.18	Del L9 & change L8 to bead for EMI	DEL L9 Change L8 to Bead
03/15	P.19	Redefine On board DDR strap pin	DEL R643, R646
03/15	P.21	Change SB +2.5valw power design	DEL R641 ADD Q60,D72
03/15	P.25	Change 5 In 1 connector	Change JP9
03/15	P.32	Add Parallel Port detect strap pin	ADD R817
03/15	P.27	Change 1394 connector footprint	NONE
03/16	P.33	Change EC SMbus2 pull high plwer plan from +5VALW to +3V	NONE
03/16	P.36	Add Battery Hibernation circuit	ADD U54,Q61 ~ Q64,U53,D75,D74,R822,R823 ~ R827,C791, C794,C792, C793,R820,R821
04/5	P.23	Change ODD Conn. layout	
04/5	P.23	Change ODD Conn. layout	

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Title	PIR		
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	LA-2301		0.2
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