

# Sakhir 10, 10C, 10G

## *LA-2491 Schematics Document*

**Intel Dothan / Alviso GM(PM) / DDR-1 / ICH6-M / Fix Bay  
(nVIDIA NV43M / NV44M / ATi M22 / M24)**

**2004 / 11 / 28**

**Rev:1.0**

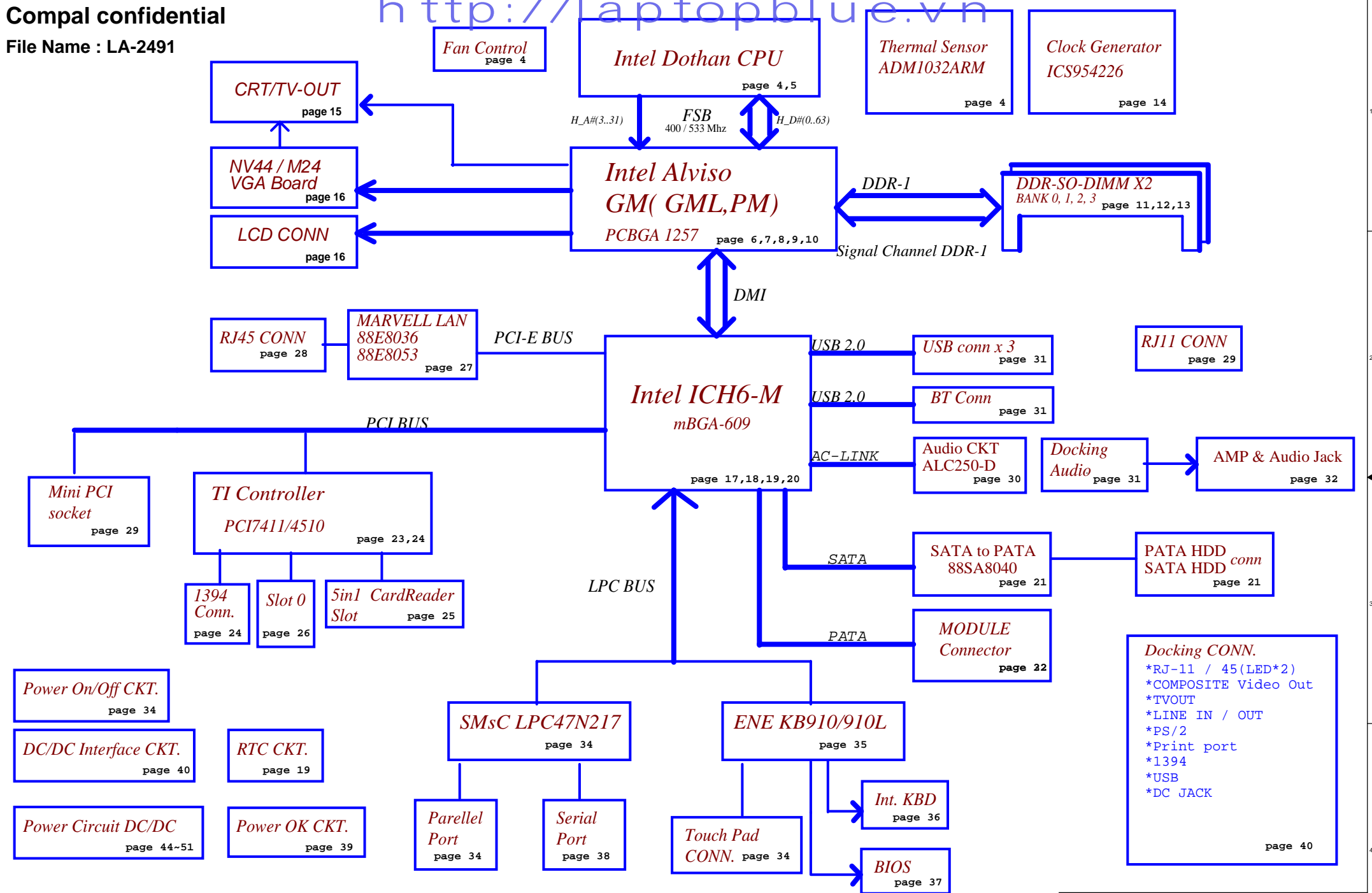
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Title	Cover Sheet
Document Number	Sakhir LA-2491
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Rev	1.0

# Compal confidential

File Name : LA-2491

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for Direct CD	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD20	2	PIRQA/PIRQB
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2'nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator ( ICS 952623)	1101 001Xb
DDR DIM#0	1001 000Xb
DDR DIM#2	1001 001Xb

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STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

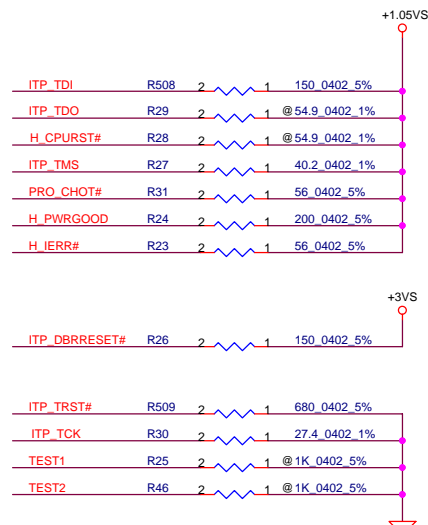
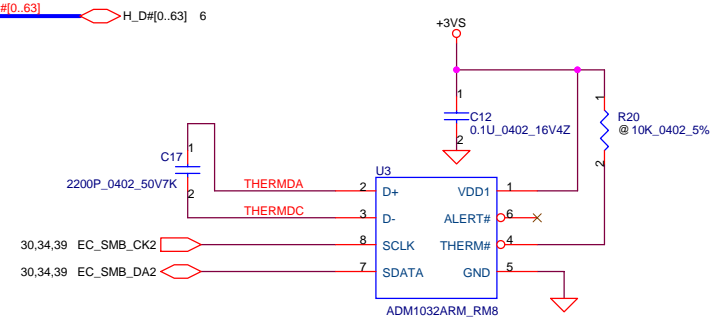
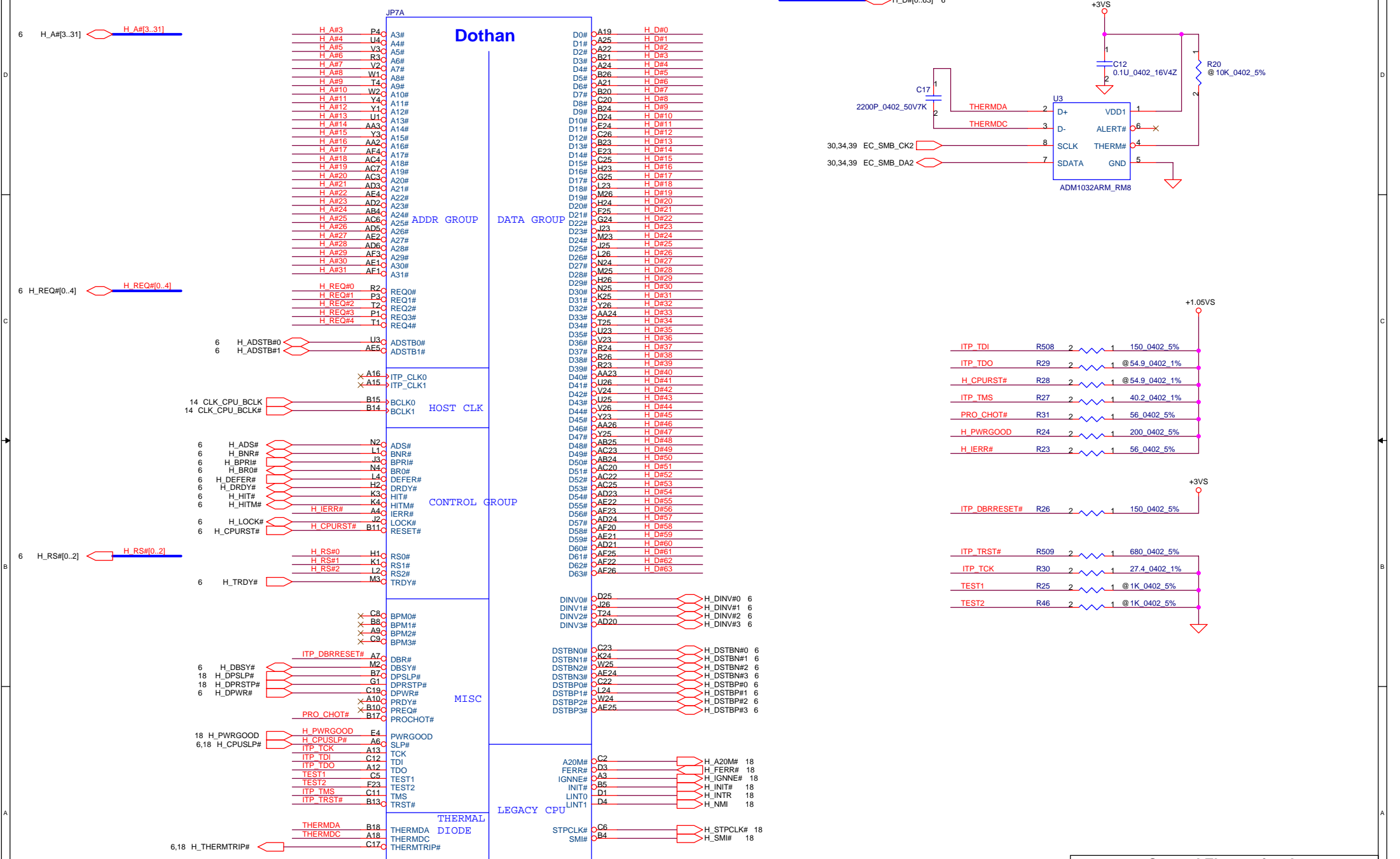
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

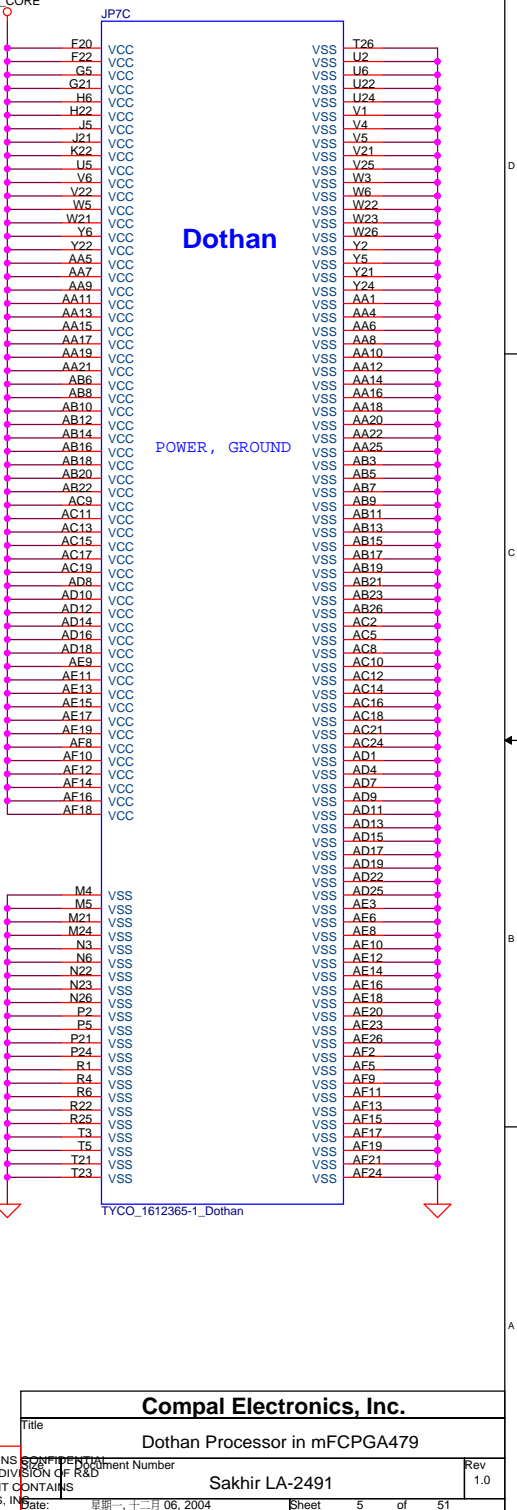
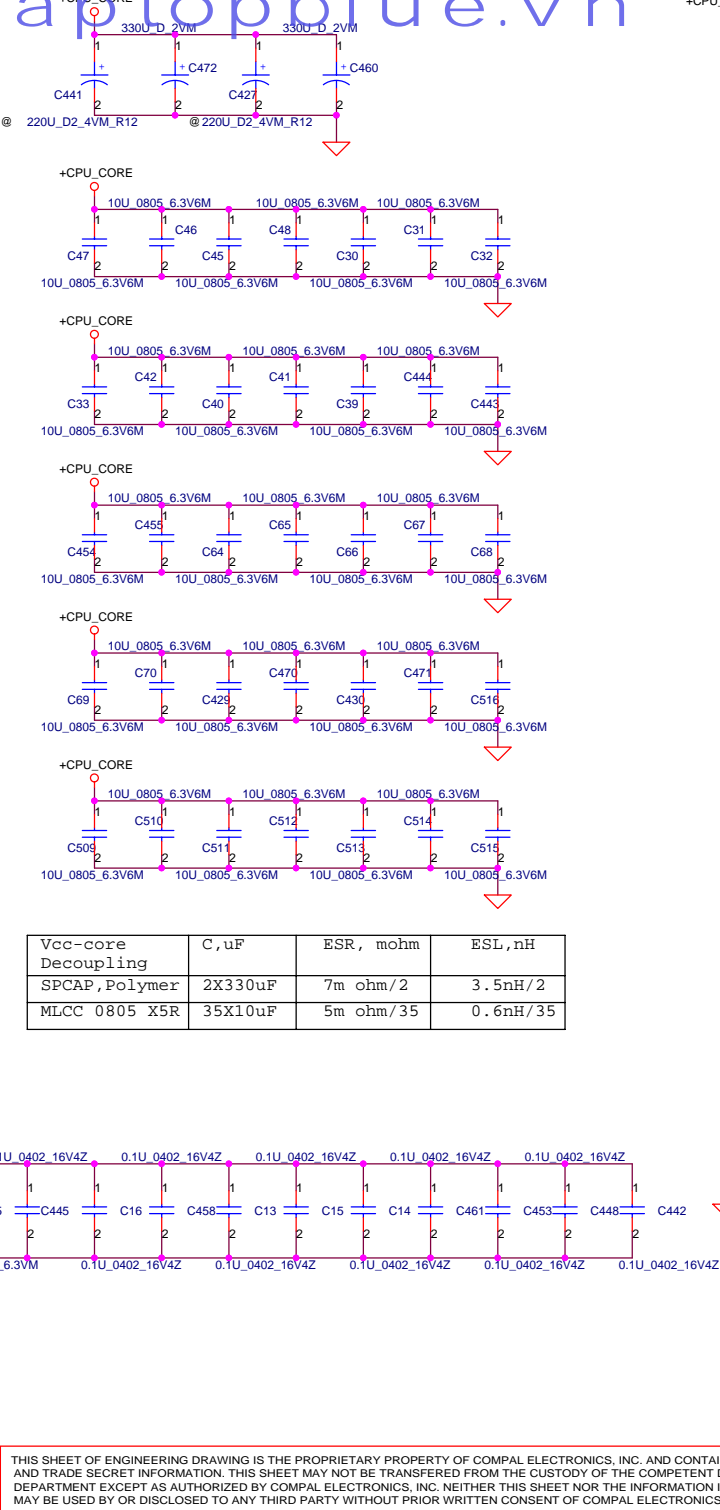
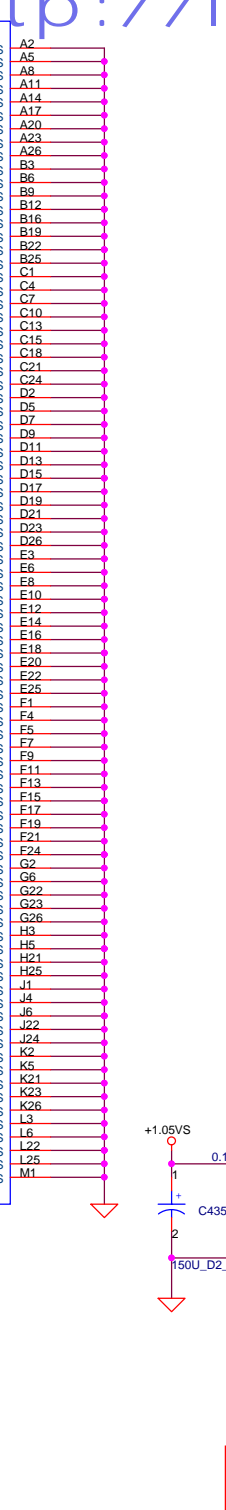
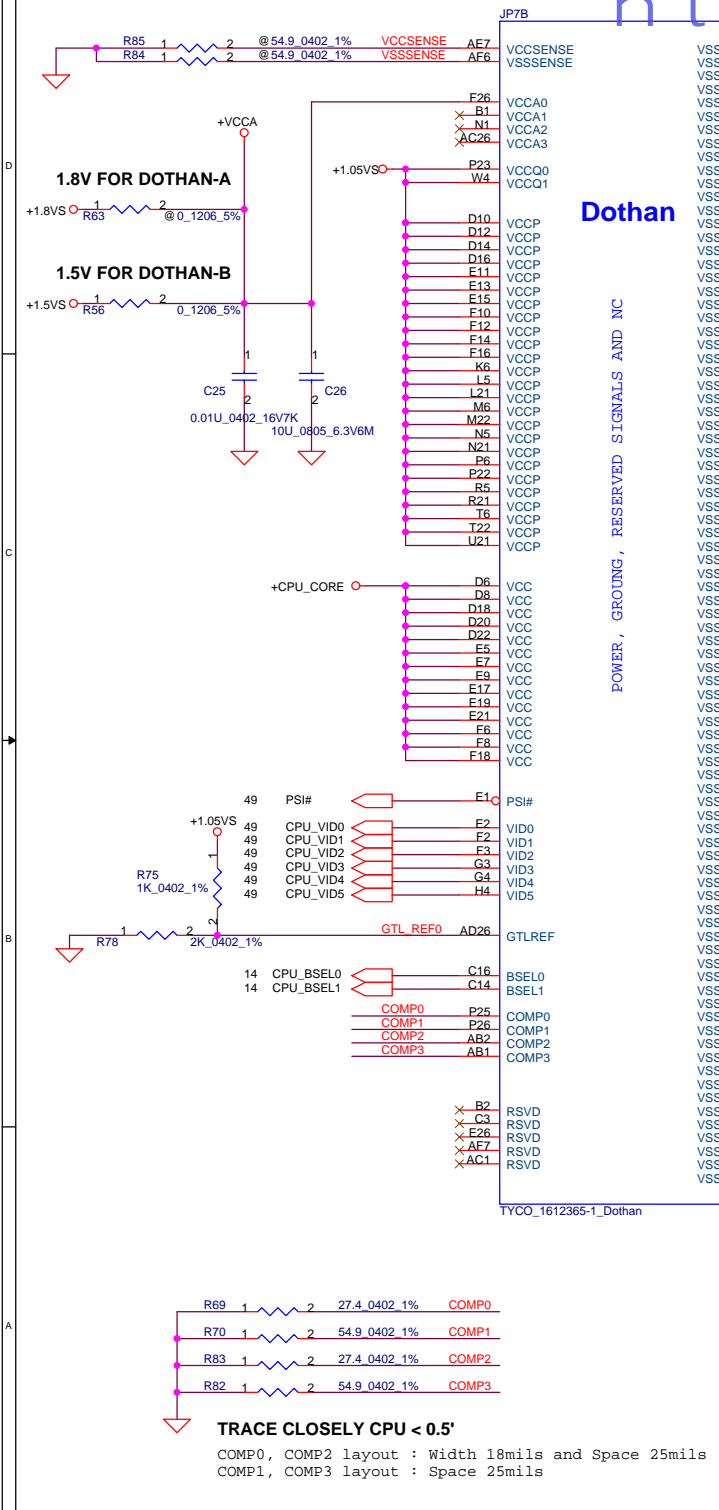
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

SKU ID Table

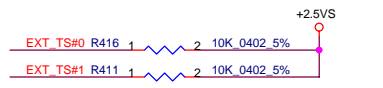
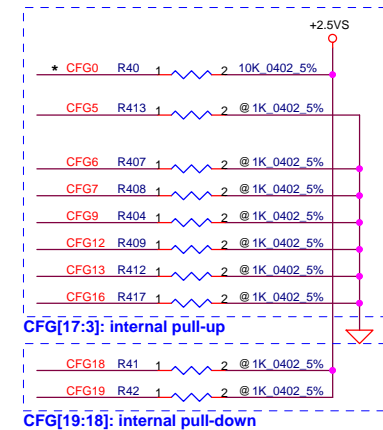
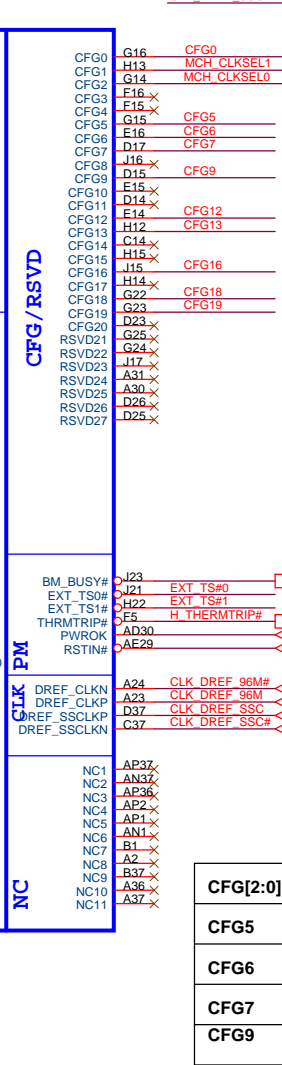
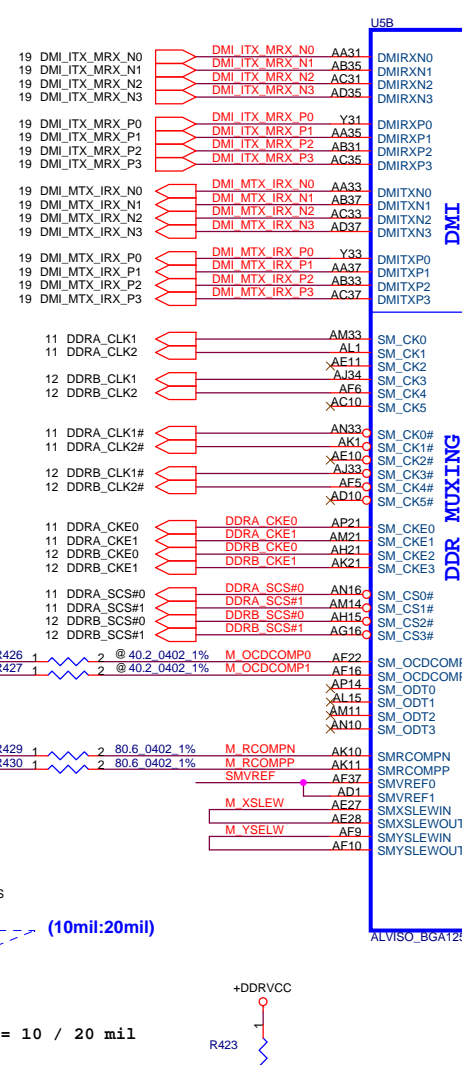
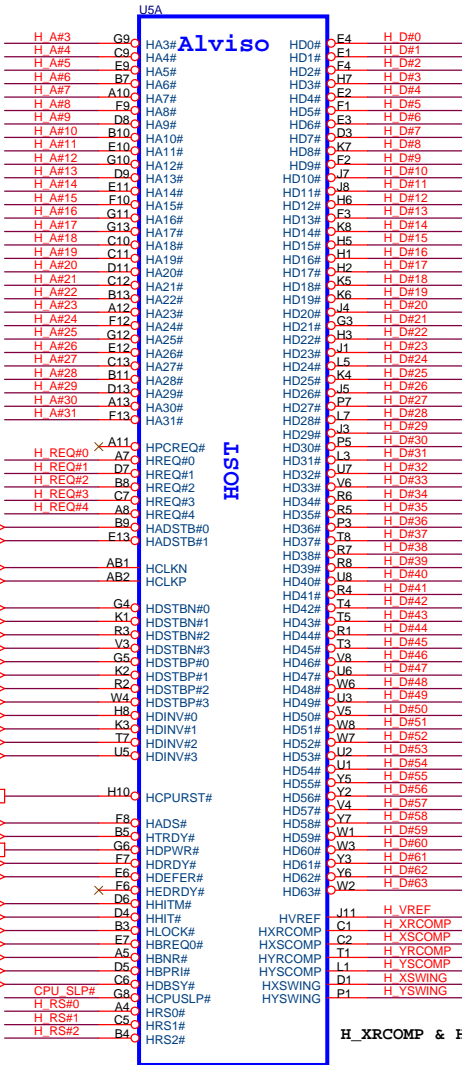
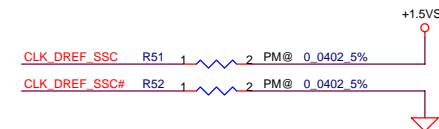
	SKU_ID_CHECK_1	7	6	5
SKU_ID_CHECK_0		1-Button	3-Buttons	7-Buttons
0	10	1		0
1	10C	3	12	2
2	10G	5		4
3	10GC	7	13	6
4	10J	11		10
5				
6				



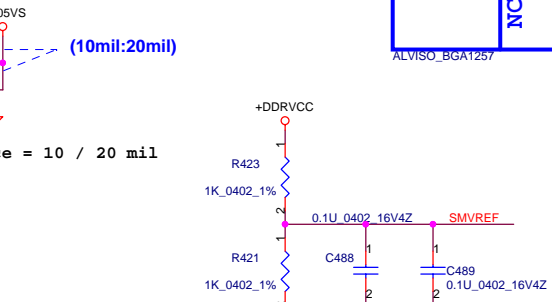
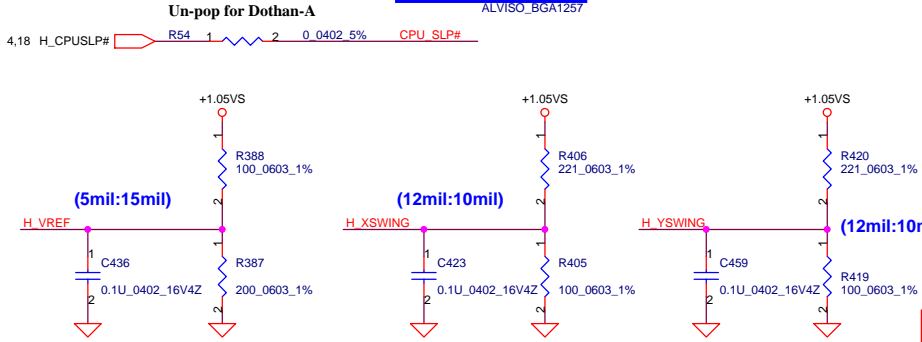
THERMDA & THERMDC Trace / Space = 10 / 10 mil



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	2X330uF	7m ohm/2	3.5nH/2
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35







CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

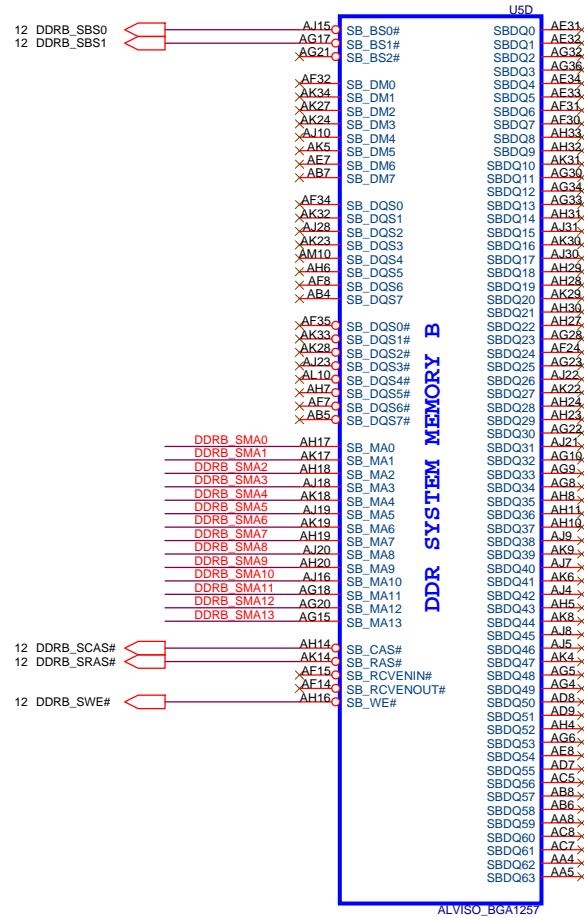
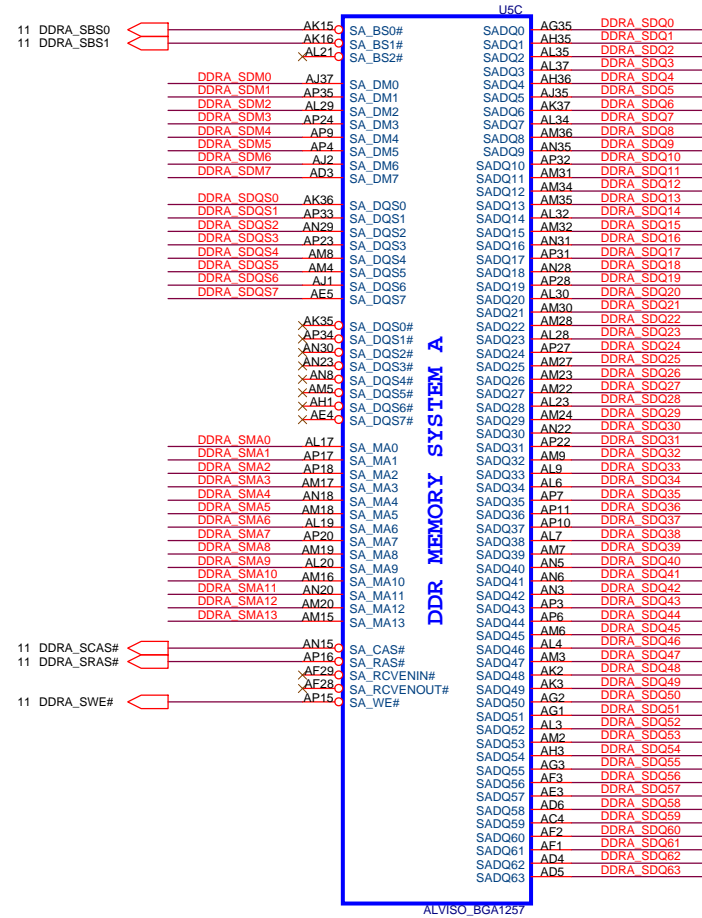


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11 DDRA\_SDQ[0..63]  DDRA\_SDQ[0..63]  
11 DDRA\_SDM[0..7]  DDRA\_SDM[0..7]  
11 DDRA\_SDQS[0..7]  DDRA\_SDQS[0..7]  
11 DDRA\_SMA[0..13]  DDRA\_SMA[0..13]

12 DDRB\_SMA[0..13]  DDRB\_SMA[0..13]

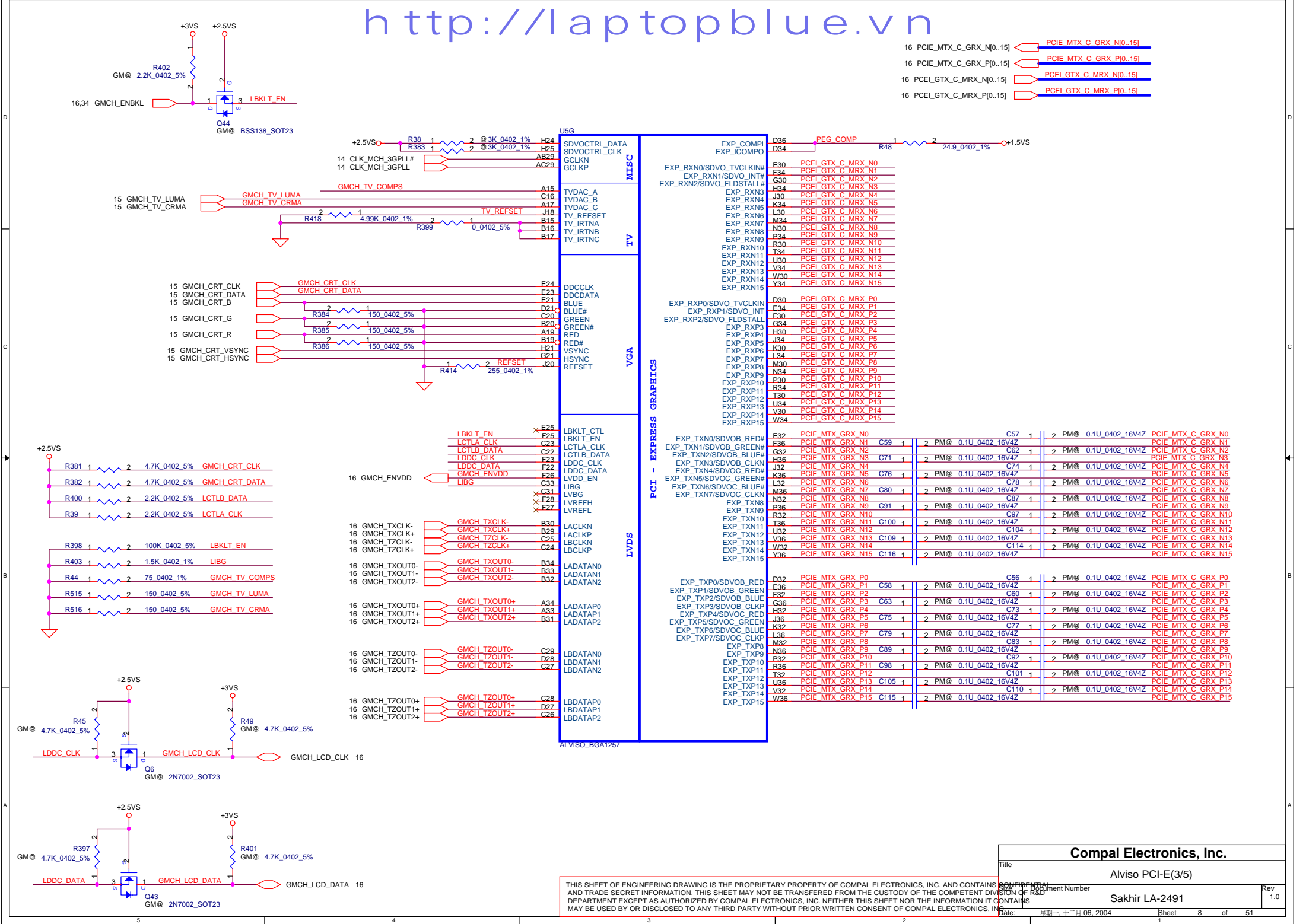


ALVISO\_BGA1257

ALVISO\_BGA1257

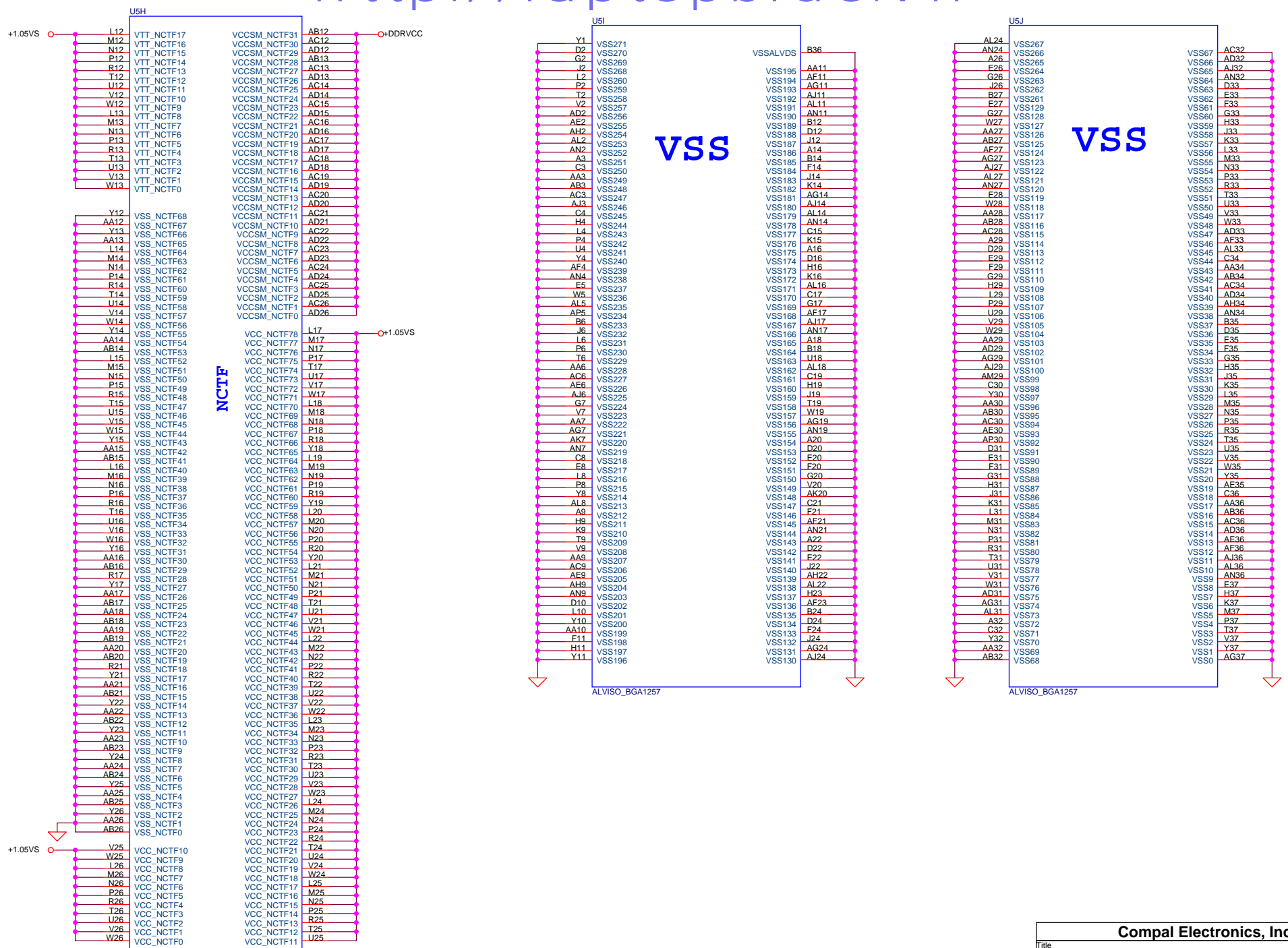
DDR MEMORY SYSTEM A

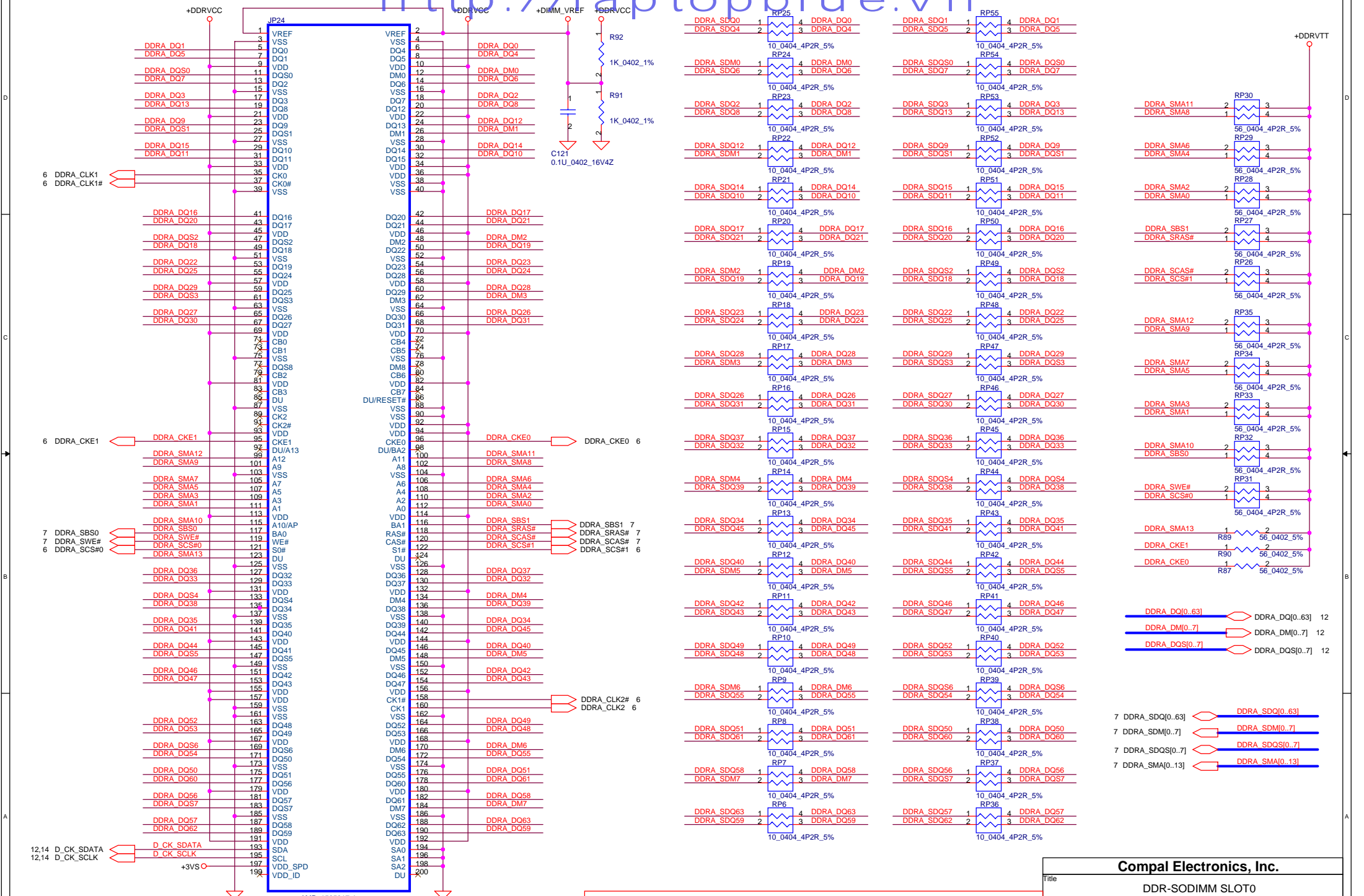
DDR SYSTEM MEMORY B



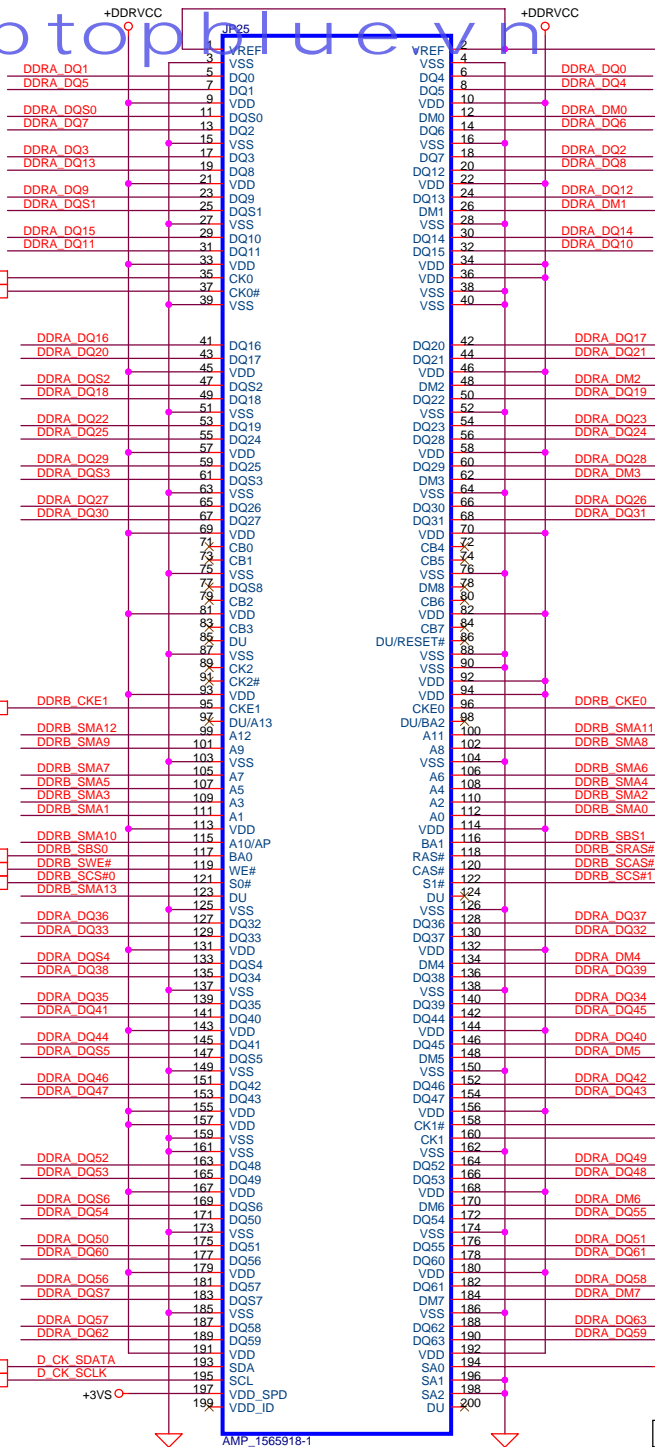
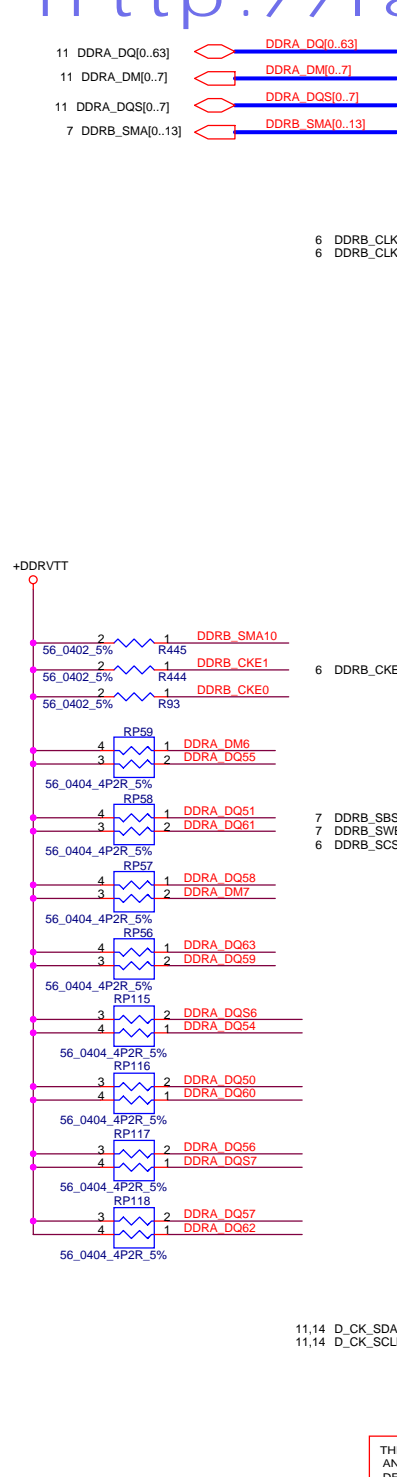
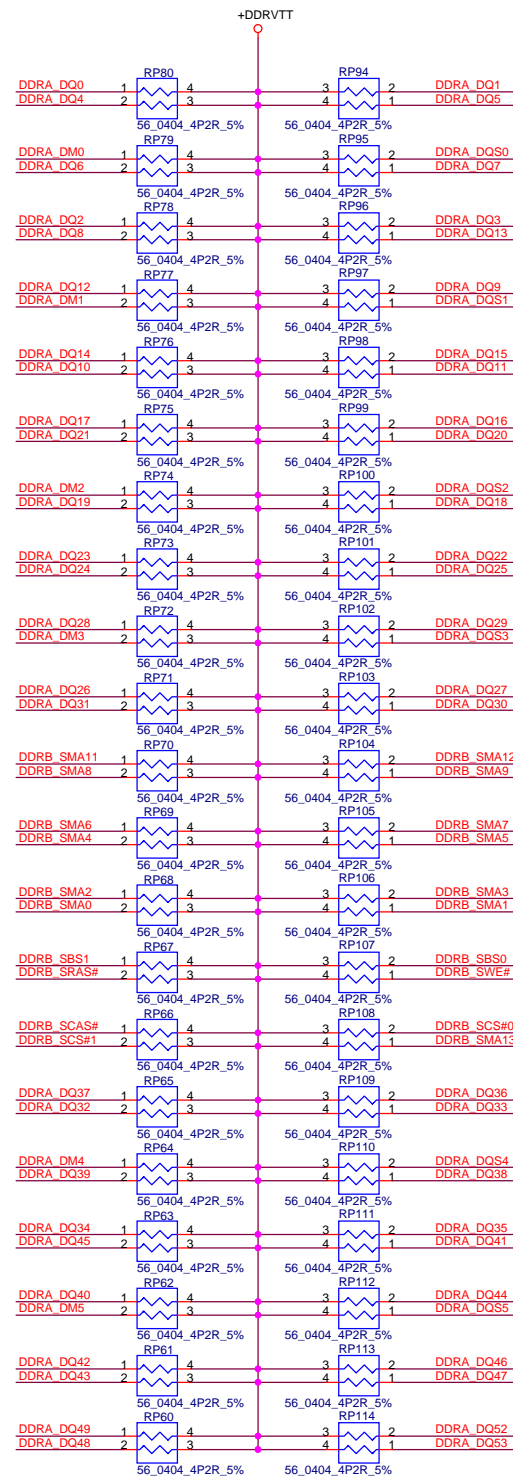




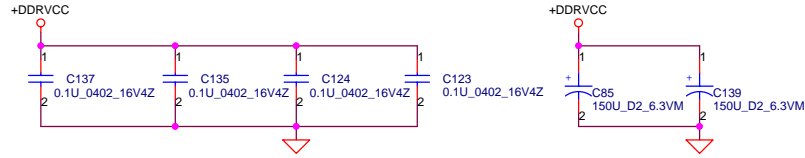
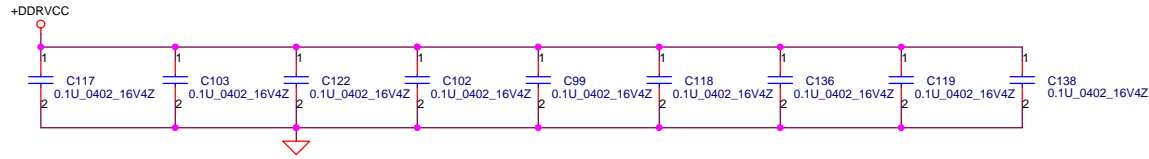




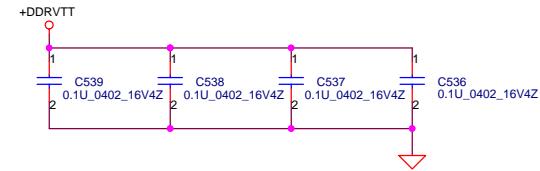
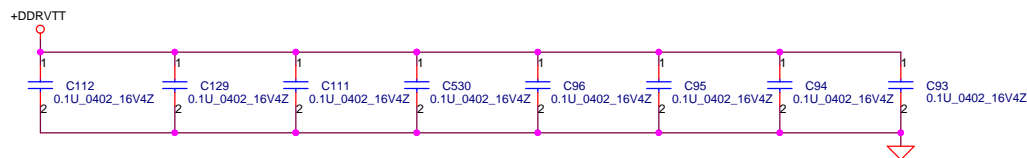
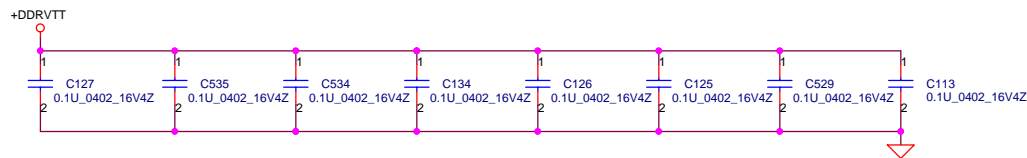
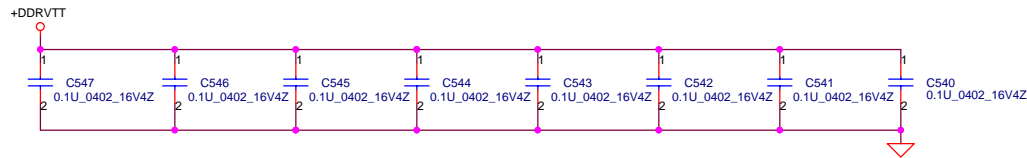
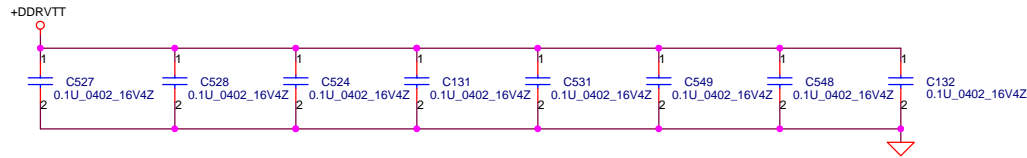
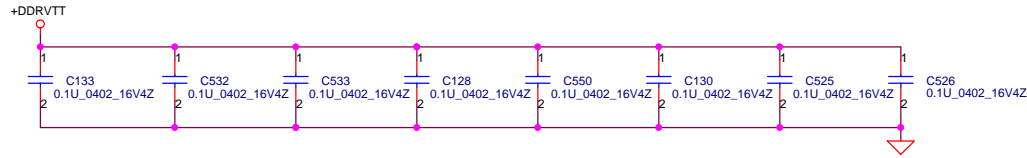
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**Layout note :**  
Distribute as close as possible to DDR-SODIMM.



**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25V



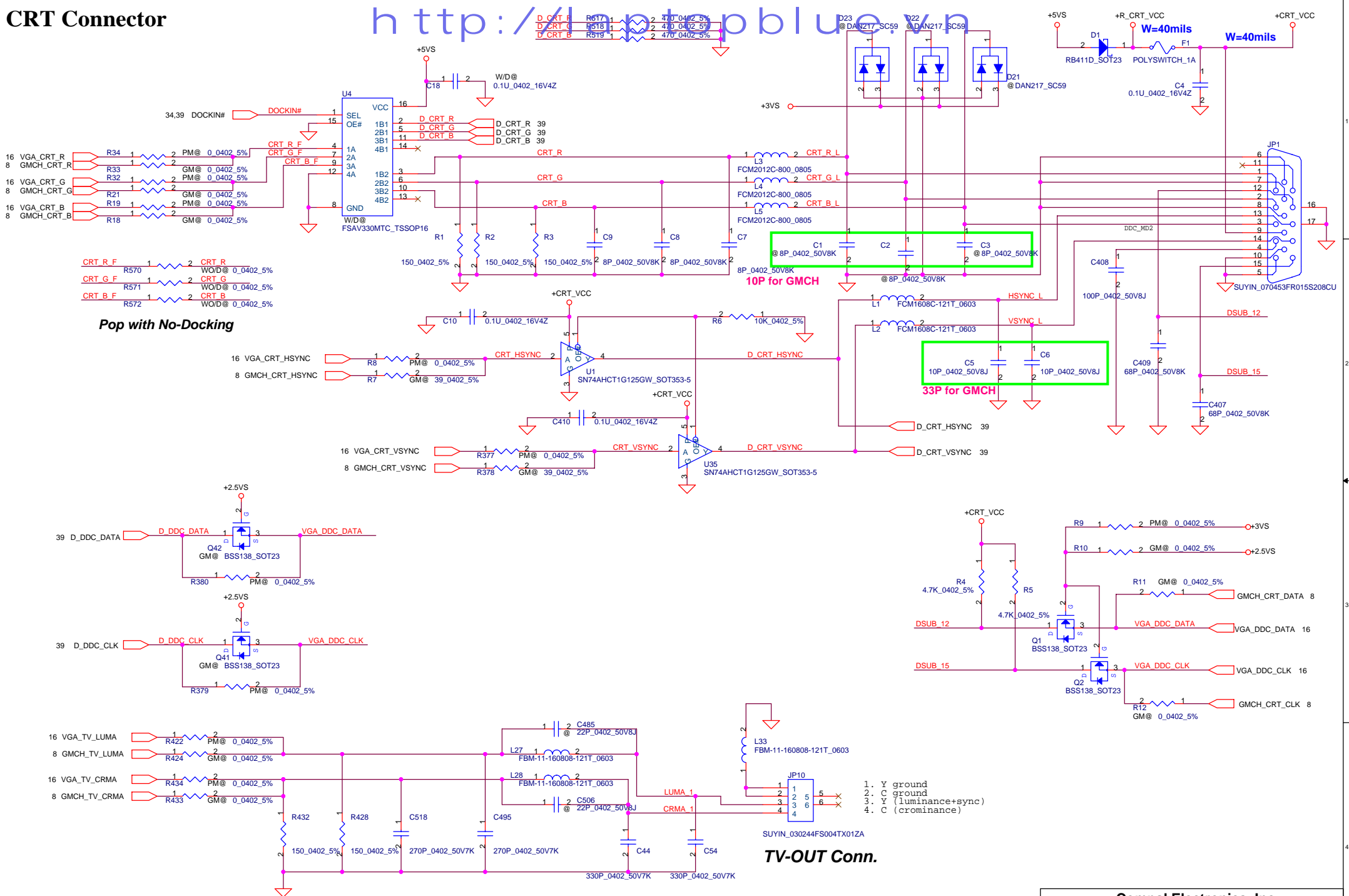




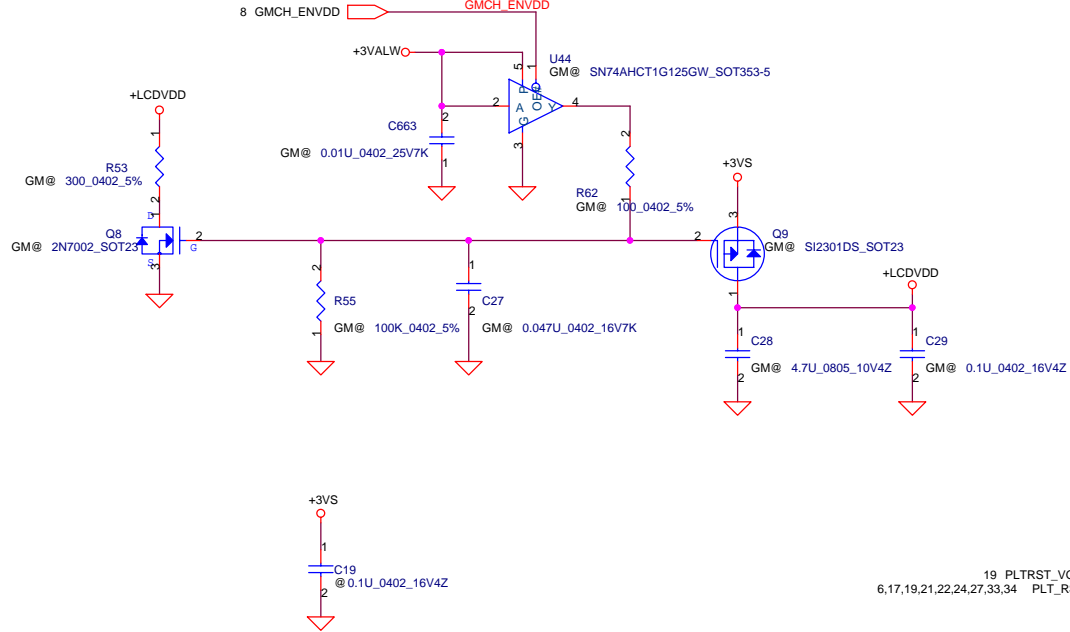


# CRT Connector

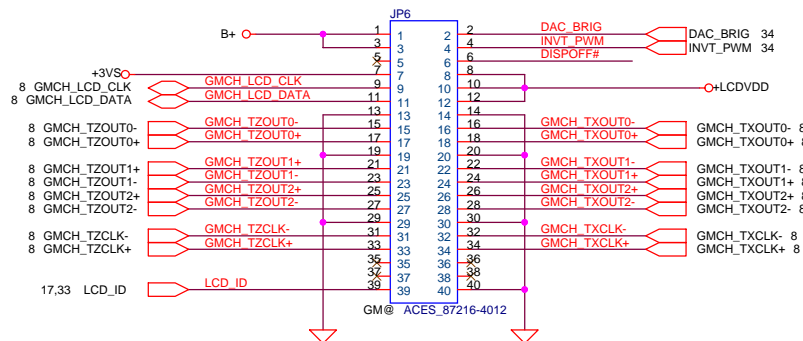
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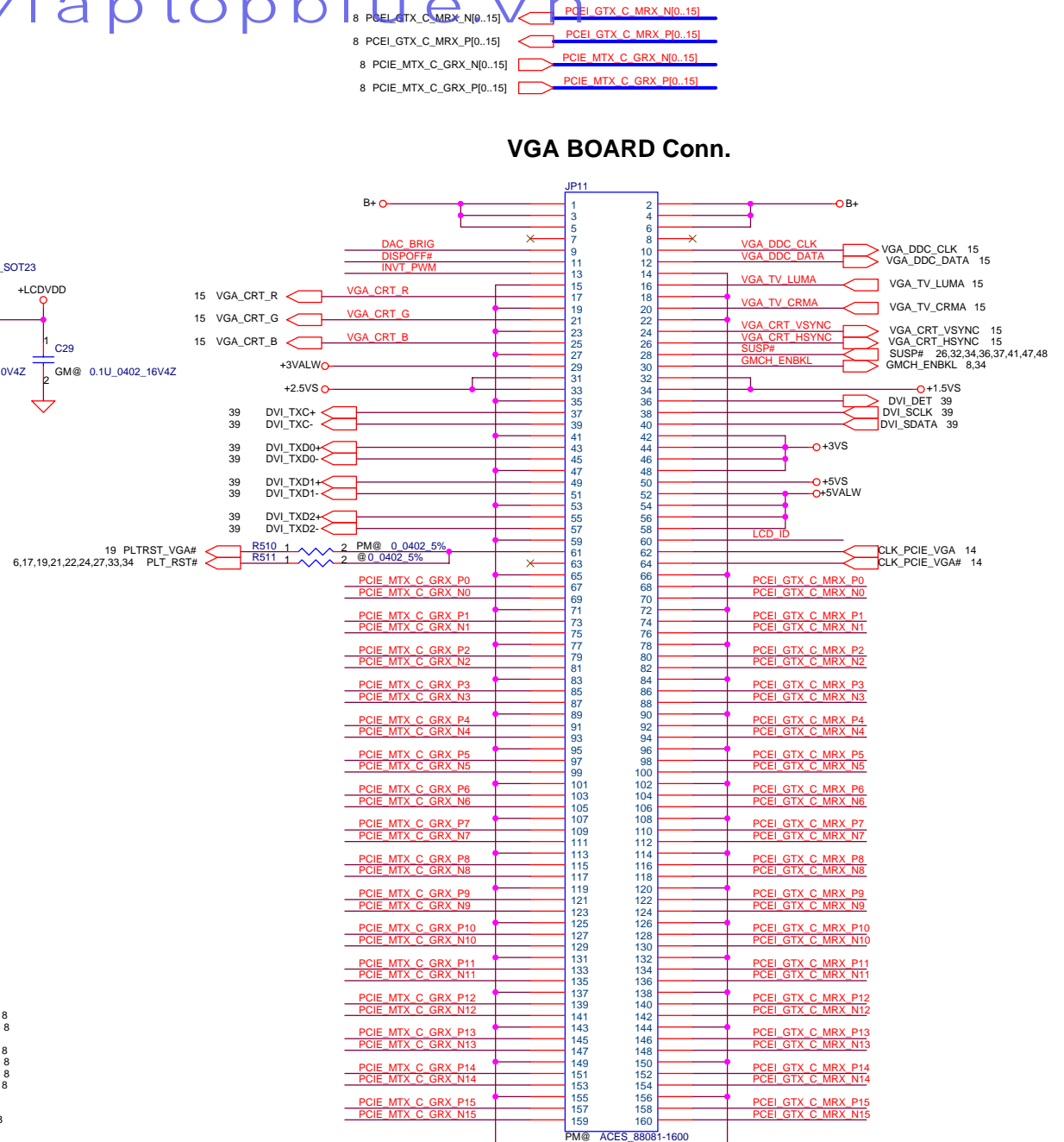
## LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.



## VGA BOARD Conn.

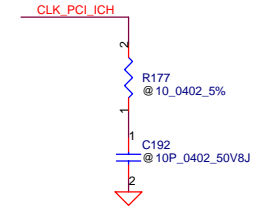
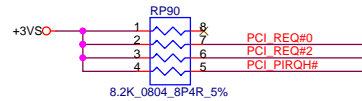


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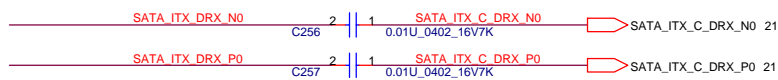
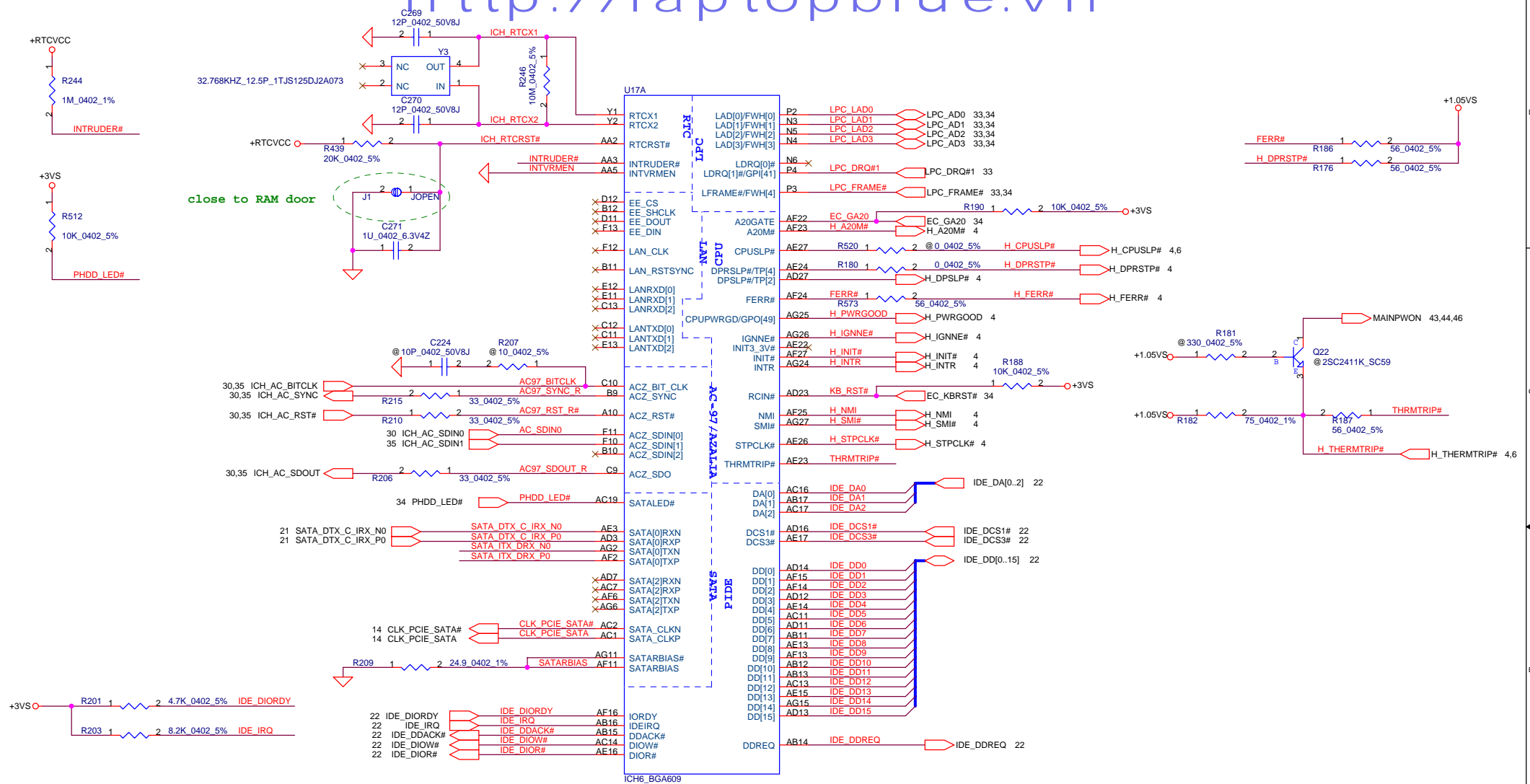
VGA / LCD CONN.

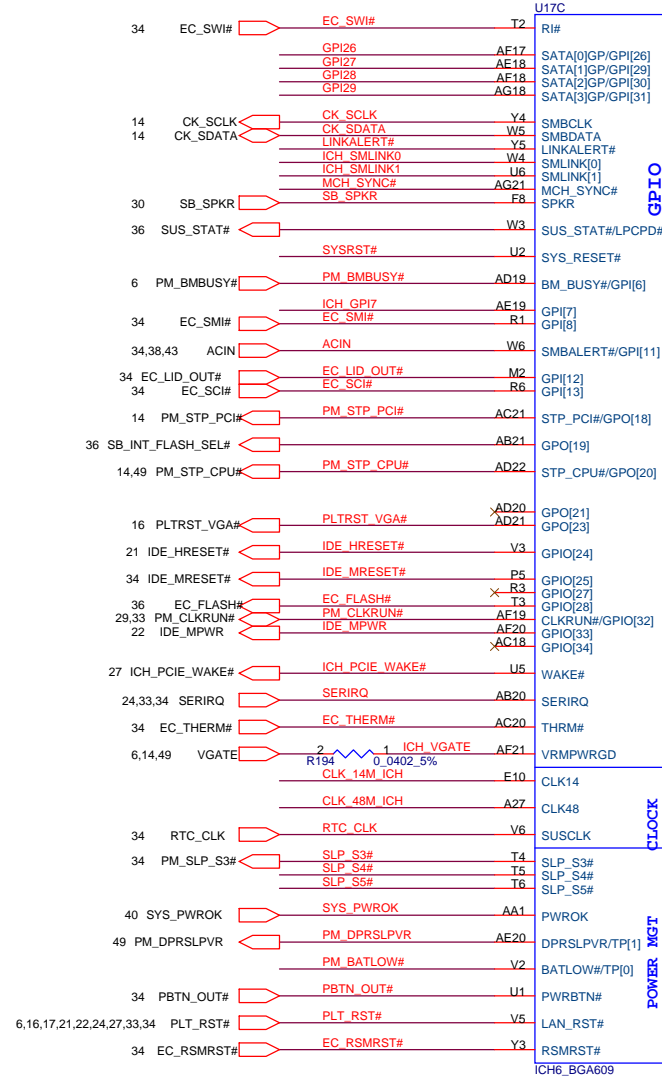
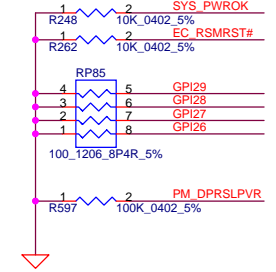
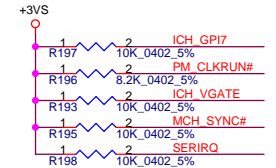
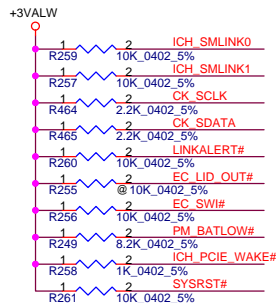
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Place near ICH6 side.





## PCI-EXPRESS

## DIRECT MEDIA INTERFACE

## USB

## POWER MGT

## CLOCK

## USB

## POWER MGT

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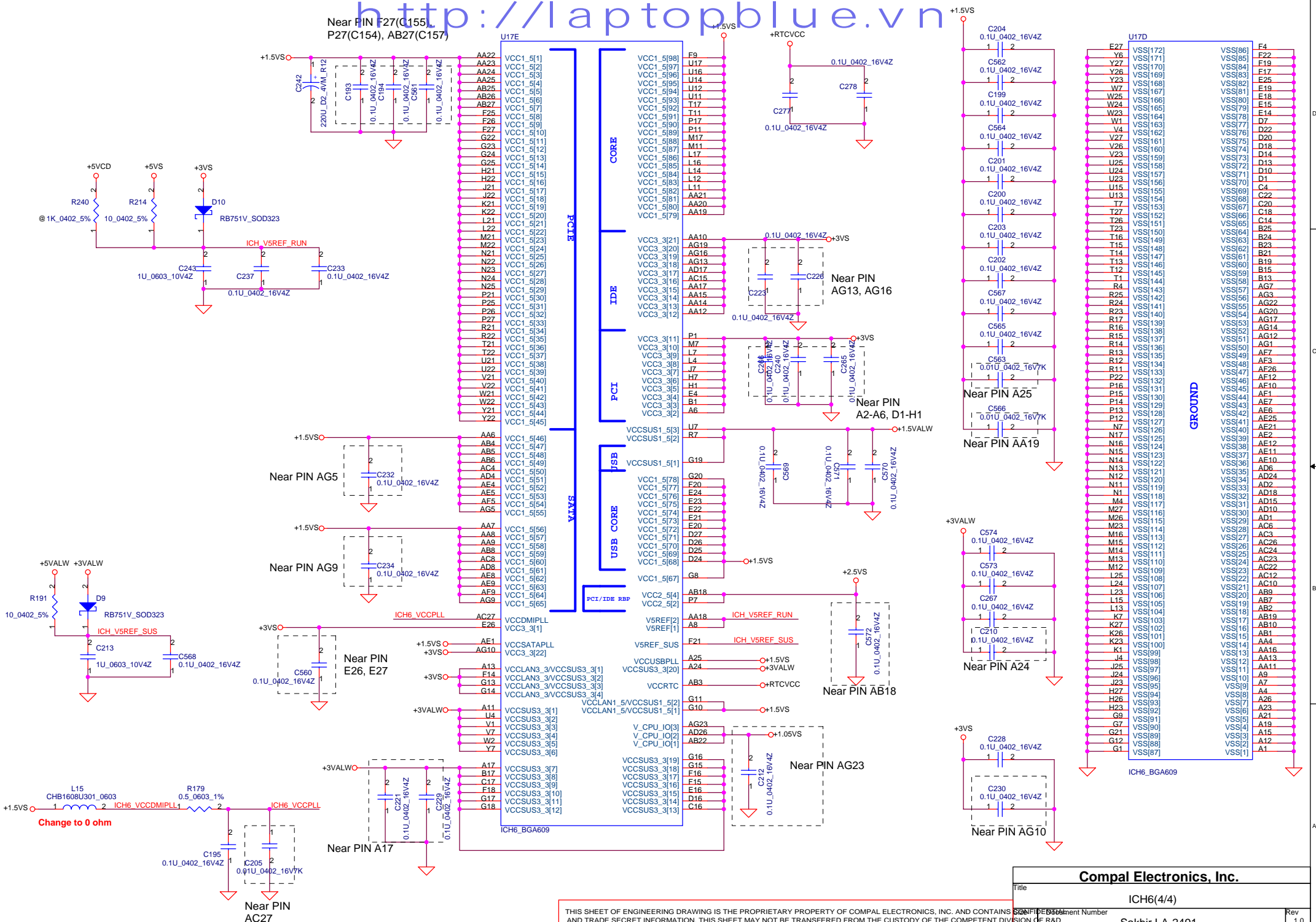
## POWER MGT

## CLOCK

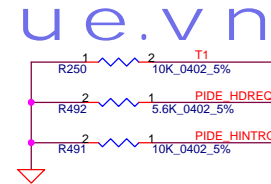
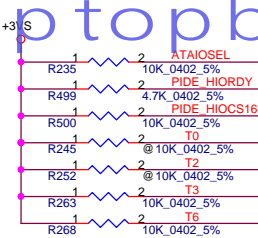
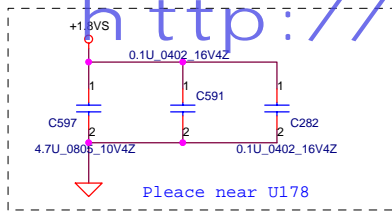
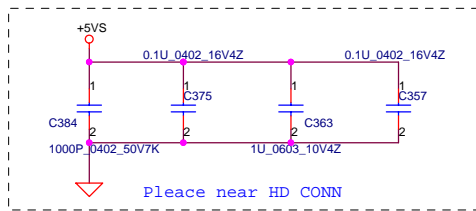
## USB

## POWER MGT

Near PIN F27(C155),  
P27(C154), AB27(C157)



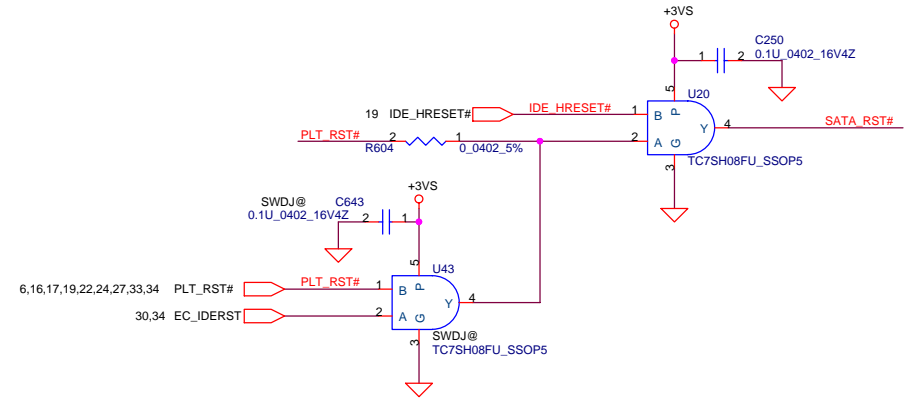
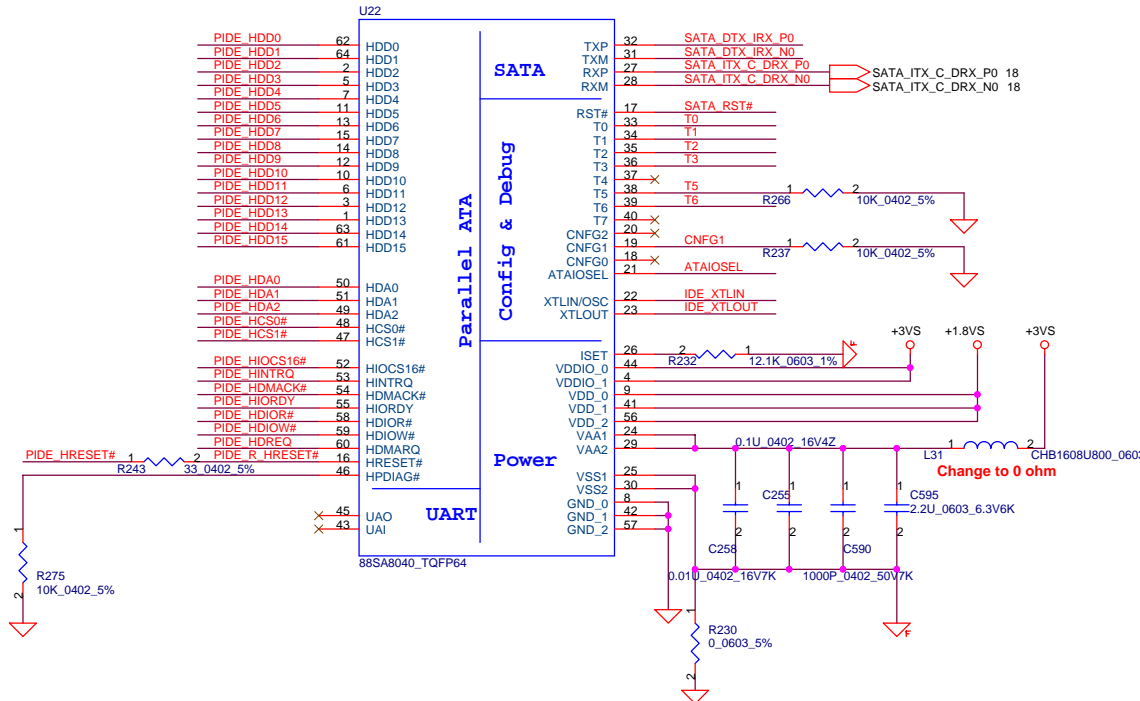




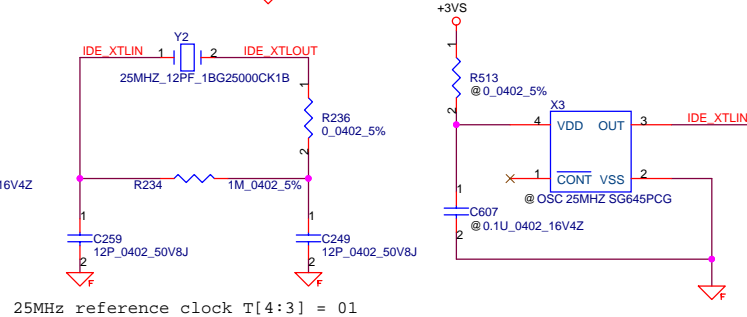
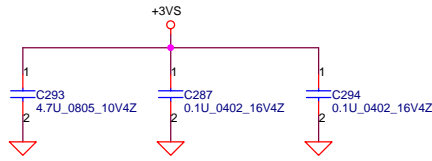
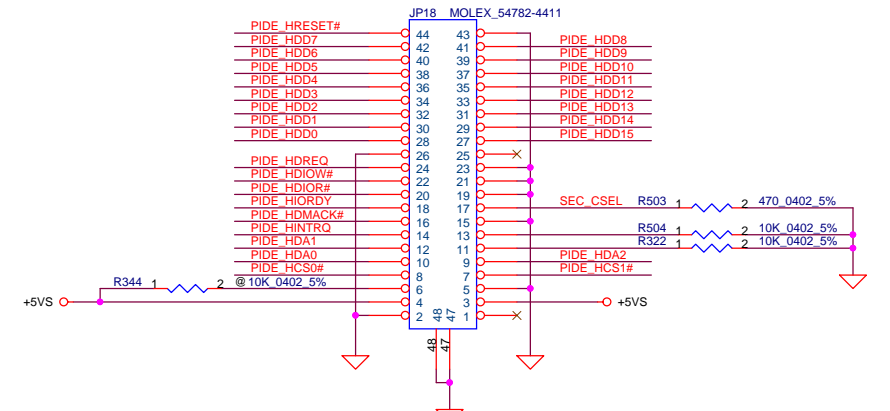
## SATA Module

Sets maximum transfer rate and UDMA mode

CNFG2 INT PD	CNFG1 INT PD	CNFG0 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved

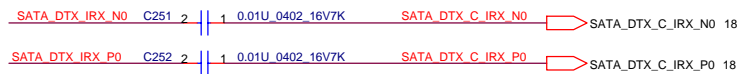


## P-ATA HDD Conn.

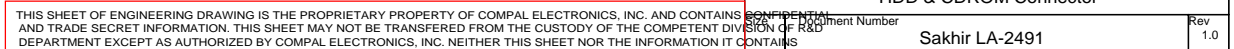
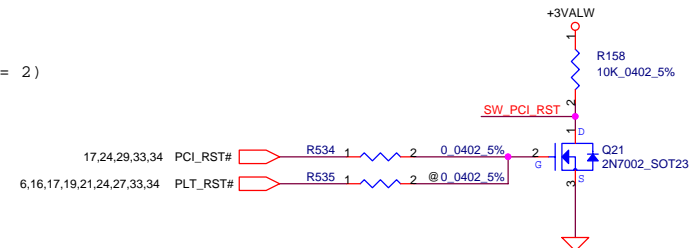
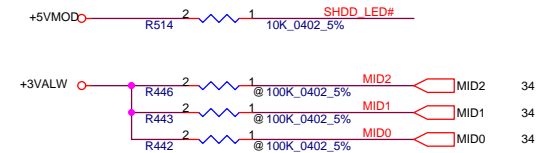
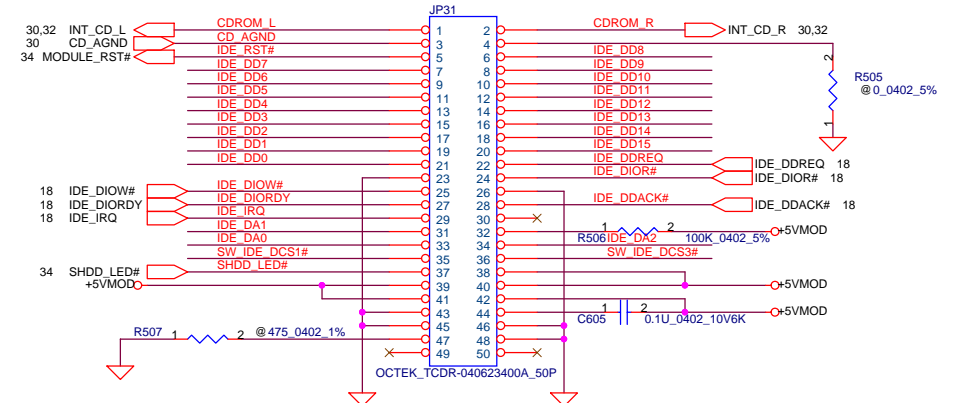
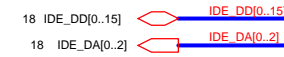


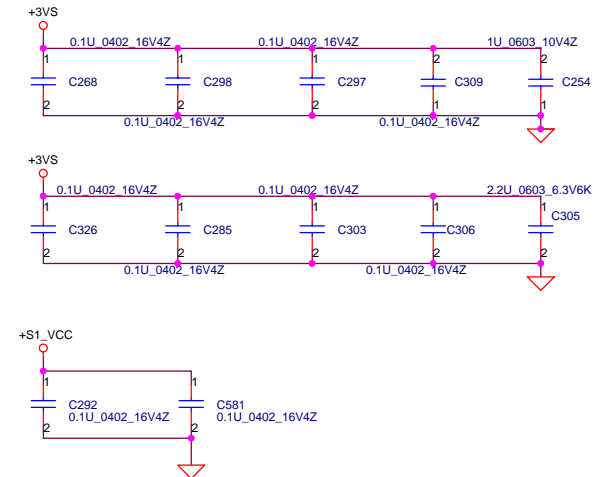
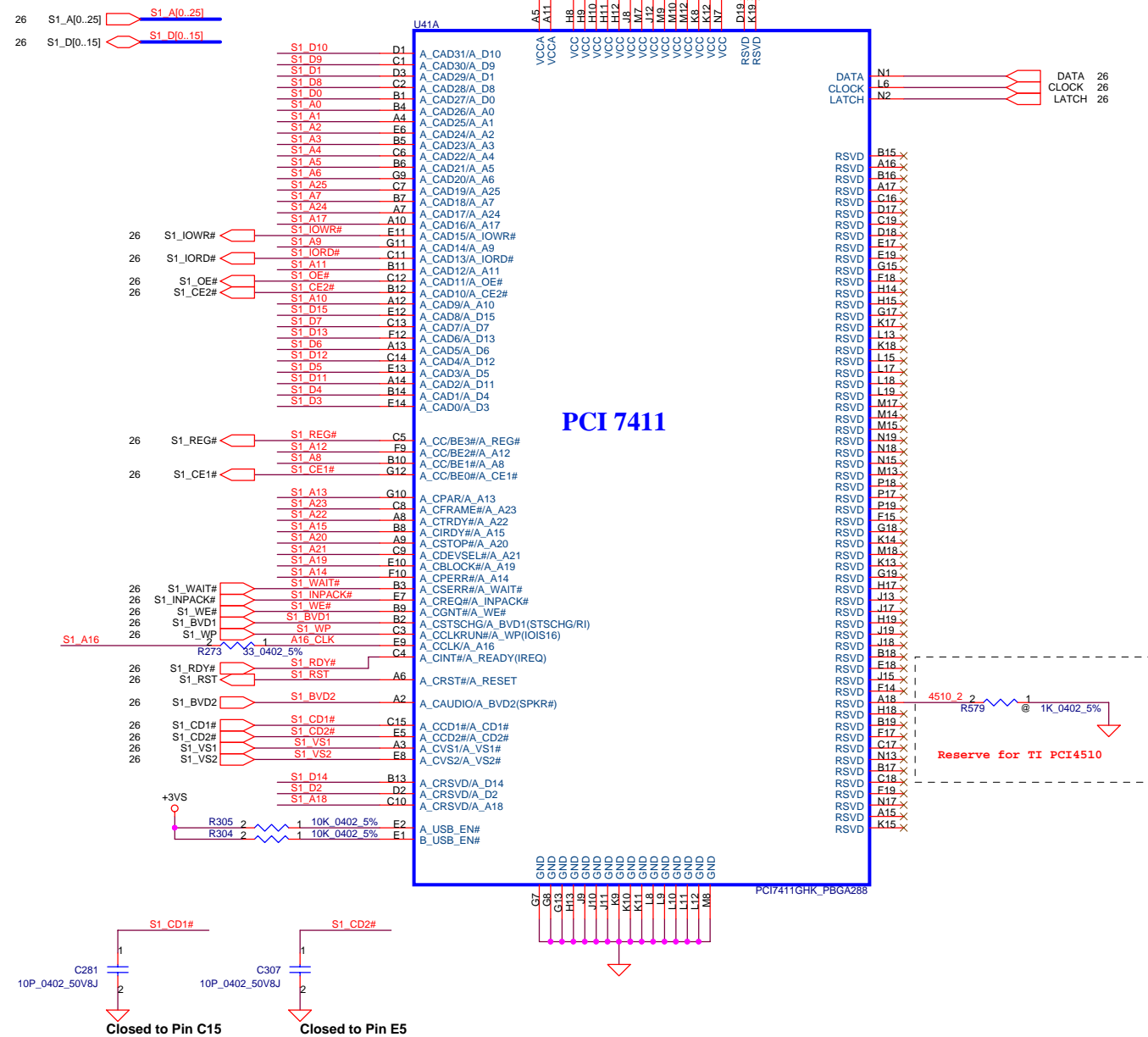
25MHz reference clock T[4:3] = 01

Place near connector side.



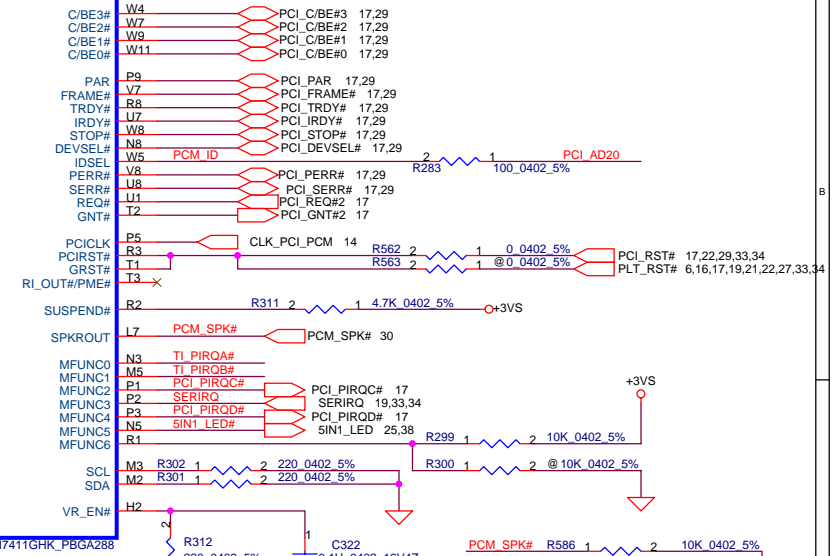
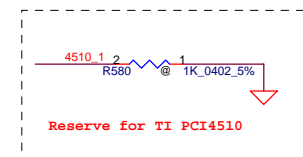
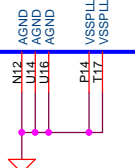
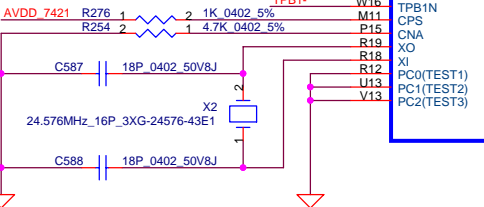
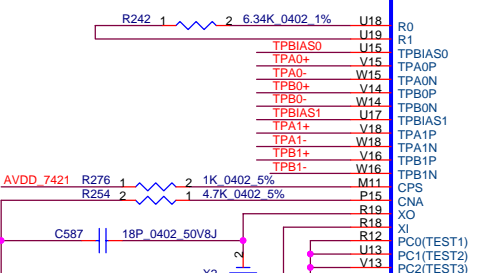
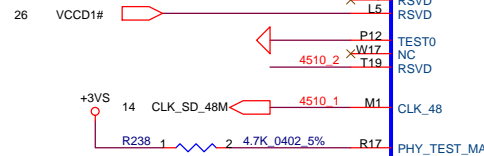
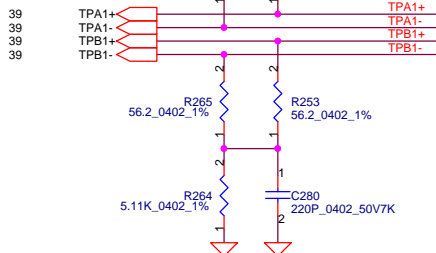
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4510 2 2 R579 @ 1K\_0402\_5% 1

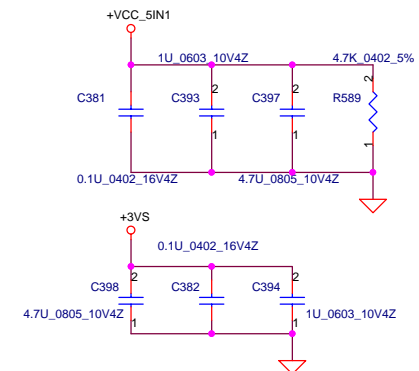
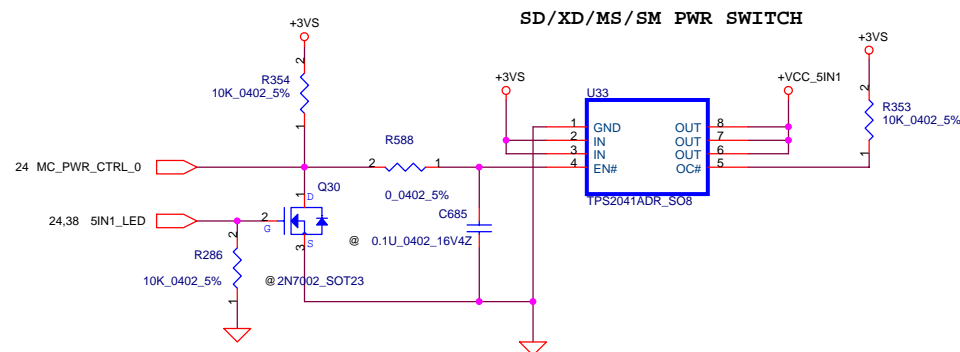
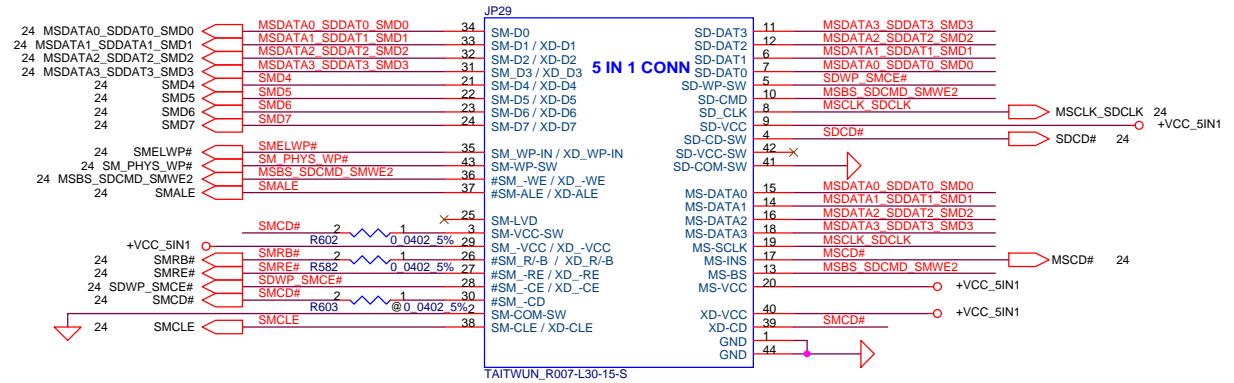
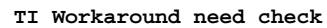
Reserve for TI PCI4510



Title		PCI7421(2/2)	
INS. CONFIDENTIAL DIVISION OF SIGN OF DOCUMENT NUMBER T. CONTAINS INC.	Sakhir LA-2491		Rev 1.0
Date:	星期一, 十二月 06, 2004	Sheet	24 of 51

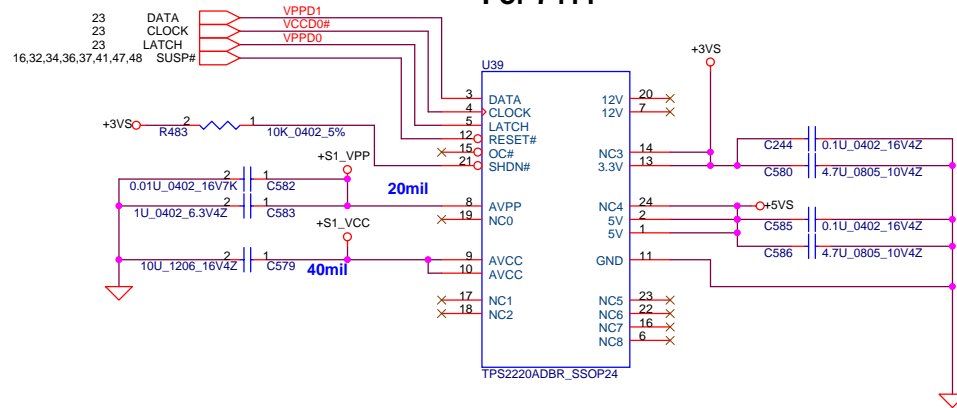
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JP29



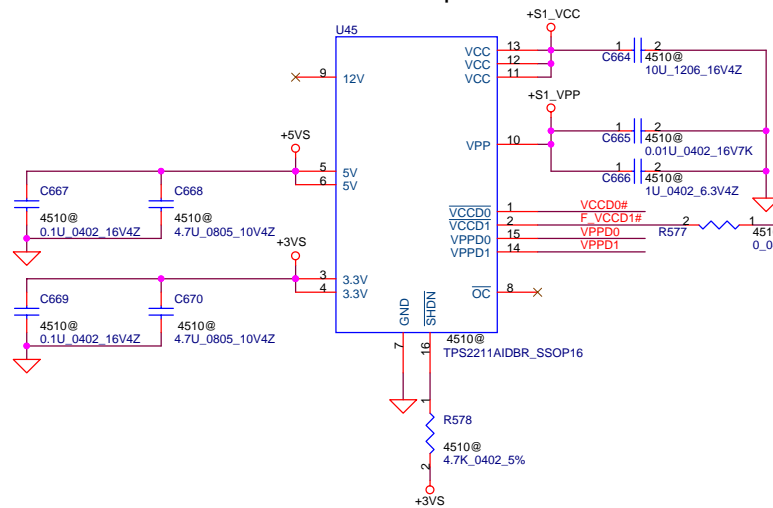
## Power Switch for PCMCIA

**For 7411**

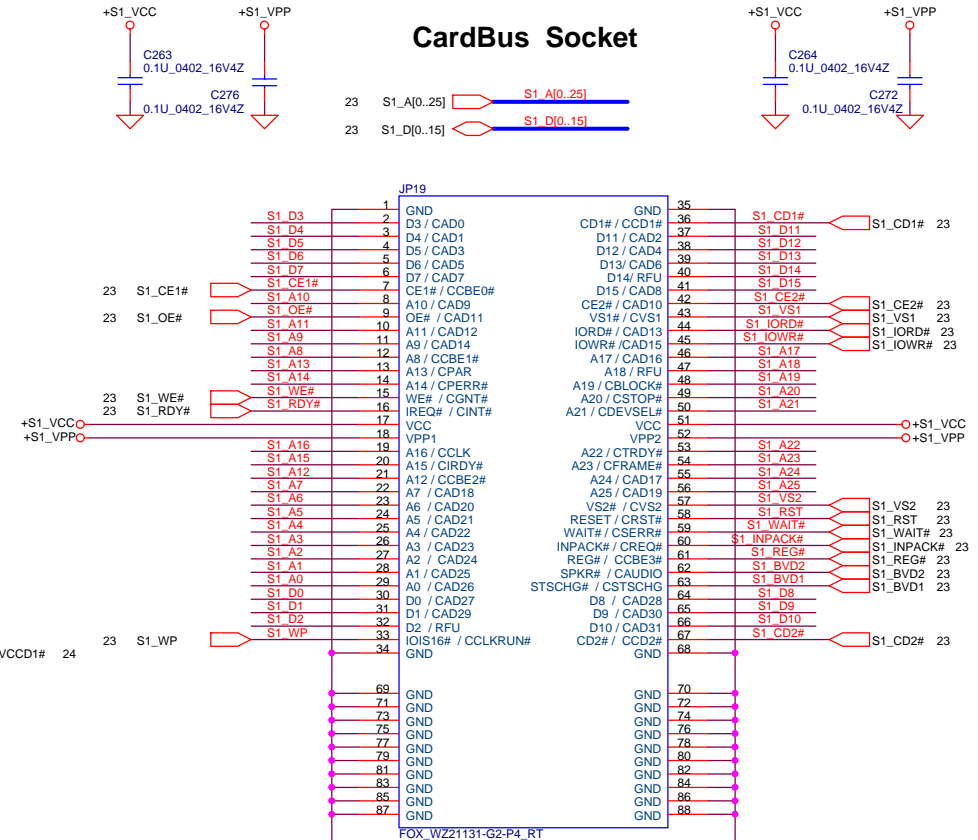


**For 4510**

**use U4 footprint**



## CardBus Socket



**Compal Electronics, Inc.**

CardBUS Socket

Sakhir LA-2491

Rev	1.0
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Title

NS CONFIDENTIAL  
DIVISION OF B&D Document Number

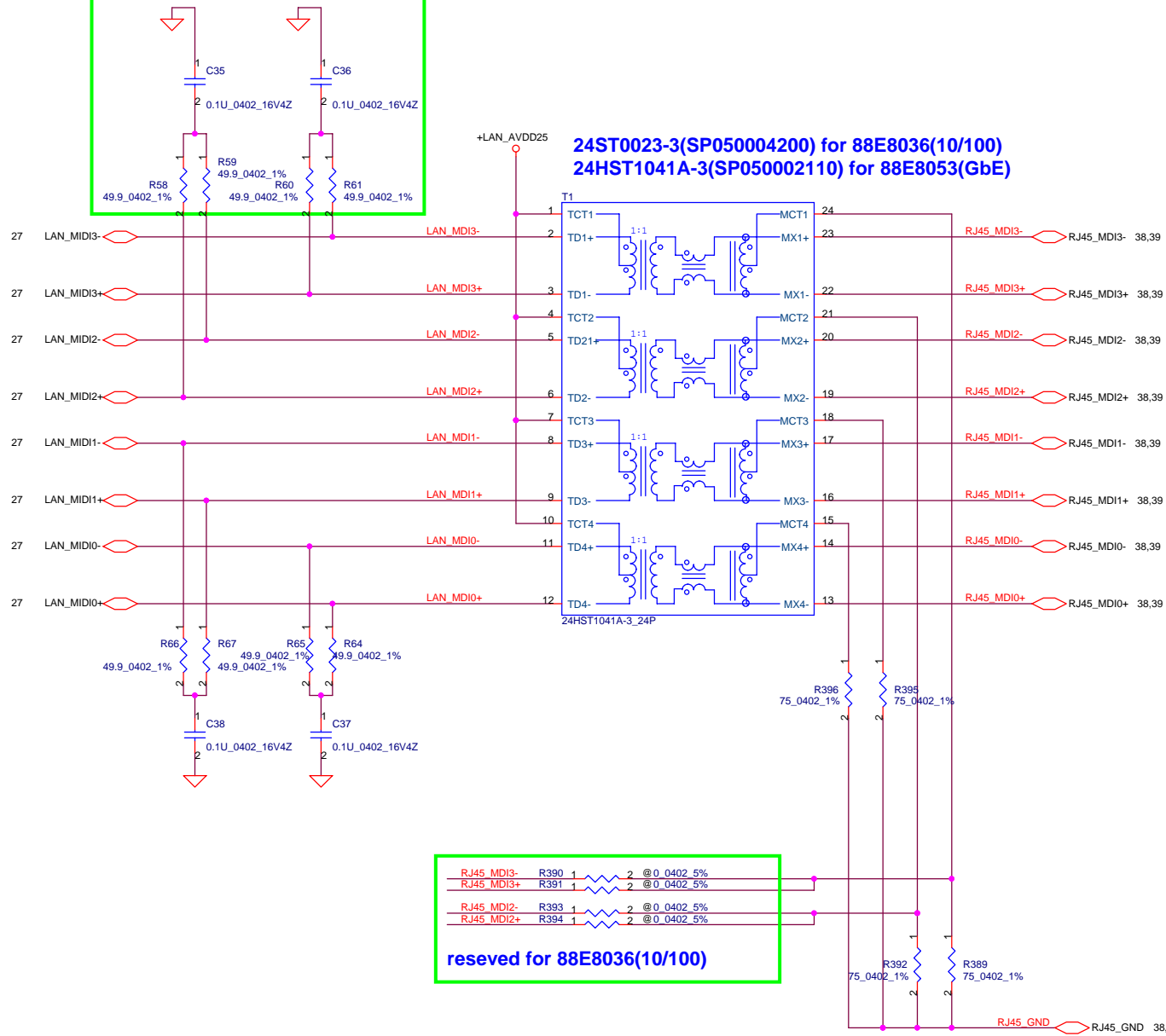
Date: 星期一, 十二月 06, 2004

Sheet 26 of 51



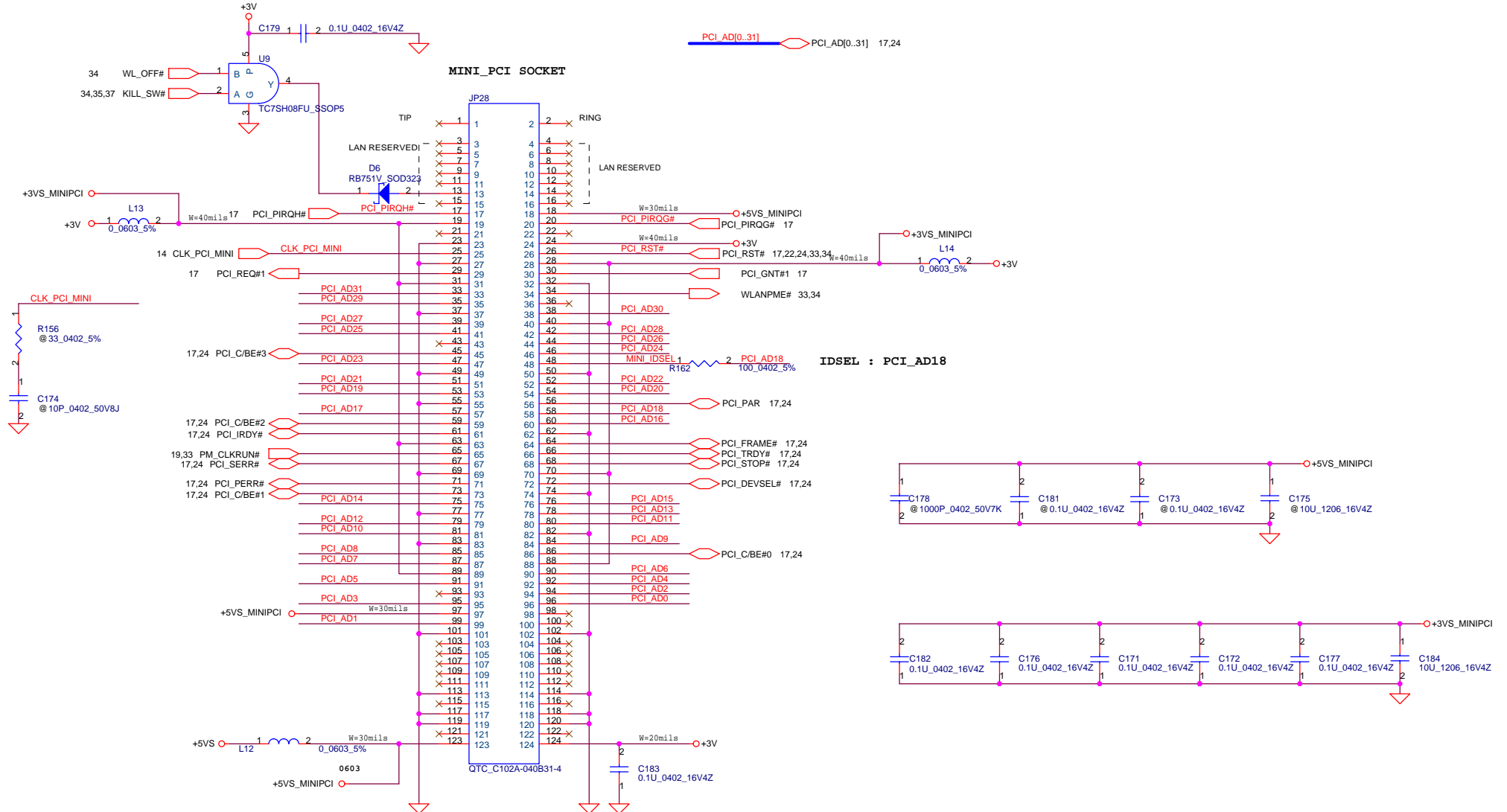


unpop when use 88E8036(10/100)

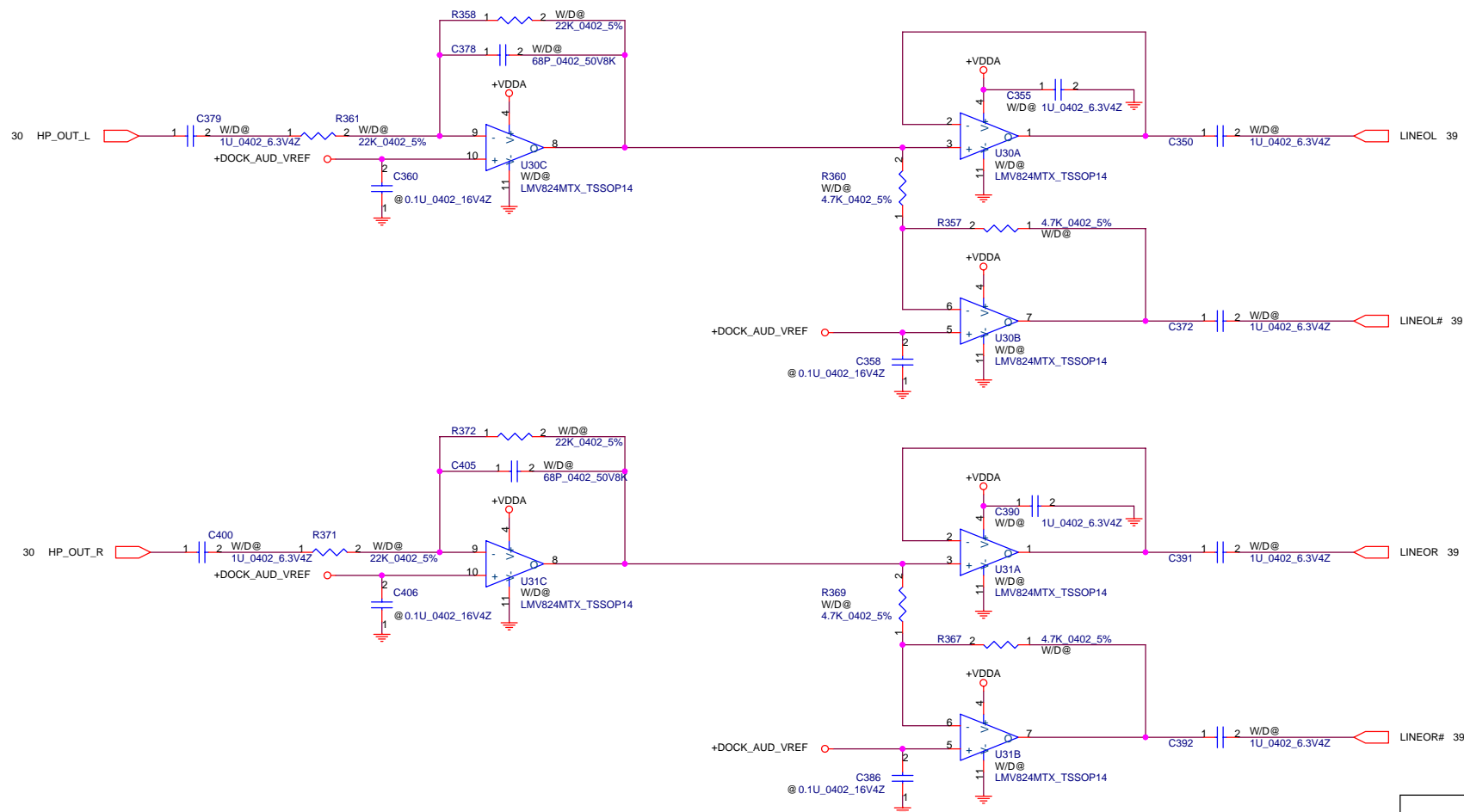
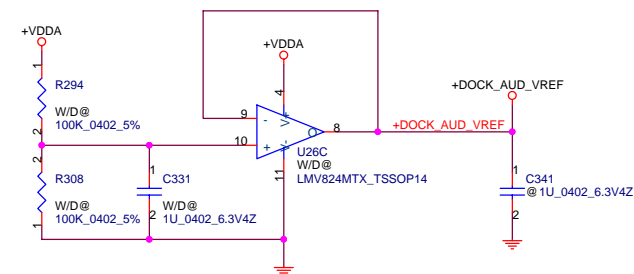


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Compal Electronics, Inc.			
Title	LAN Conn.		
Document Number	Sakhir LA-2491		
Rev	1.0		
Date	星期一, 十二月 06, 2004	Sheet	28 of 51

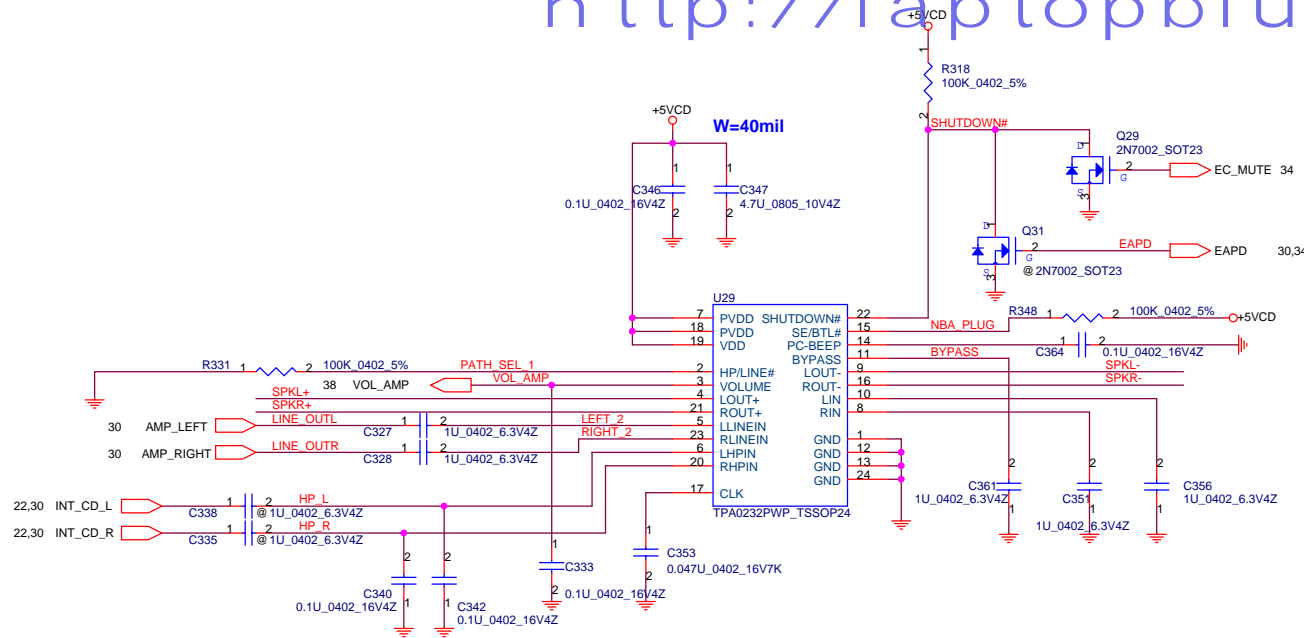




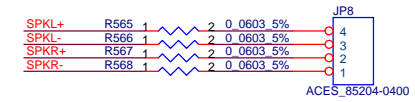


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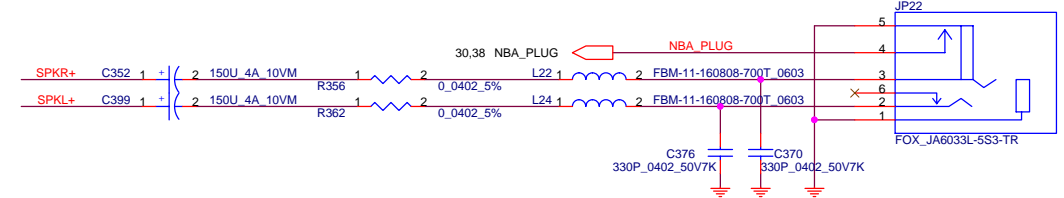
<b>Compal Electronics, Inc.</b>			
Title		Docking Audio	
Size	Document Number	Sakhir LA-2491	Rev 1.0
Date:	星期一, 十二月 06, 2004	Sheet 31	of 51



## Speaker Conn.



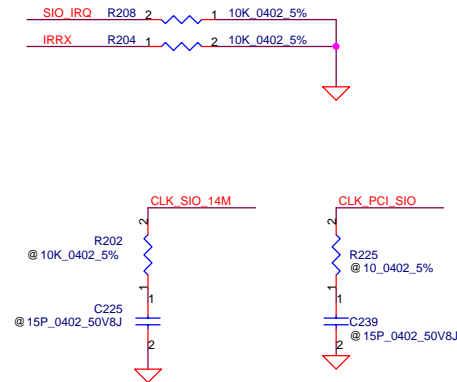
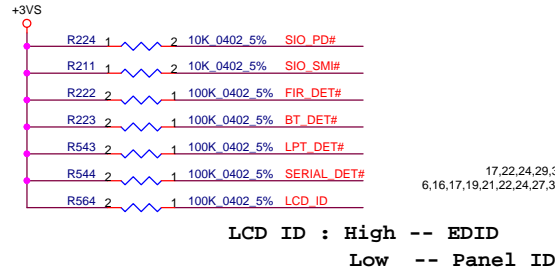
## HeadPhone JACK



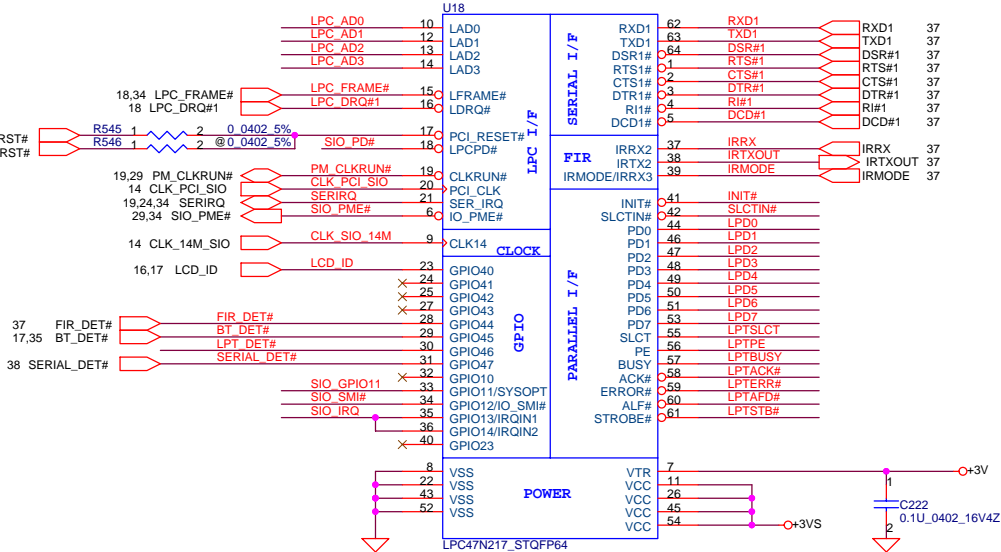
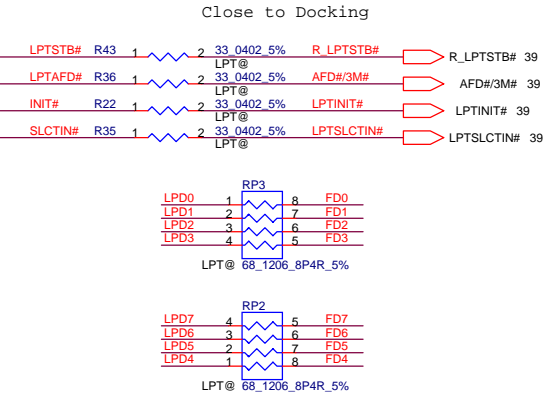


SUPER I/O SMsC LPC47N217

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No Docking and Parallel Port ----->Del

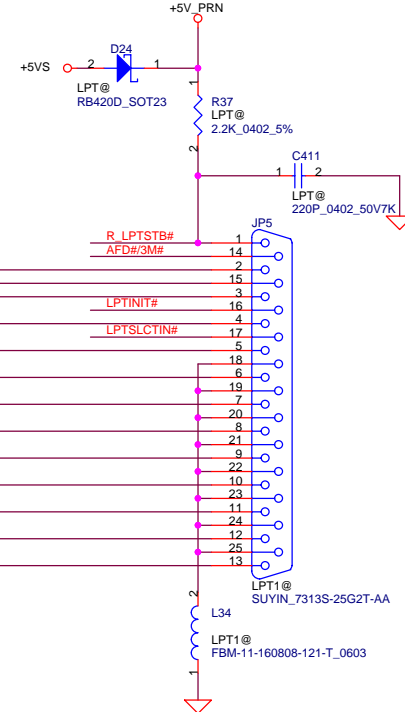
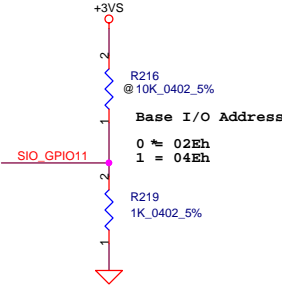
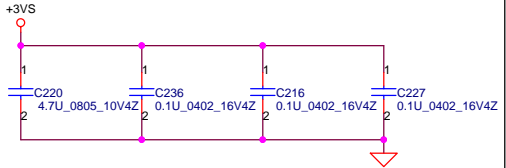
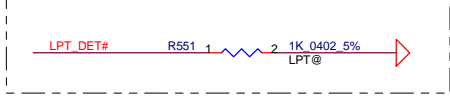


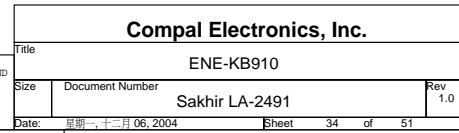
Parallel Port

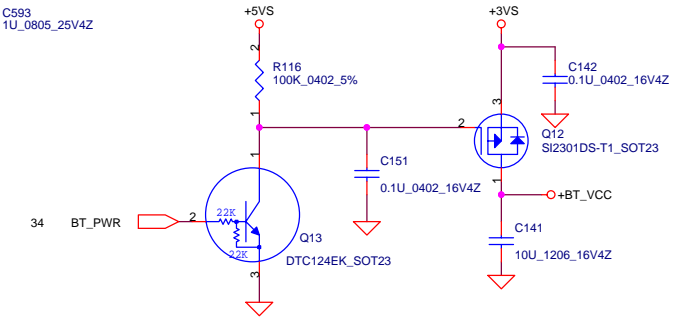
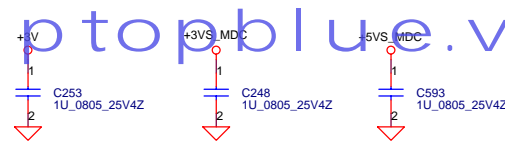
LPT Module

L: R POP LPT Enable

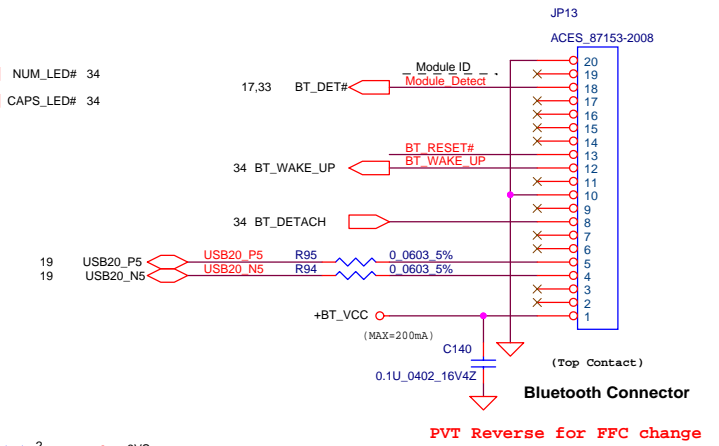
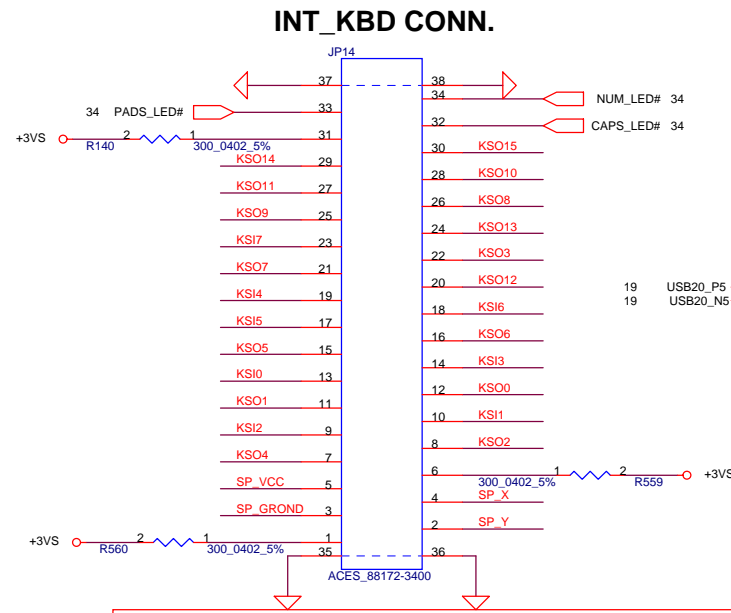
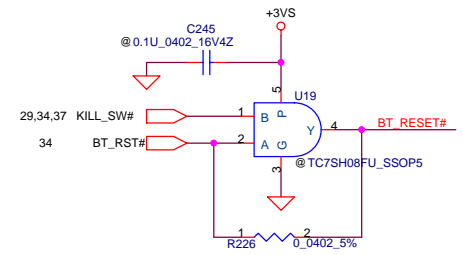
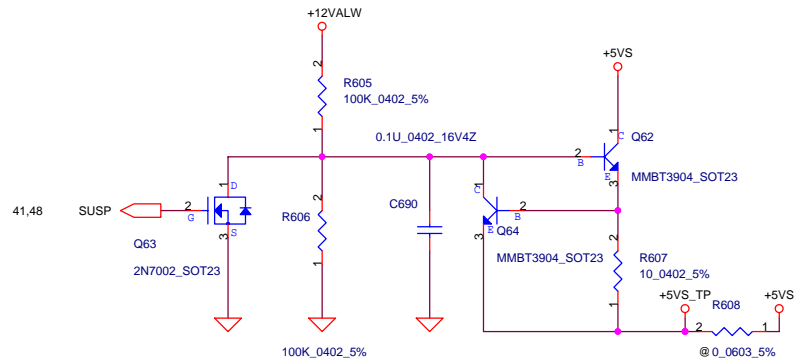
H: R De-POP LPT Disable







Module ID  
Indication for polarity of reset  
Reset input High Active --> Low ,  
Reset input Low Active --> Open



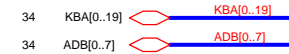
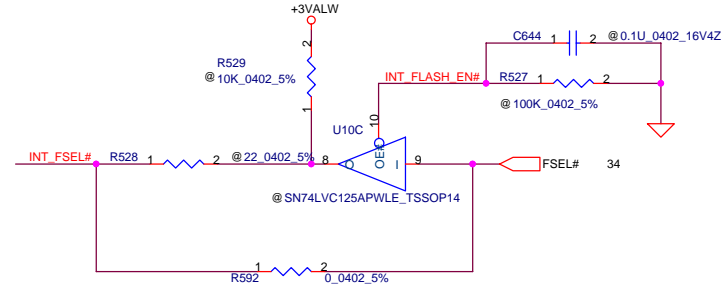
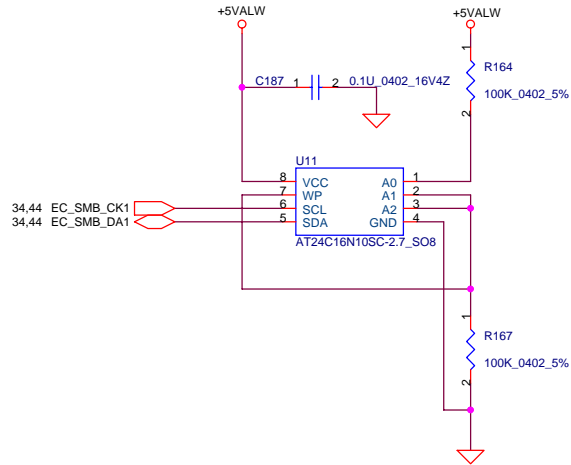
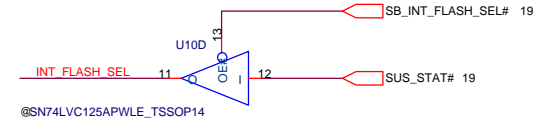
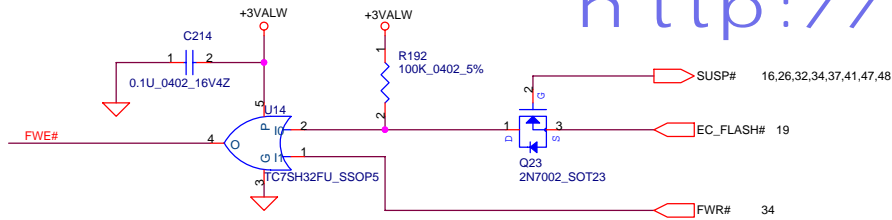
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MDC / BT / KBD / TP

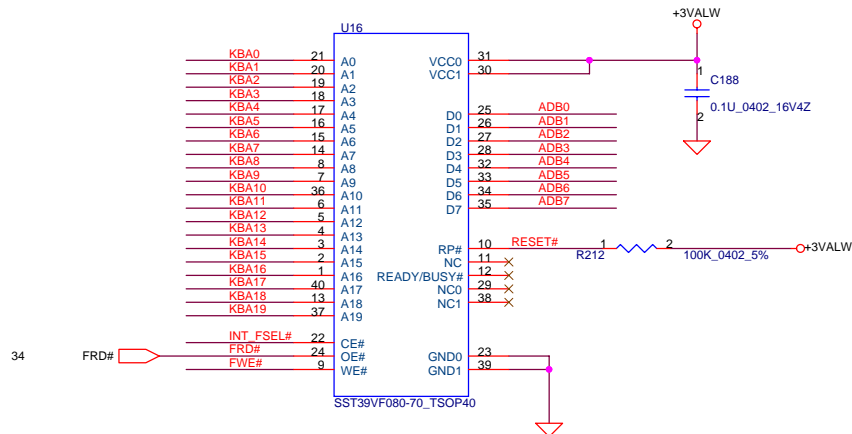
**Sakhir LA-2491**

10

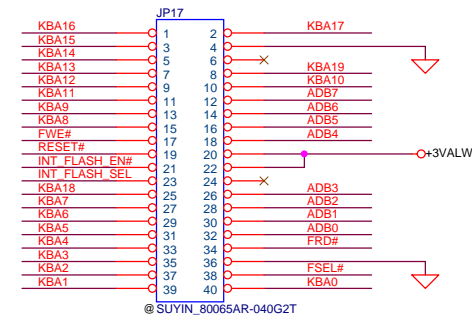
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## 1MB Flash ROM



## 1MB ROM Socket






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Title		BIOS & EXT. I/O PORT	
Revision		Sakhir LA-2491	
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Date		Sheet 36 of 51	

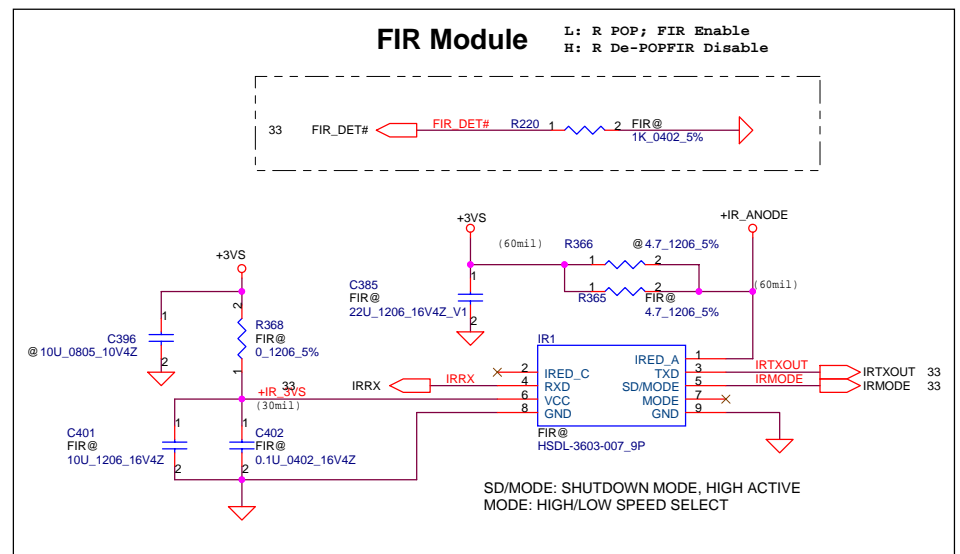
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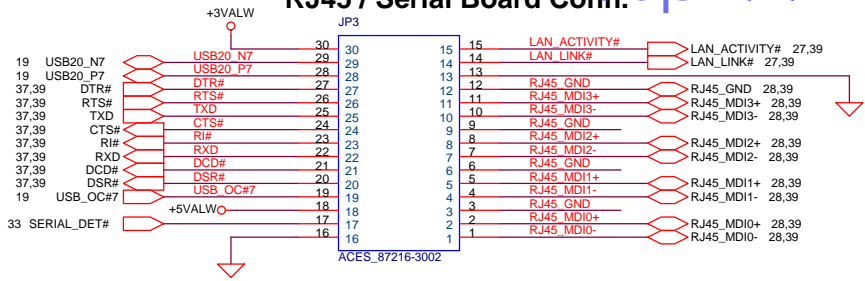
## FIR Module

33 FIR\_DET#  FIR\_DET# R220 1  2 FIR@ 1K\_0402\_5% 

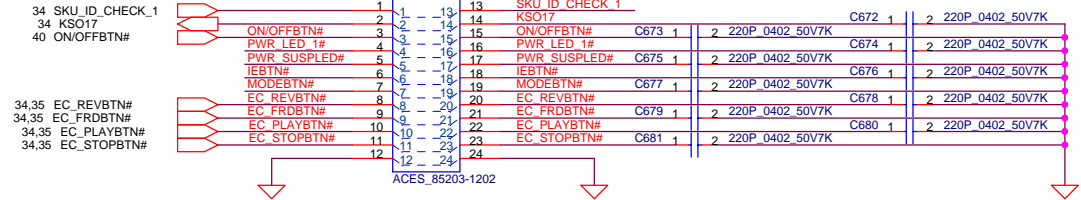


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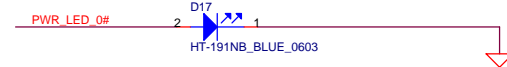
## RJ45 / Serial Board Conn.



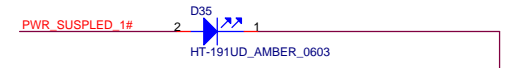
## Power / LED Board Conn.



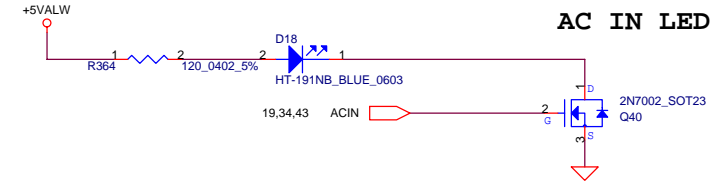
## POWER/ON LED



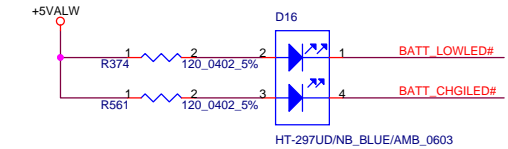
## POWER/SUSP LED



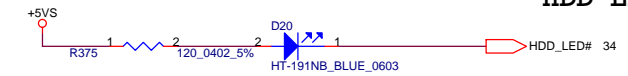
## AC IN LED



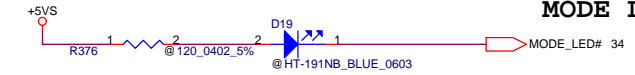
## BATTERY CHG



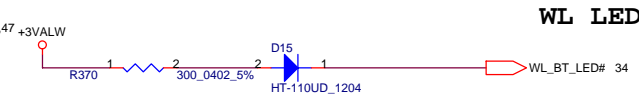
## HDD LED



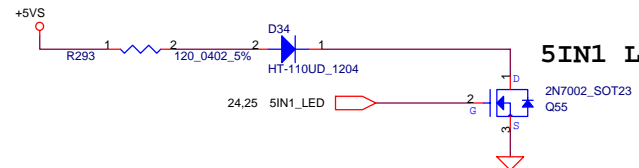
## MODE LED



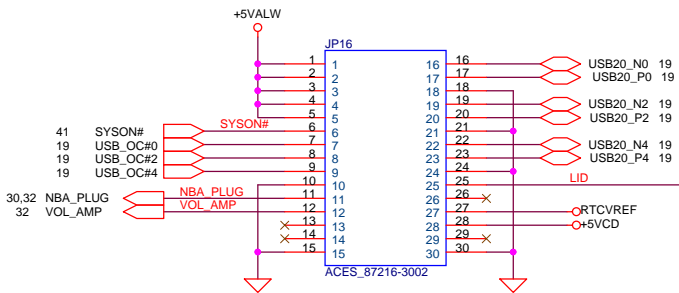
## WL LED



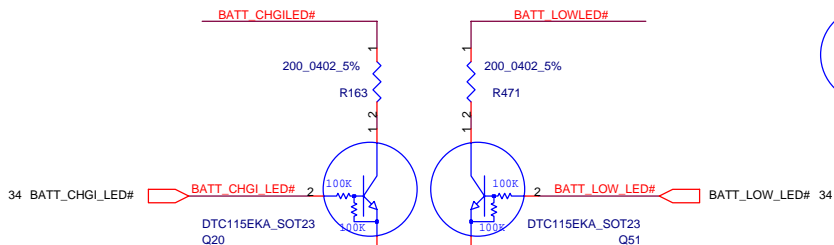
## 5IN1 LED



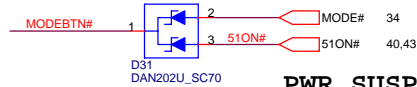
## USB Board Conn.



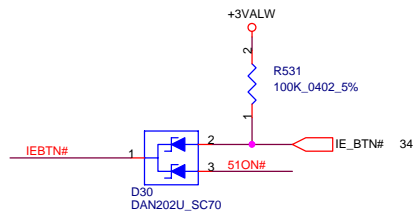
## BATTERY CHG/Low LED



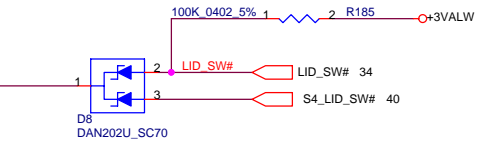
## PWR SUSP LED



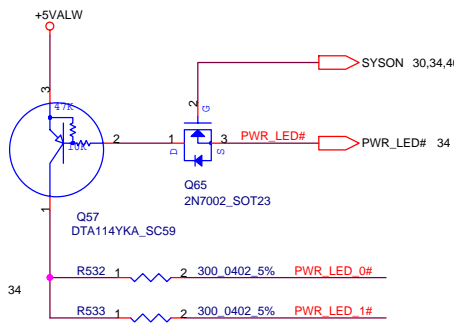
## IEBTN#



## LID SW#



## PWR\_LED#



## Compal Electronics, Inc.

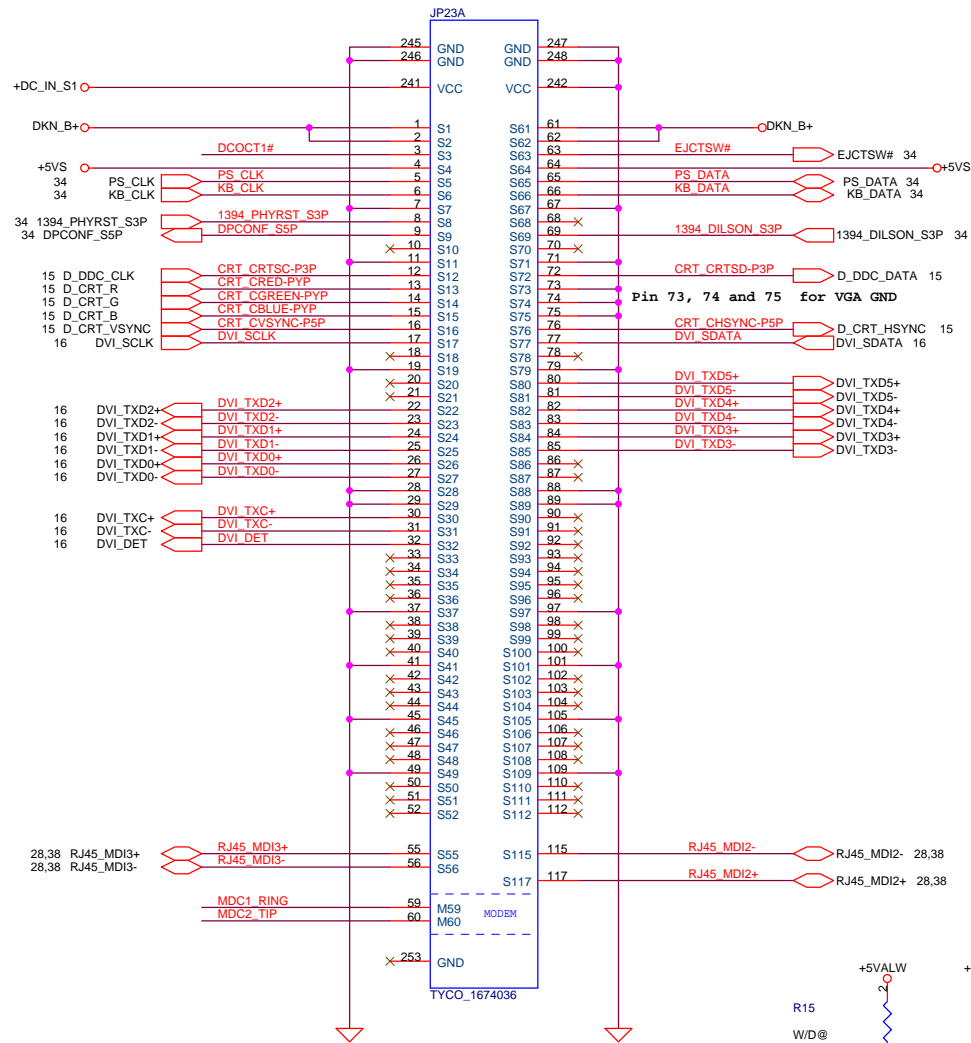
### Switches & LED

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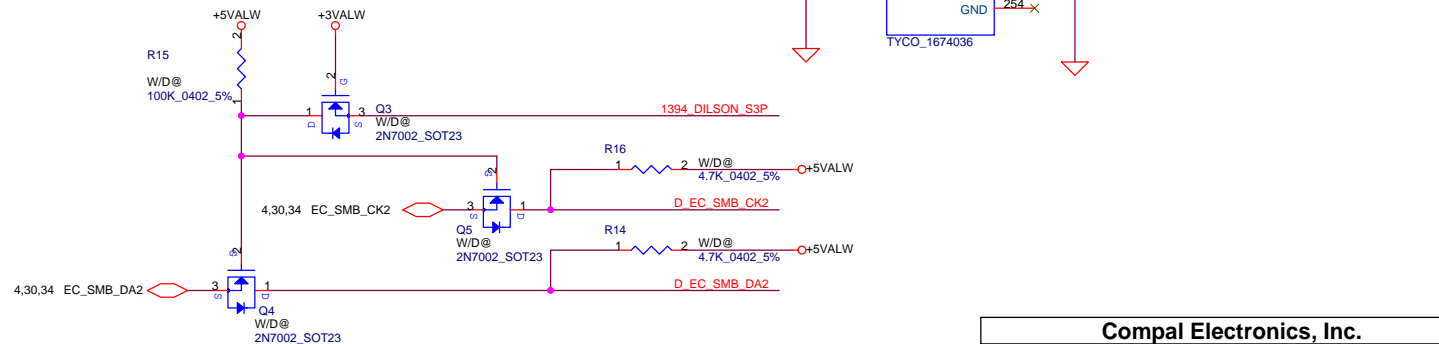
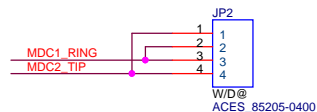
Title	Switches & LED	
Rev	1.0	
Date	星期二, 十二月 06, 2004	
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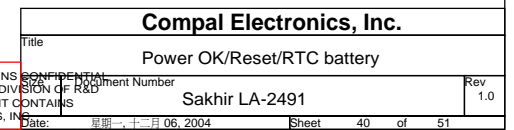


## Docking Conn.

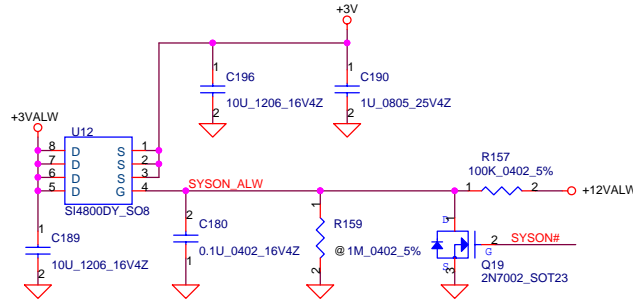


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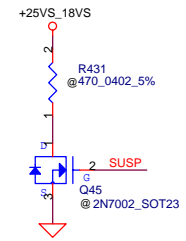
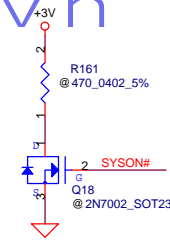
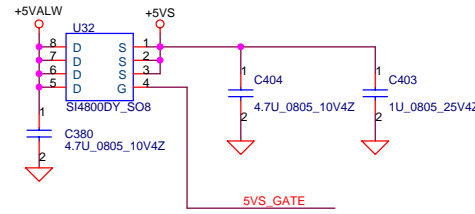




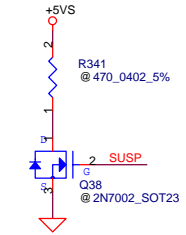
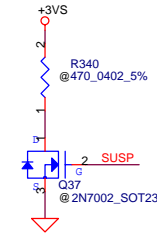
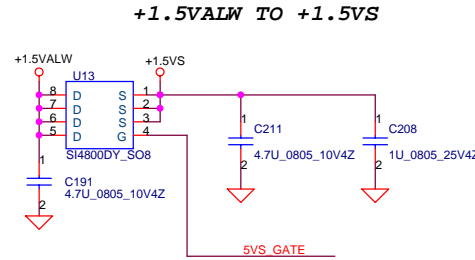
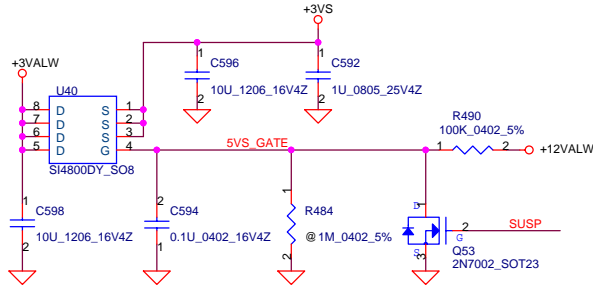
### +3VALW TO +3V



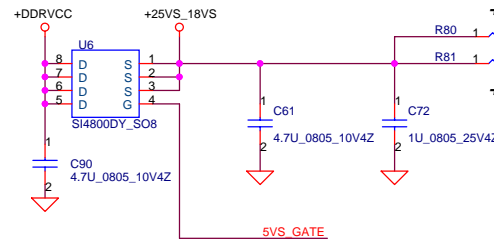
### +5VALW TO +5VS



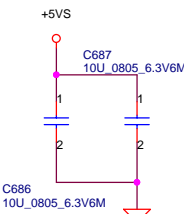
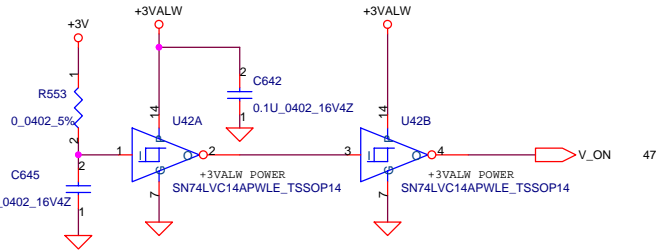
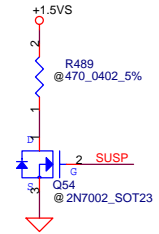
### +3VALW TO +3VS



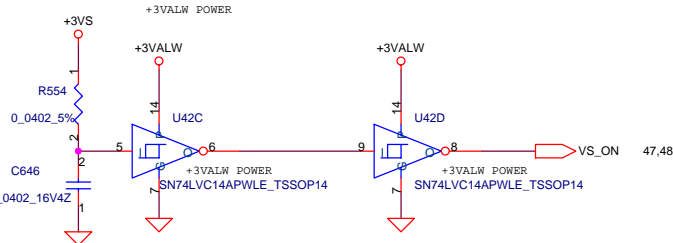
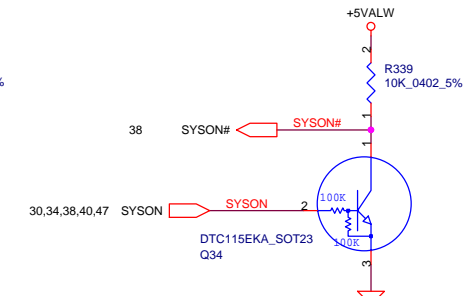
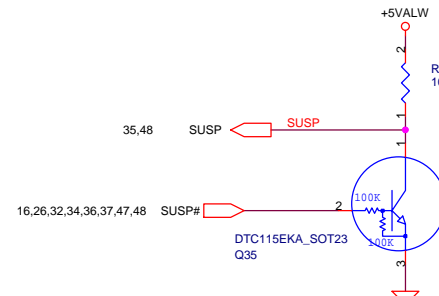
### +2.5V TO +2.5VS (DDR1)



### +1.8V TO +1.8VS (DDR2)



In CUP side



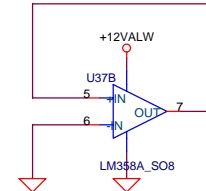
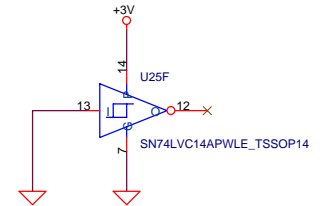
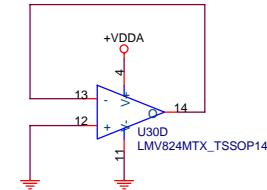
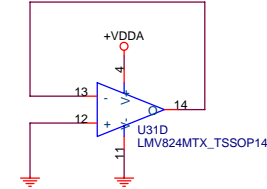
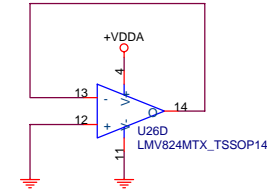
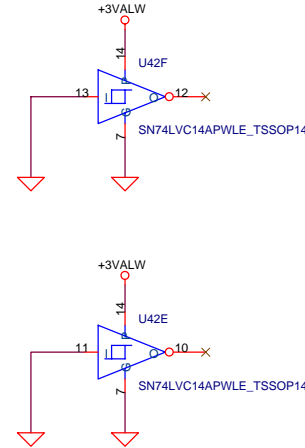
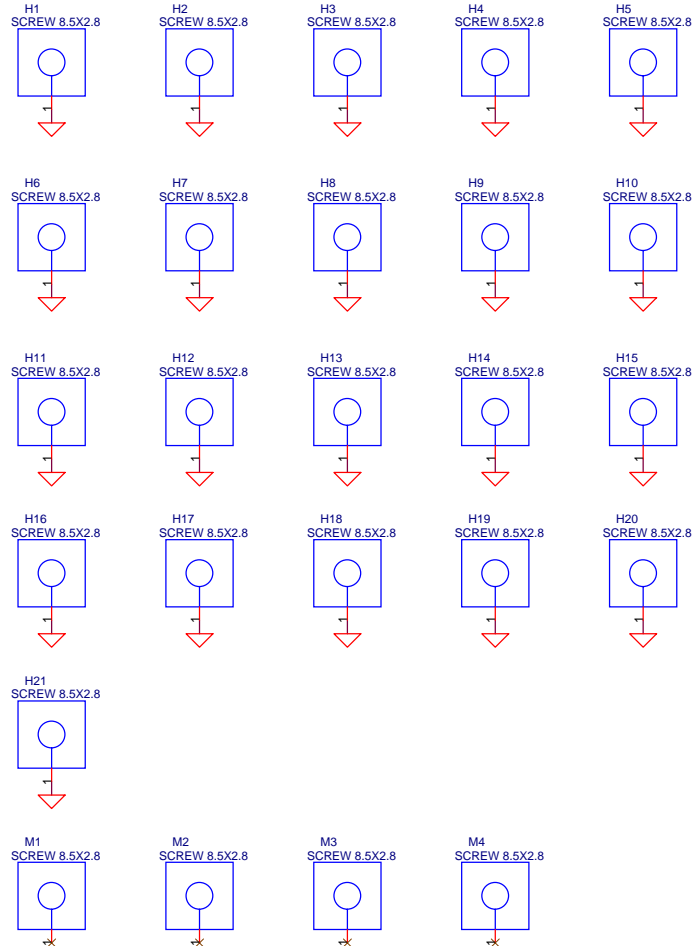
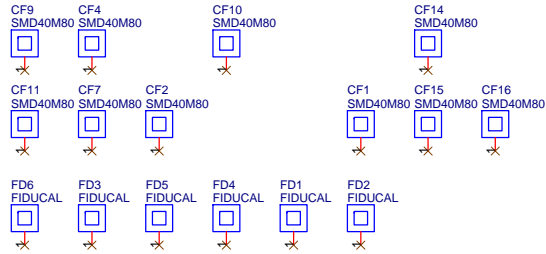
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POWER CONTROL CKT

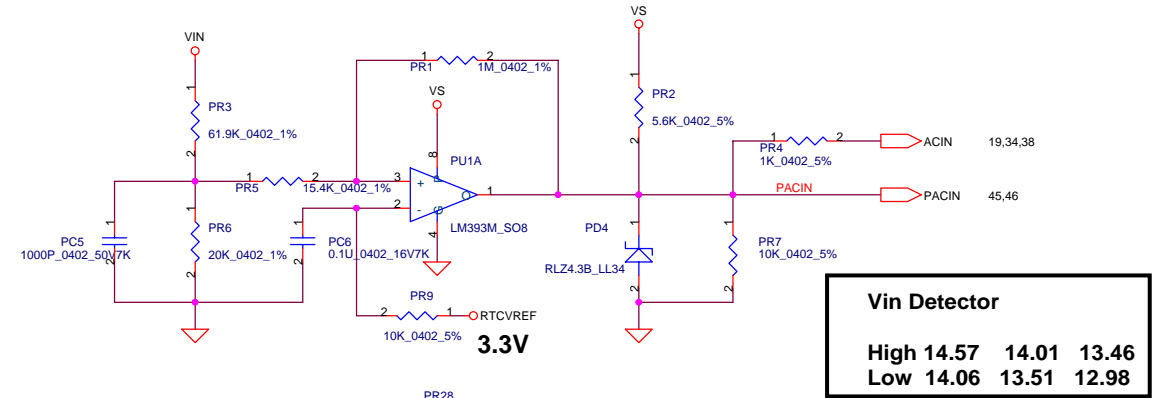
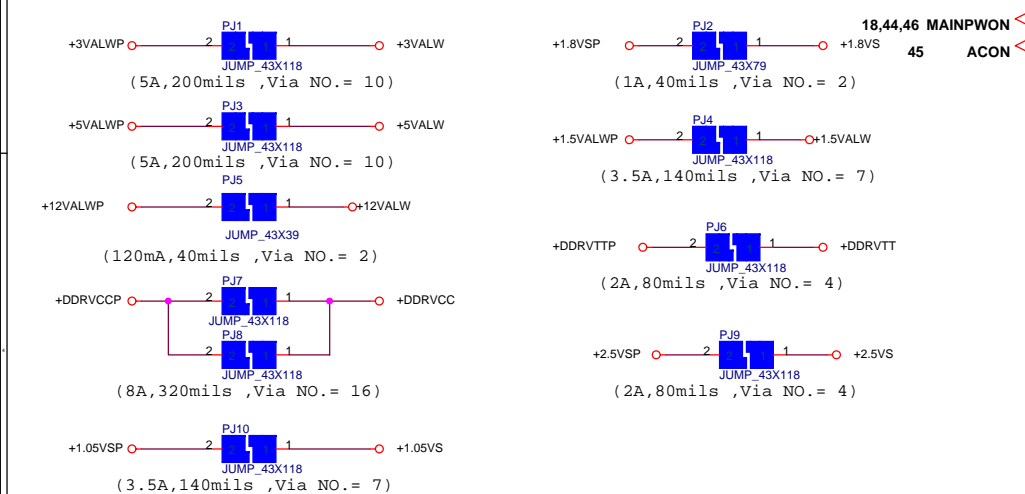
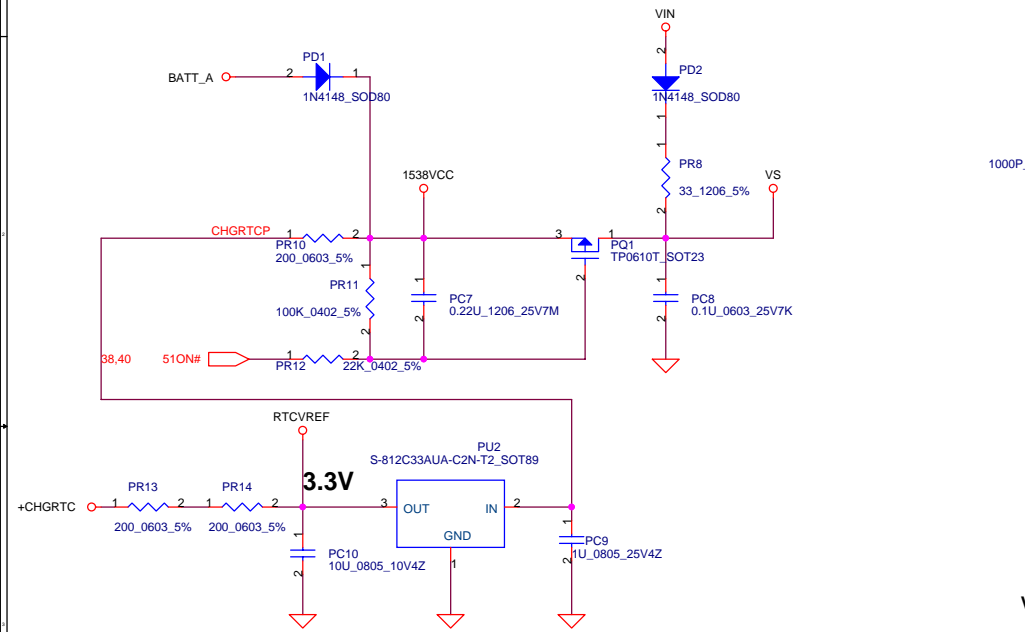
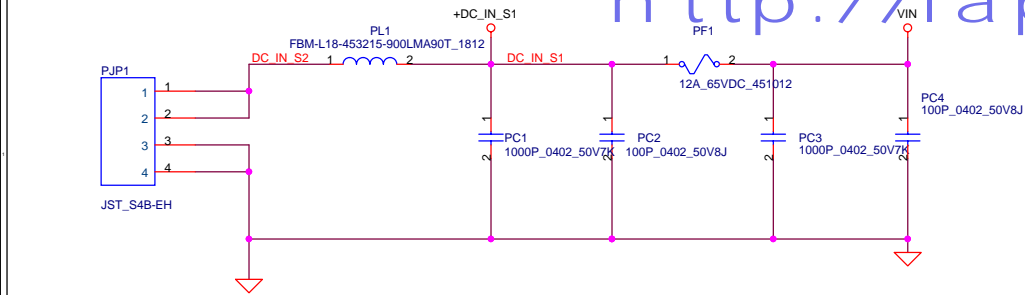
Size B	Document Number	Rev 1.0
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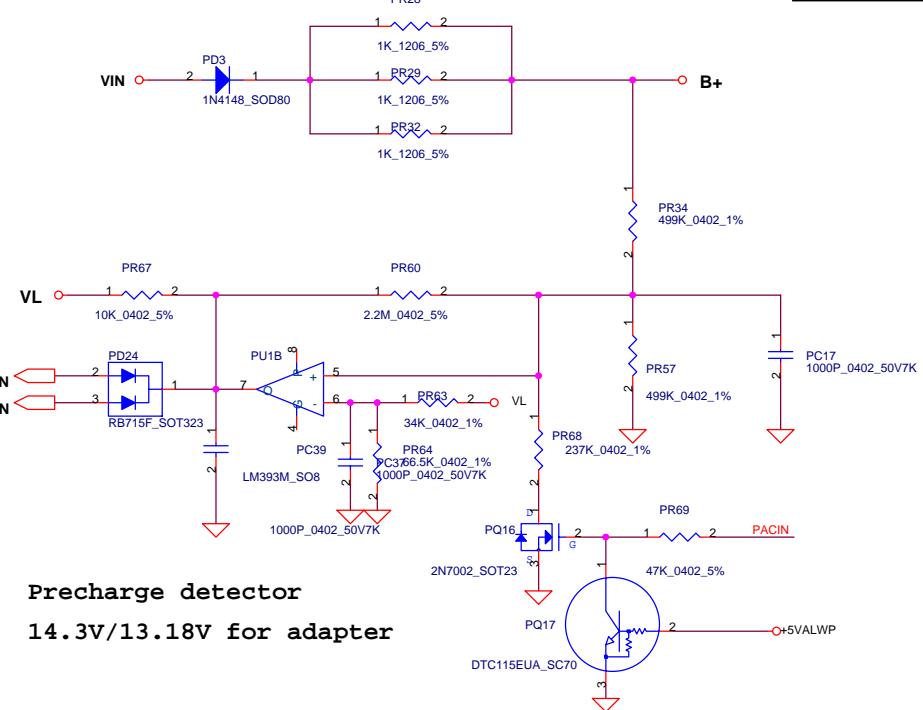


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Compal Electronics, Inc.			
Title		Screws	
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Vin Detector			
High	14.57	14.01	13.46
Low	14.06	13.51	12.98

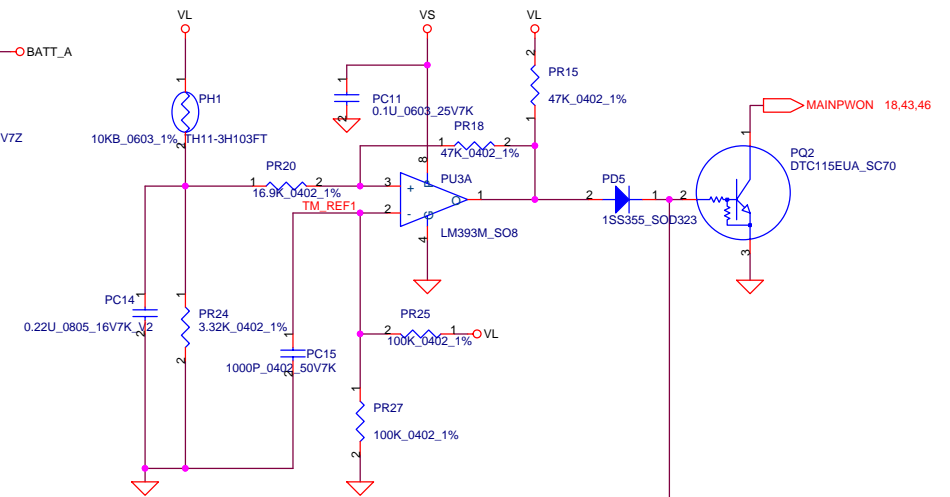
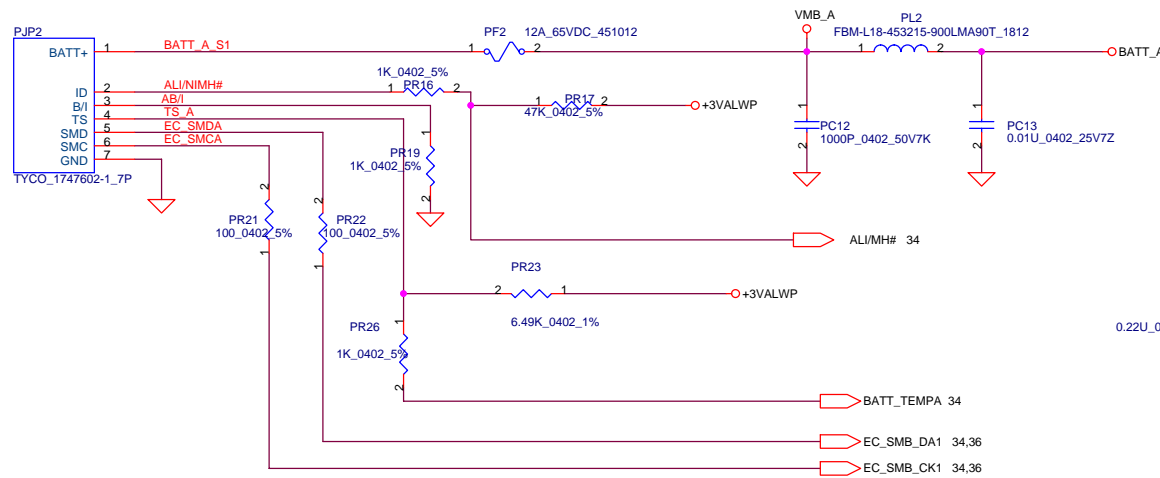


**Precharge detector**  
14.3V/13.18V for adapter

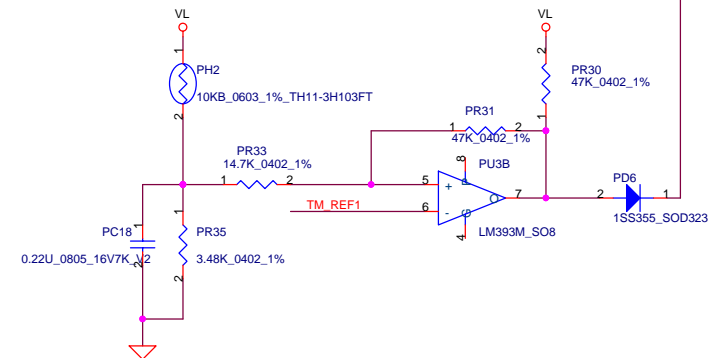
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Compal Electronics, Inc.			
Title <b>DCIN &amp; DETECTOR</b>			
Size	Document Number <b>Sakhir LA-2491</b>	Rev 1.0	
Date	星期二, 十二月 06, 2004	Sheet	43 of 51

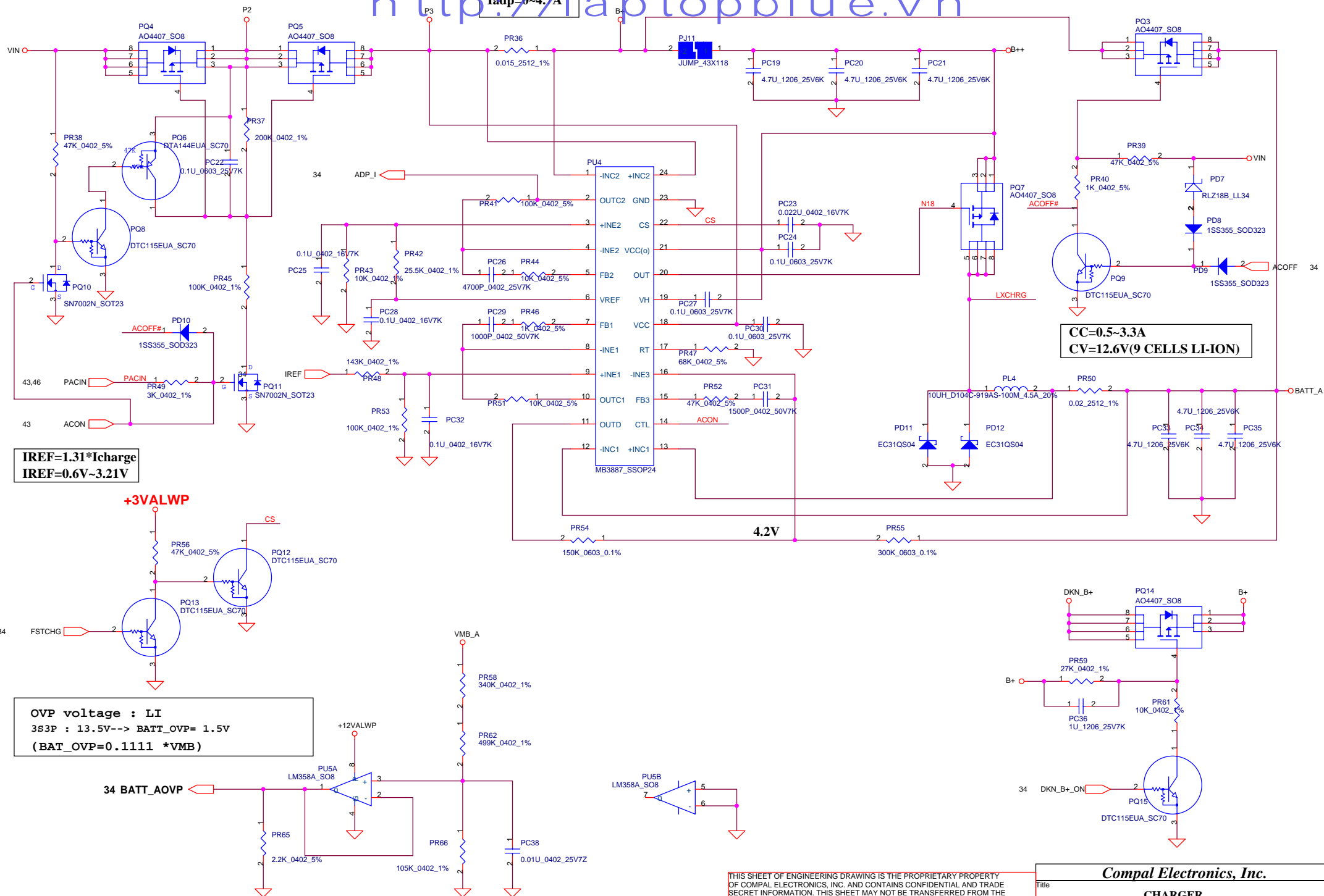
**PH1 under CPU botten side :**  
CPU thermal protection at 84 degree C  
Recovery at 45 degree C



**PH2 near main Battery CONN :**  
BAT. thermal protection at 79 degree C  
Recovery at 45 degree C



I<sub>adp</sub>=0~4.7A



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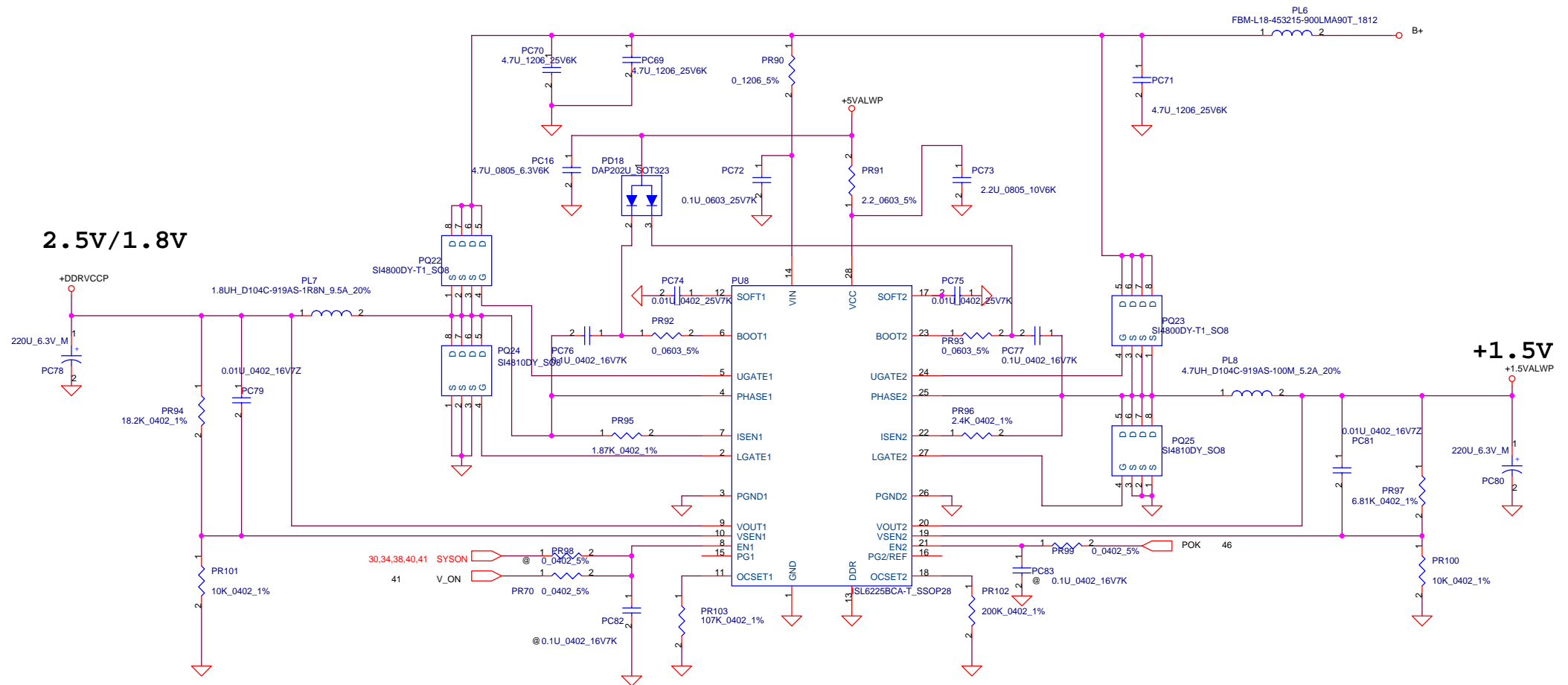
**Compal Electronics, Inc.**

Title				
CHARGER				
Size	Document Number			Rev
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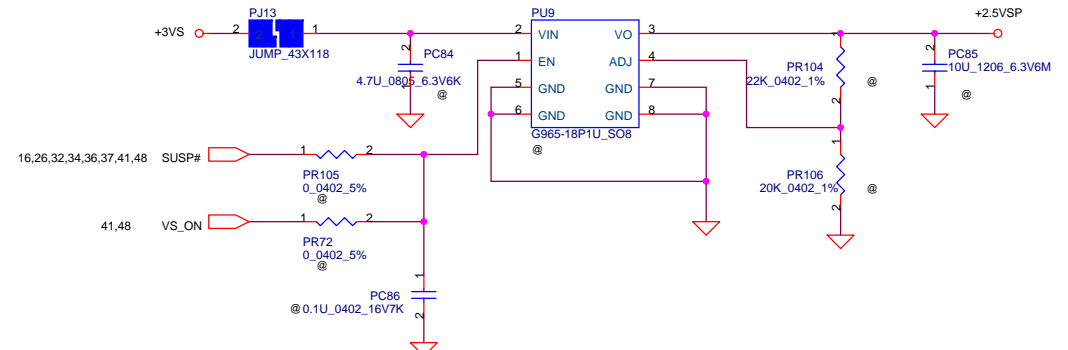


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Title			
5V/3.3V/12V			
Size	Document Number		Rev
	Sakhr LA-2491		1.0
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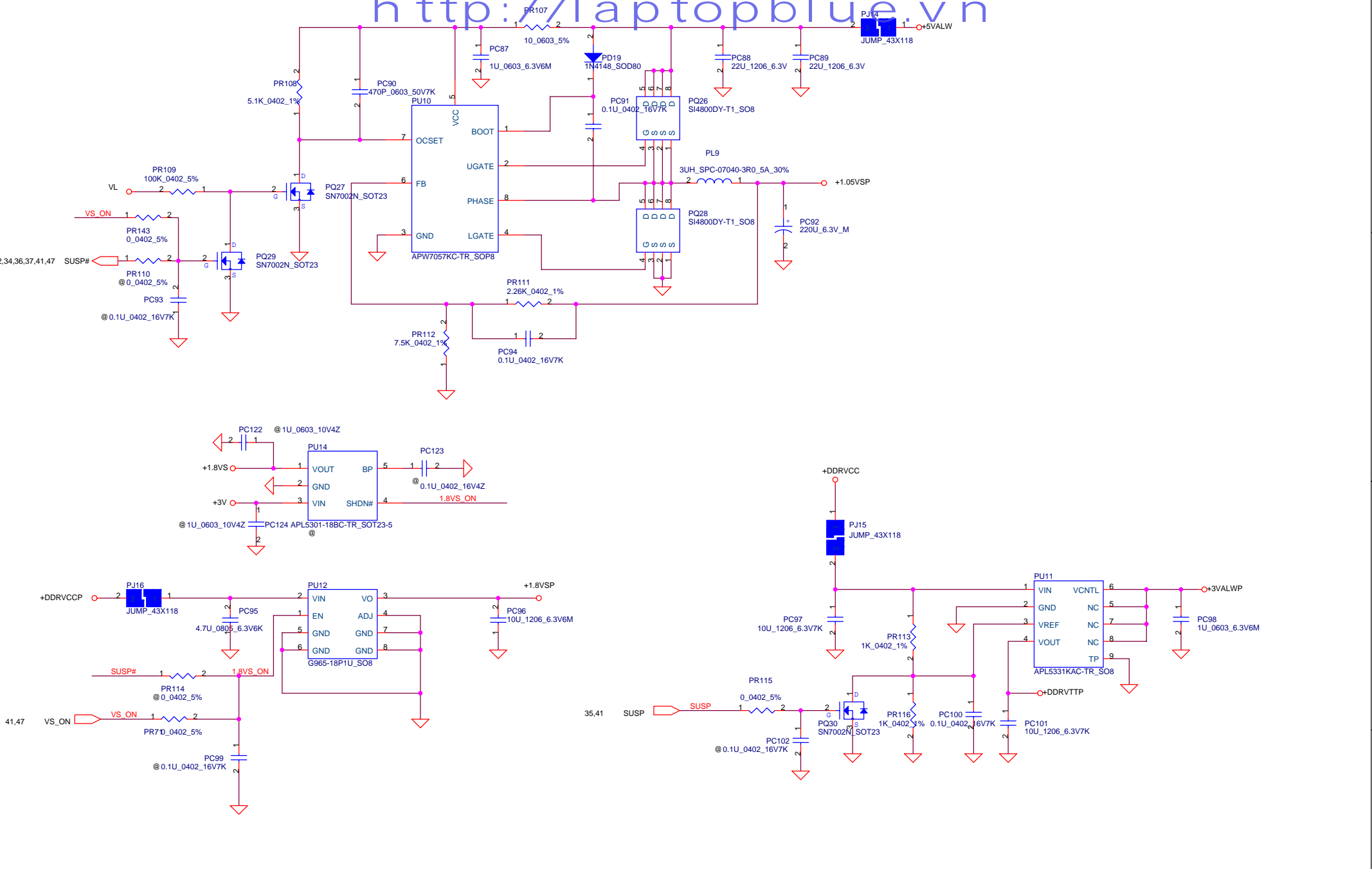


	PR94	UNPOP
DDRI	18.2K_0402_1% (2.5V)	PU9, PC84, PR105, PR104, PR106, PC85
DDRII	10K_0402_1% (1.8V)	PU12, PC95, PR114, PC96



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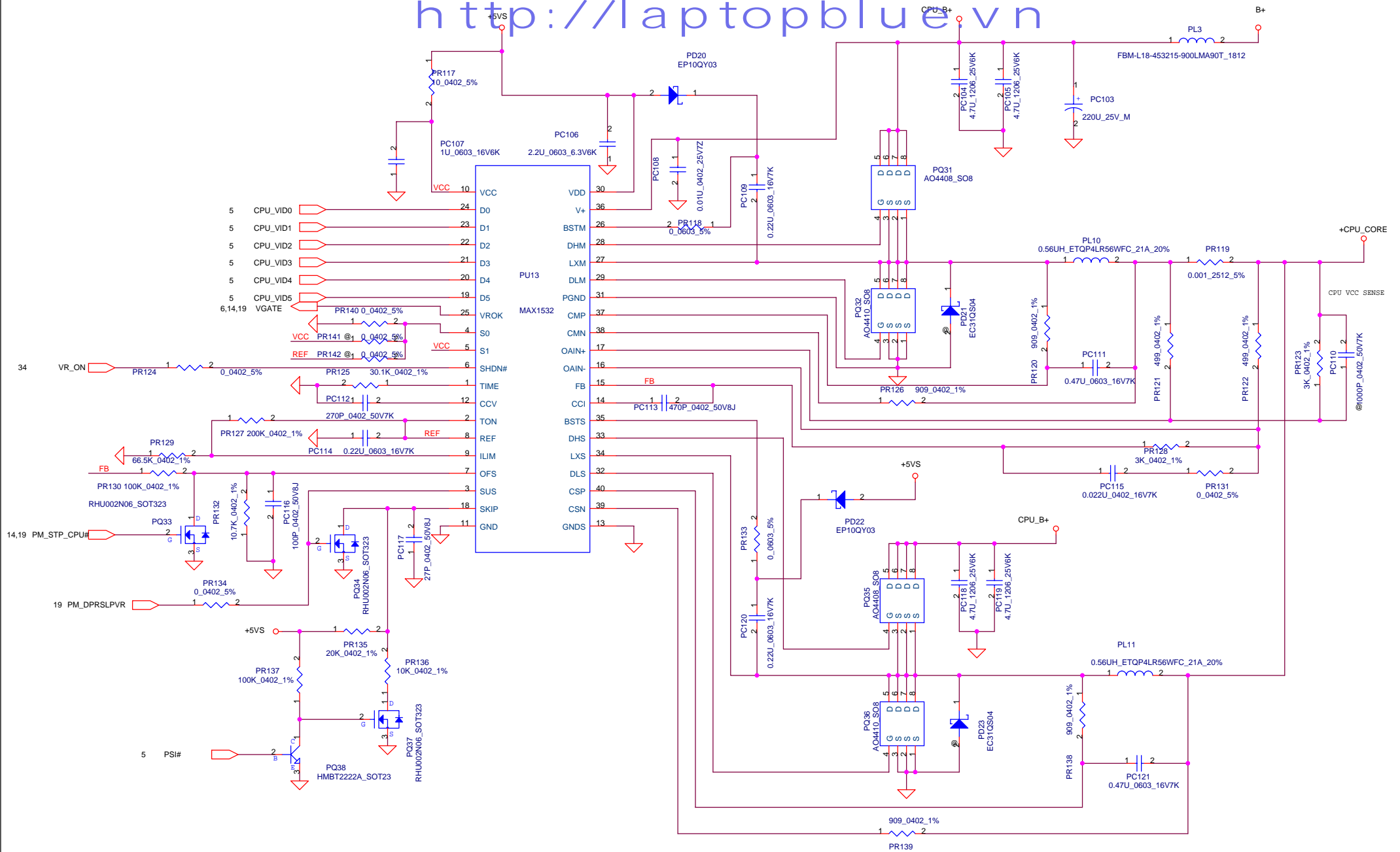
Compal Electronics, Inc.			
Title		DDRVCC/1.5V/2.5V	
Size	Document Number	Sakhir LA-2491	
Date:	星期一, 十二月 06, 2004	Sheet	47 of 51
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Compal Electronics, Inc.		
Title		
1.05V/1.8V/DDRVTT		
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CPU\_CORE

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\*\*\*\*\* Rev:0.3 PIR List 2004/10/26 Writer by Sam Tsai \*\*\*\*\*

Intel Recommend

Power Team testing OK

Intel Recommend

RGB without Docking  
EMI  
EMI

### LCDVDD Soft-Start

Intel Recommend

Intel Recommend

Intel Recommend

Intel Recomm

SWDJ testing

TI Recommend

## 11 Recommend

Marvwl Recom

Design Change

Intel Recommend

Power Team testing OK

Intel Recommend

RGB without Docking  
EMI  
EMI

### LCDVDD Soft-Start

Intel Recommend

Intel Recommend

Intel Recomm

SWDJ testing

TI Recommend

## 1.1 Recommendation

Marvwl Recom

Design Change

Design Change

EMI

2002-2003

EMI

Design Change

ON20 0000119

Design Change

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PIR			
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*List ) for Power Circuit*

DD