

# ***PWWAA***

## ***Marseille LC***

# **L-A6841P REV 0.1 Schematic**

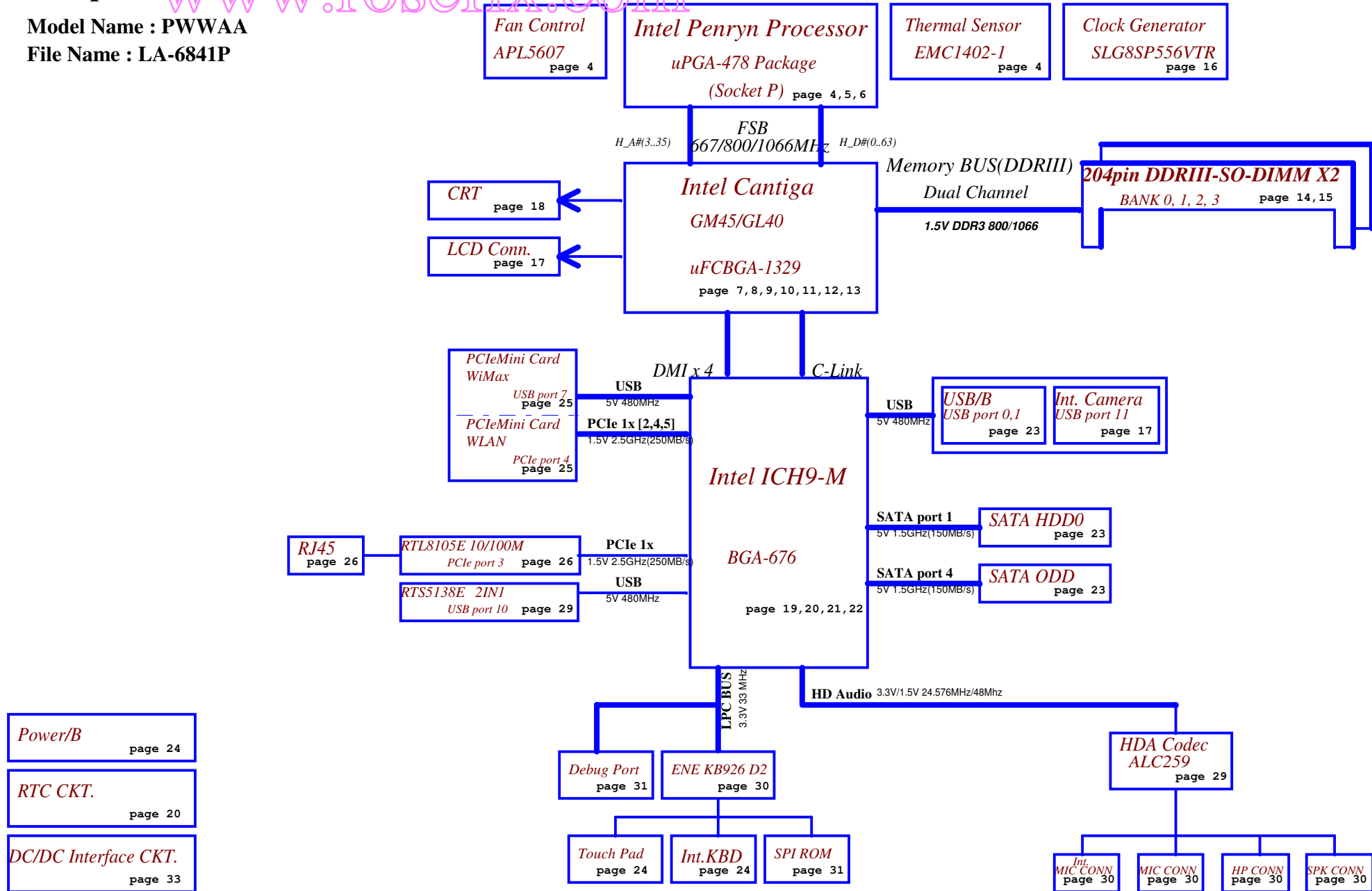
Intel Penryn/ Cantiga/ ICH9M  
2010-07-22 Rev. 0.1

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				PWWAA LA6841P M/B	

# Compal Confidential

Model Name : PWWAA

File Name : LA-6841P



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## Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5 power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for SB	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

## BTO Option Table

Function	Card Reader	Camera	WLAN	Energy Star
description		(X)	Always	Always
explain		Camera	WLAN	Energy Star
BTO		CAM@	WLAN@	

## External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
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## EC SM Bus1 address

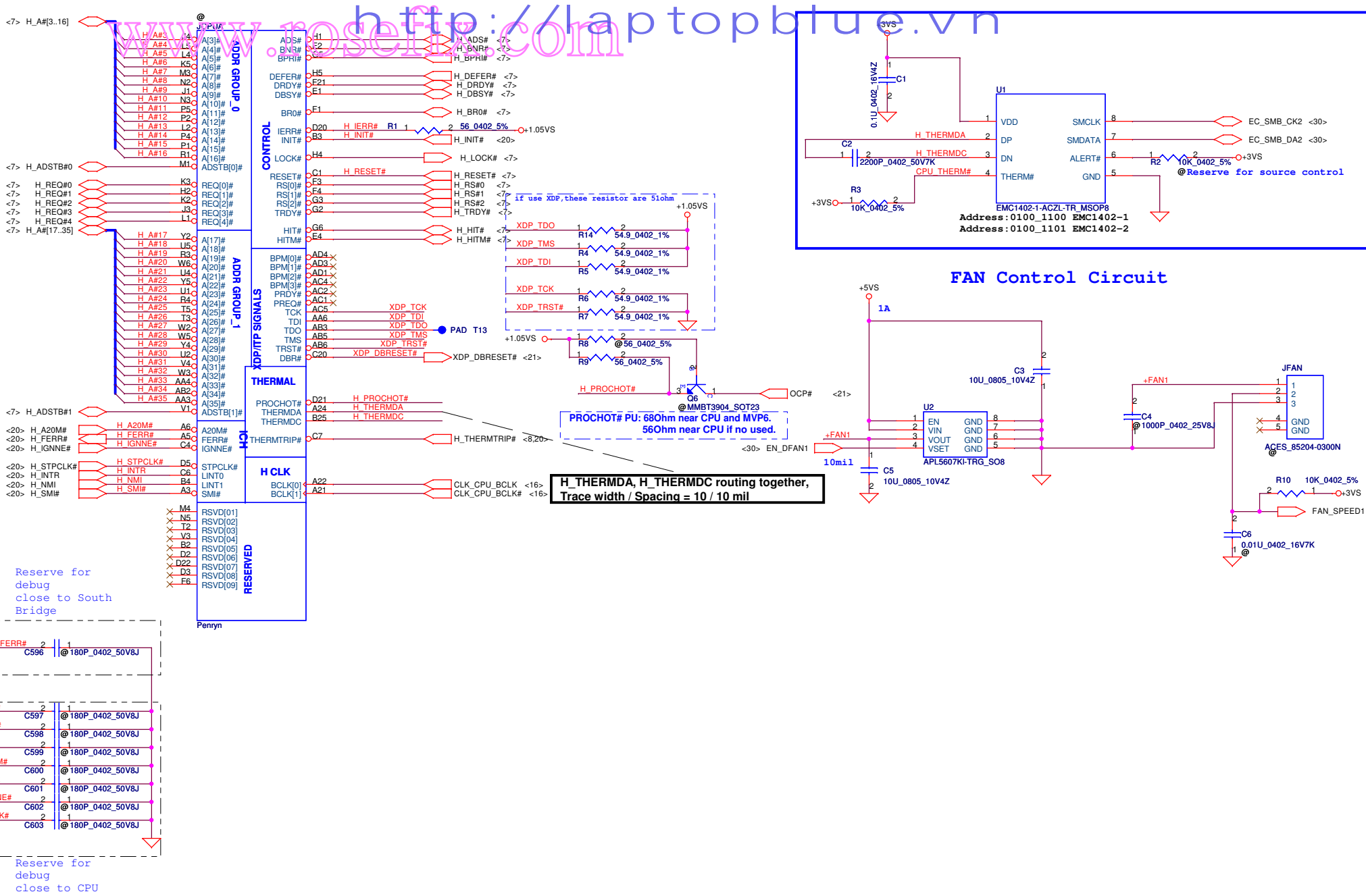
## EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D2		+3VS	EC KB926 D2	
+3VL	Smart Battery	0001 011X b	+3VS	CPU THM Sen	1001 101Xb
				SMSC SMC1402	

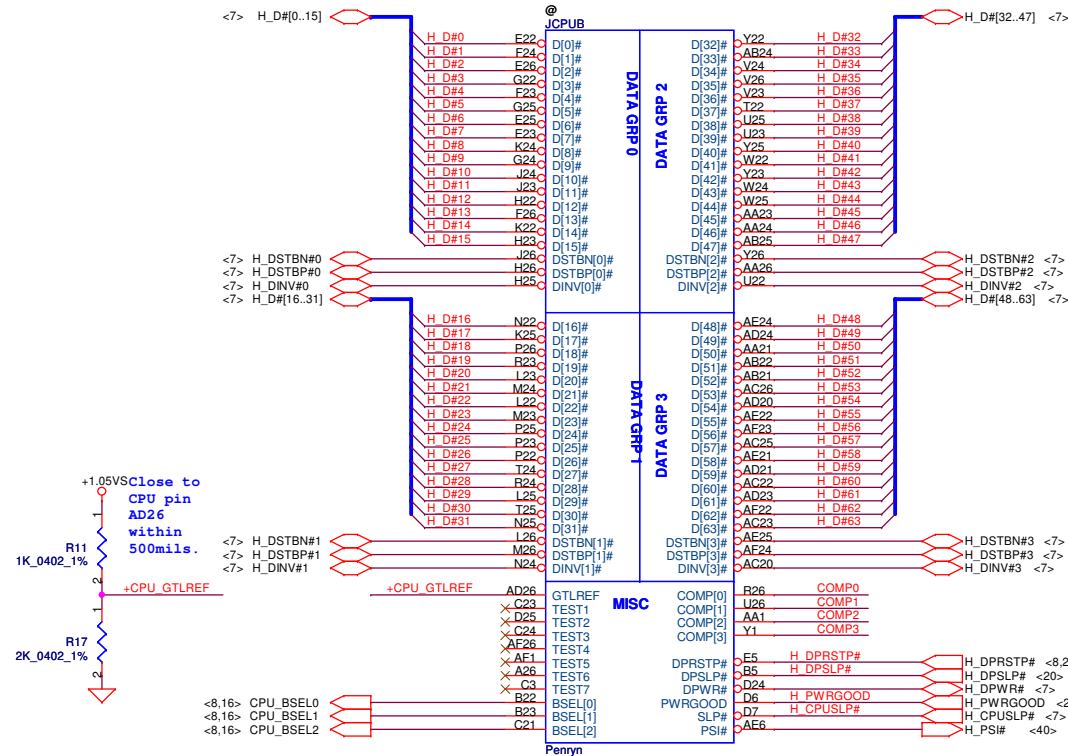
## ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb

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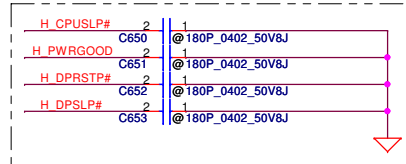


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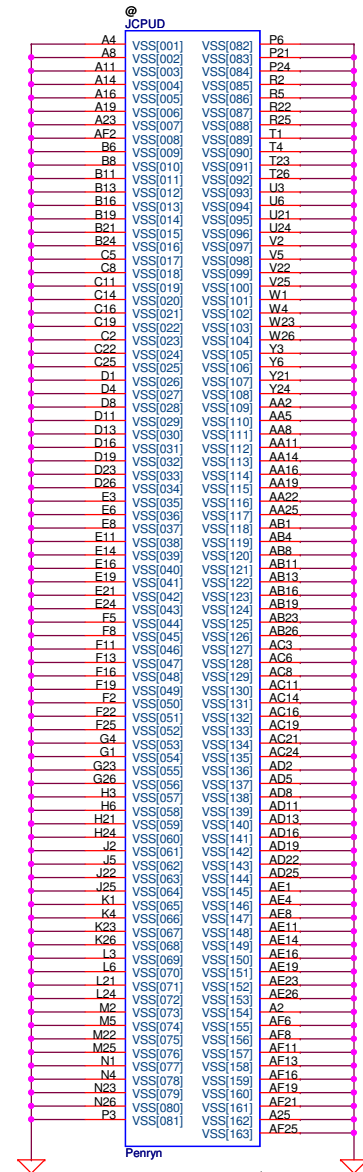


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



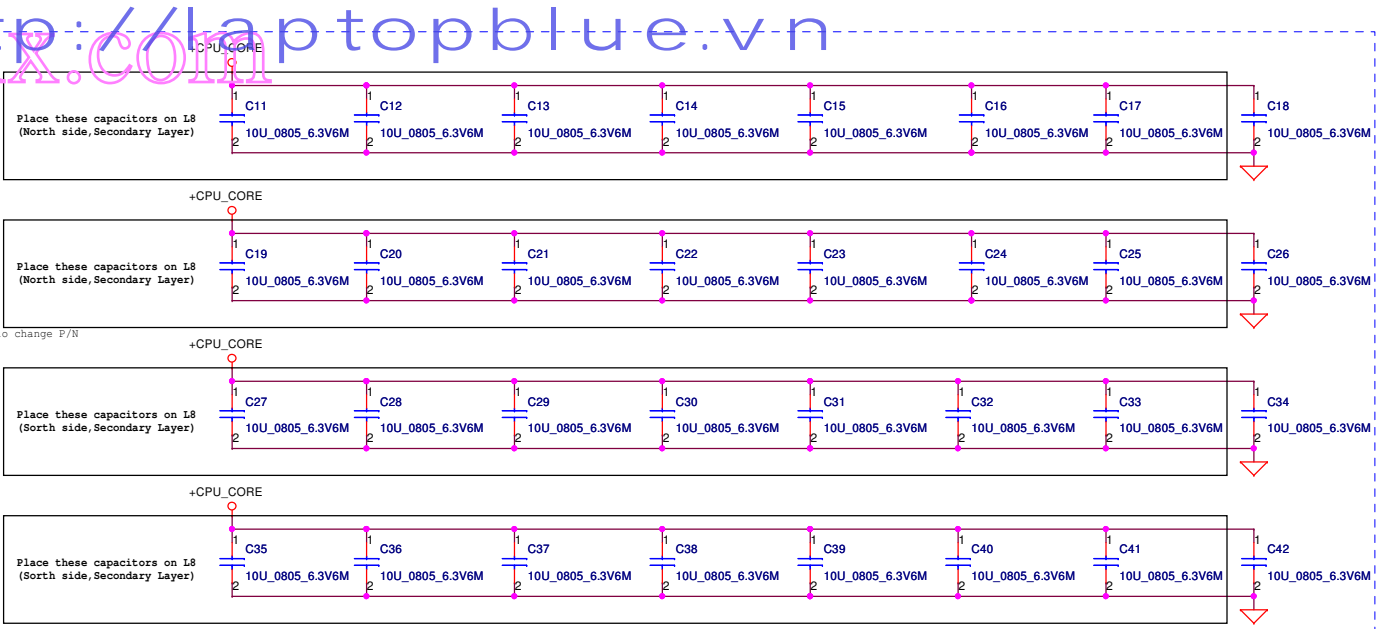
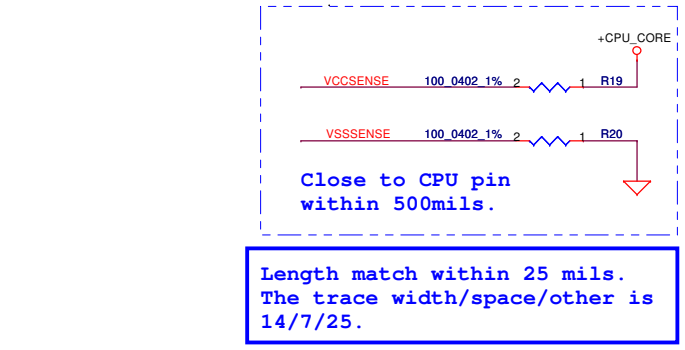
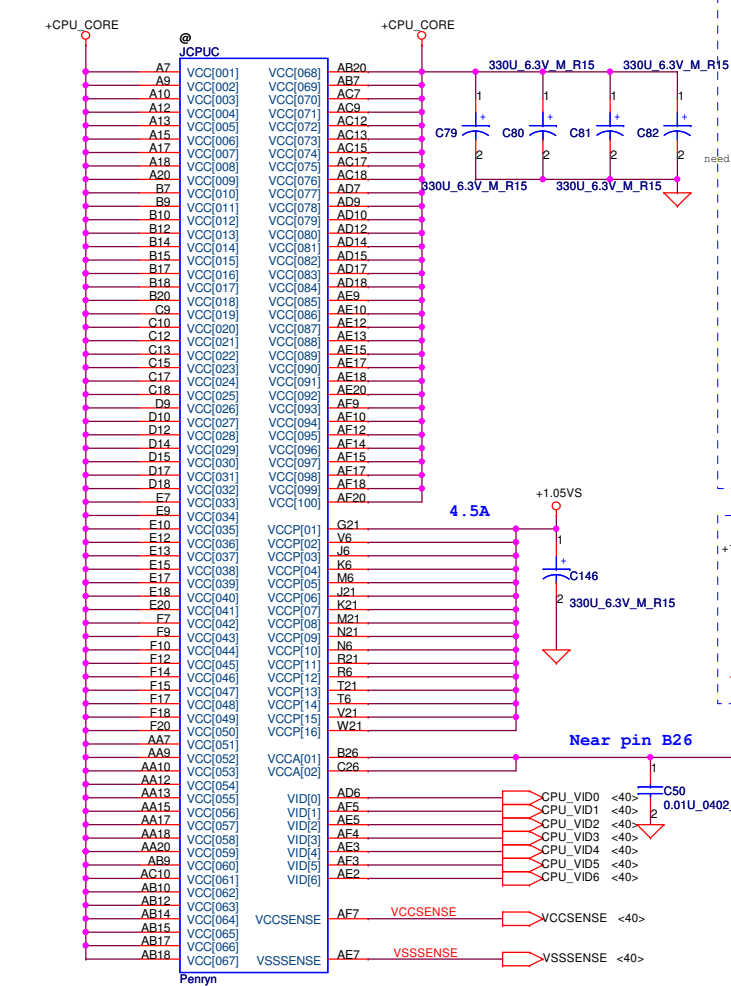
Reserve for debug close to CPU



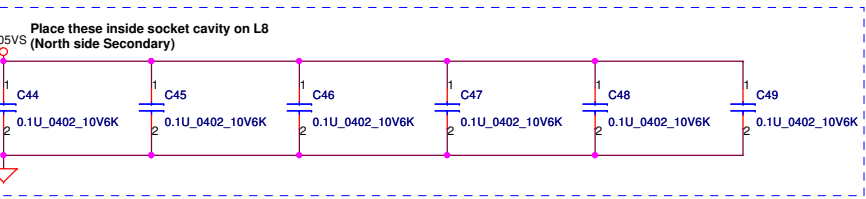
layout note: Please use "Daisy Chain" to layout and the signal (H\_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

Near CPU CORE regulator

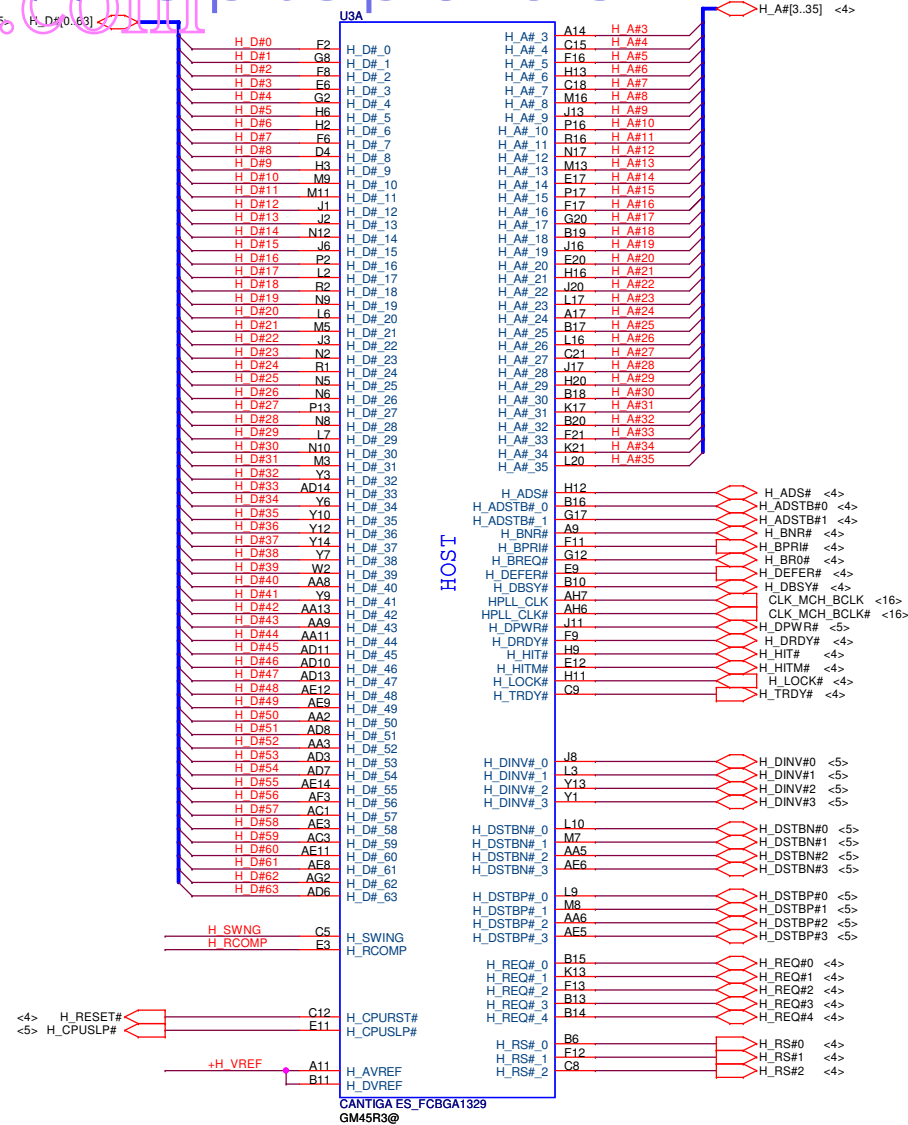
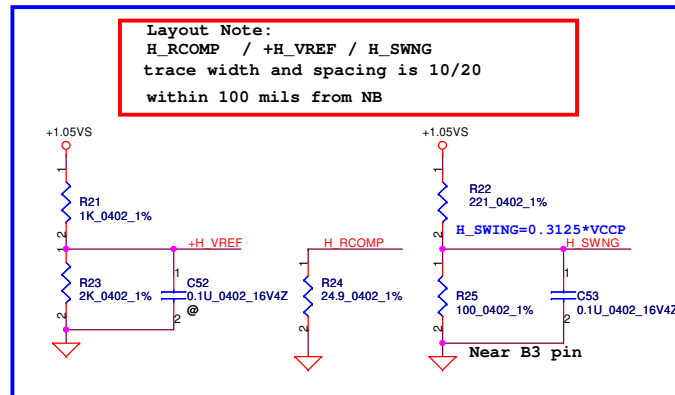
ESR <= 1.5m ohm  
Capacitor > 1980uF



Mid Frequency Decoupling

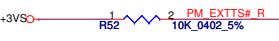
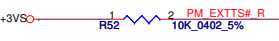


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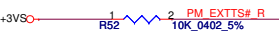
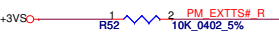
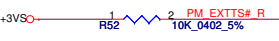
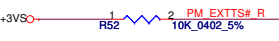
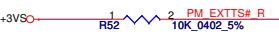
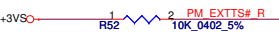


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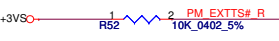


1 2 PM EXTTS# R  
R52 10K\_0402\_5%



1 2 PM EXTTS# R  
R52 10K\_0402\_5%

1 2 PM EXTTS# R  
R52 10K\_0402\_5%



1 2 PM EXTTS# R  
R52 10K\_0402\_5%

1 2 PM EXTTS# R  
R52 10K\_0402\_5%

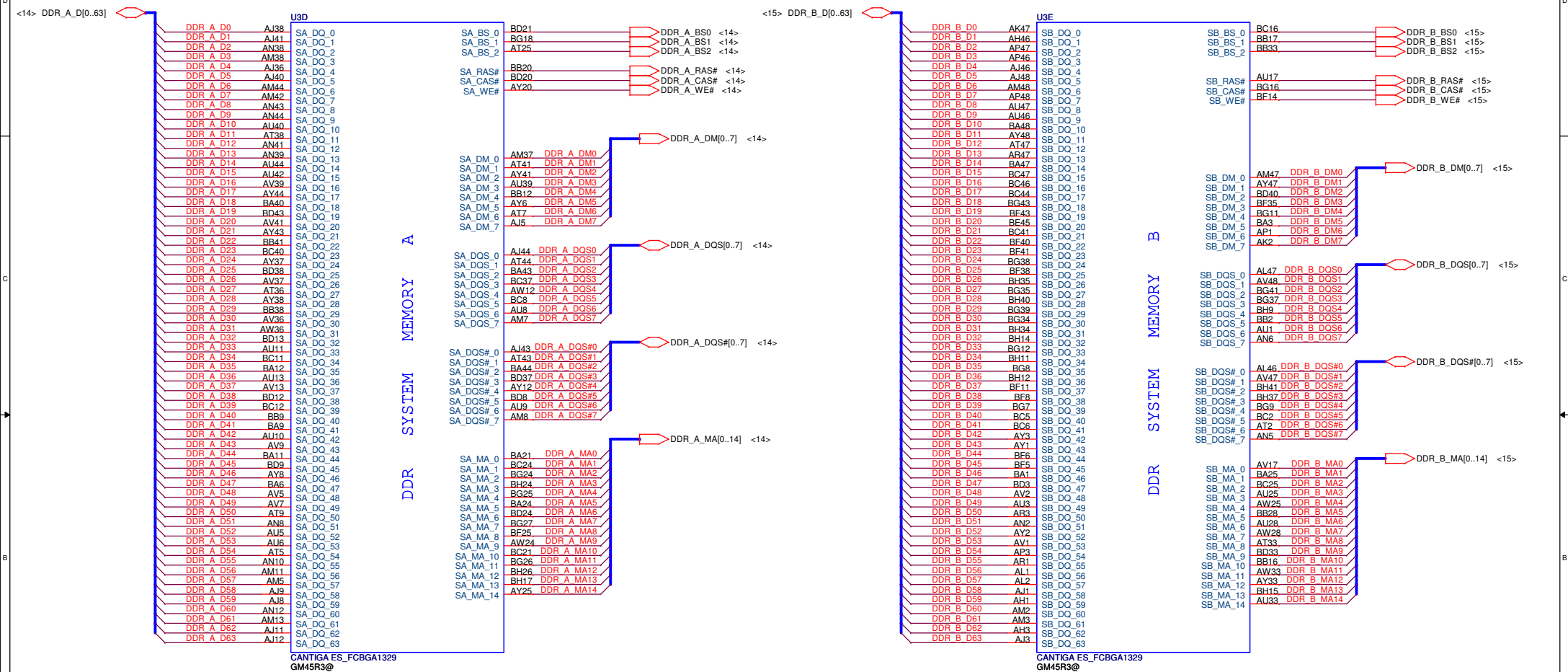
1 2 PM EXTTS# R  
R52 10K\_0402\_5%

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R52 10K\_0402\_5%





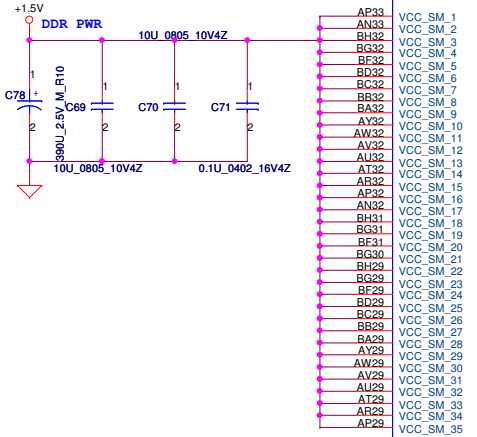
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DDR2, 657mA, 2500mA  
DDR3, 870mA, 3000mA

Int. Graphic

Extna Graphic: 1210.34mA  
Integrated Graphic: 1930.4mA  
Intel Management Engine Link: 508.12mA



- VCC\_SM\_1
- VCC\_SM\_2
- VCC\_SM\_3
- VCC\_SM\_4
- VCC\_SM\_5
- VCC\_SM\_6
- VCC\_SM\_7
- VCC\_SM\_8
- VCC\_SM\_9
- VCC\_SM\_10
- VCC\_SM\_11
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- VCC\_SM\_14
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- VCC\_SM\_33
- VCC\_SM\_34
- VCC\_SM\_35

- VCC\_SM\_36/NC
- VCC\_SM\_37/NC
- VCC\_SM\_38/NC
- VCC\_SM\_39/NC
- VCC\_SM\_40/NC
- VCC\_SM\_41/NC
- VCC\_SM\_42/NC

- VCC\_AXG\_1
- VCC\_AXG\_2
- VCC\_AXG\_3
- VCC\_AXG\_4
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- VCC\_AXG\_41
- VCC\_AXG\_42

PAD T3: VCC\_AXG\_SENSE  
PAD T4: VSS\_AXG\_SENSE

CANTIGA ES\_FCBGA1329  
GM45R3@

WS\_C3A

VCC GFX NCTF

POWER

VCC GFX

VCC SM LF

- VCC\_AXG\_NCTF\_1
- VCC\_AXG\_NCTF\_2
- VCC\_AXG\_NCTF\_3
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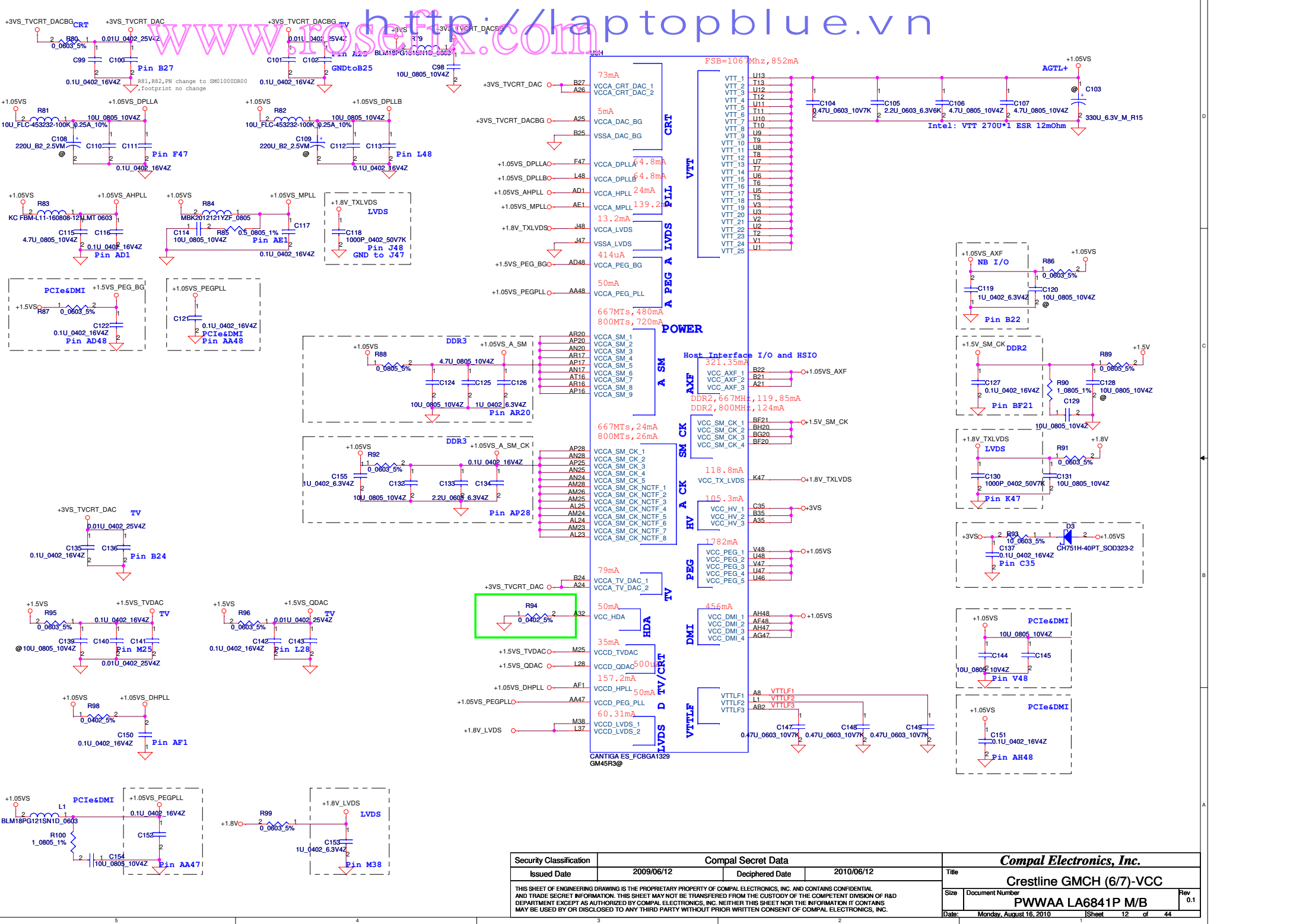
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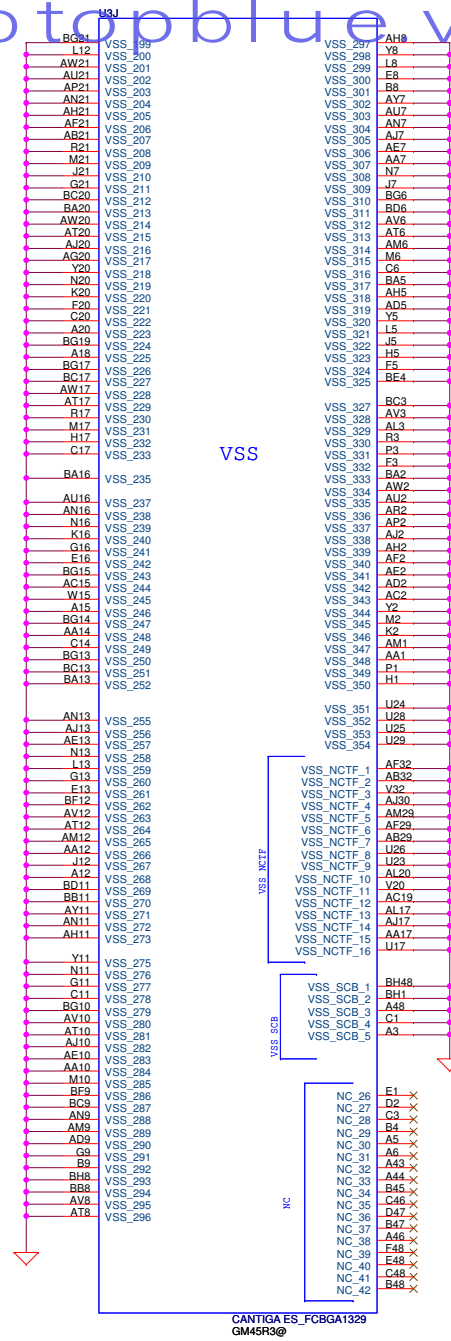
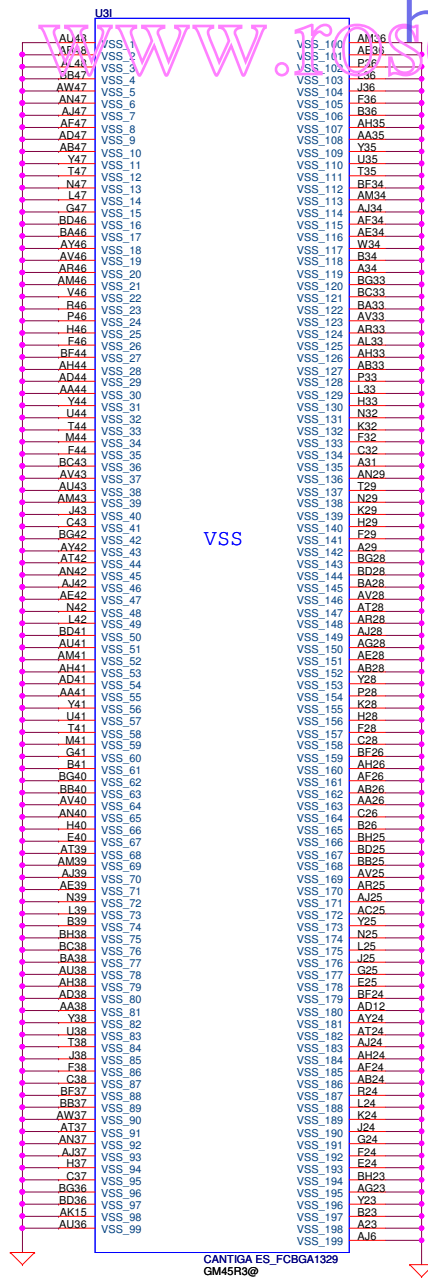
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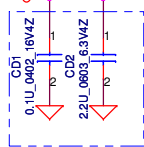


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+V\_DDR3\_DIMM\_REF



close to JDDR.H.1

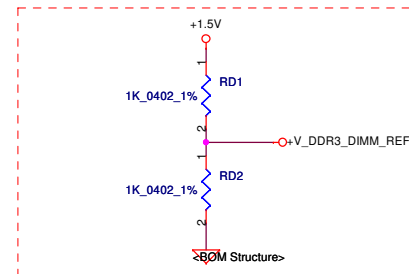
DDR A D0  
DDR A D1  
DDR A DM0  
DDR A D2  
DDR A D3  
DDR A D8  
DDR A D9  
DDR A DQS#1  
DDR A DQS1  
DDR A D10  
DDR A D11  
DDR A D16  
DDR A D17  
DDR A DQS#2  
DDR A DQS2  
DDR A D18  
DDR A D19  
DDR A D24  
DDR A D25  
DDR A DM3  
DDR A D26  
DDR A D27

VREF#\_DQ  
VSS1  
VSS2  
VSS3  
VSS4  
VSS5  
VSS6  
VSS7  
VSS8  
VSS9  
VSS10  
VSS11  
VSS12  
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VSS67  
VSS68  
VSS69  
VSS70  
VSS71  
VSS72

DDR A D4  
DDR A D5  
DDR A DQS#0  
DDR A DQS0  
DDR A D6  
DDR A D7  
DDR A D12  
DDR A D13  
DDR A DM1  
DDR A D14  
DDR A D15  
DDR A D20  
DDR A D21  
DDR A DM2  
DDR A D22  
DDR A D23  
DDR A D28  
DDR A D29  
DDR A DQS#3  
DDR A DQS3  
DDR A D30  
DDR A D31

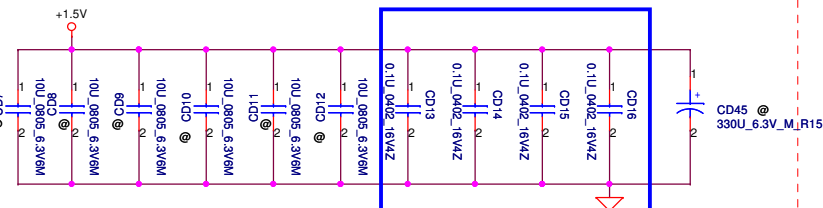
## DDR3 SO-DIMM A REVERSE TYPE

DDR A DQS[0..7] <9>  
DDR A DQS#0[0..7] <9>  
DDR A\_D[0..63] <9>  
DDR A\_DM[0..7] <9>  
DDR A\_MA[0..14] <9>

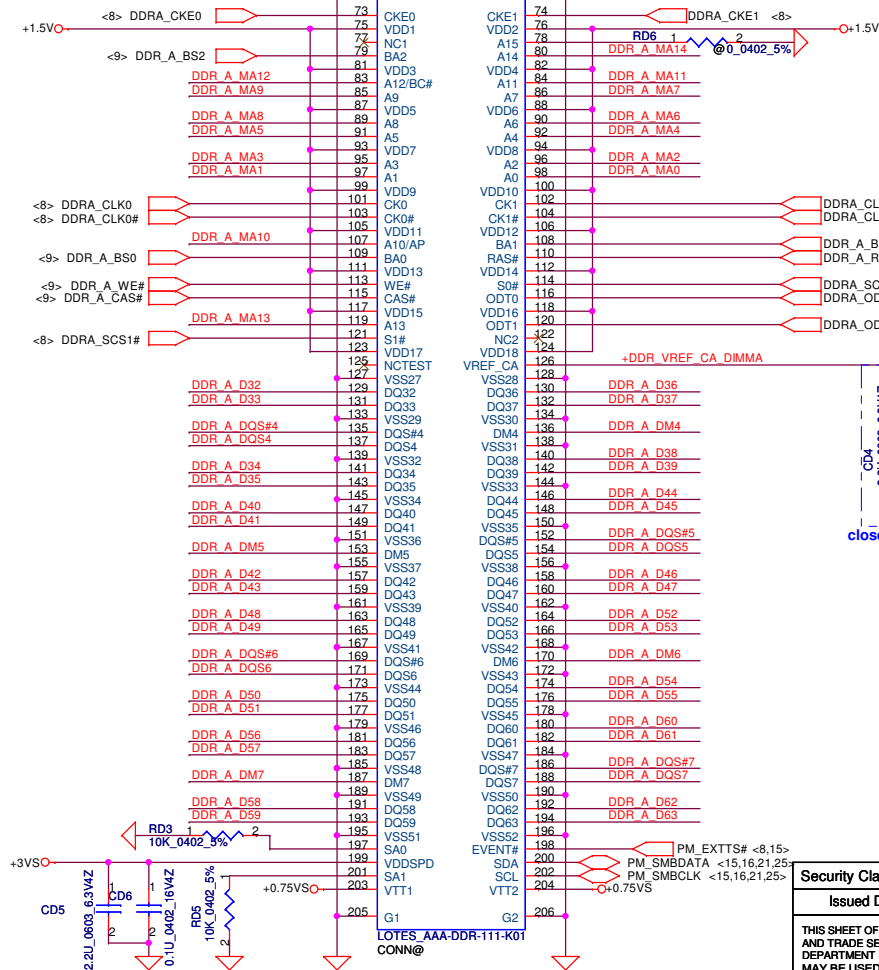
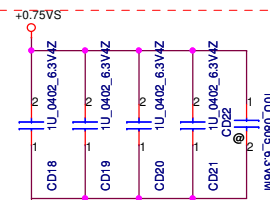


Layout Note:  
Place near JDDR.H

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMM

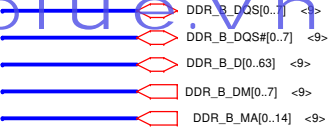


Layout Note:  
Place near JDDR.H.203 & JDDR.H.204

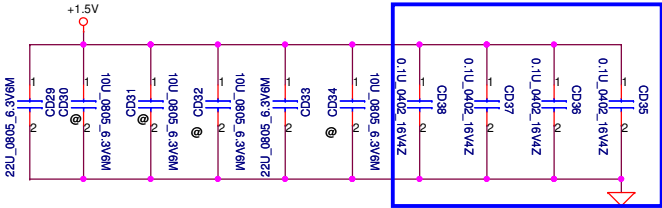


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								DDR II-SODIMMO	
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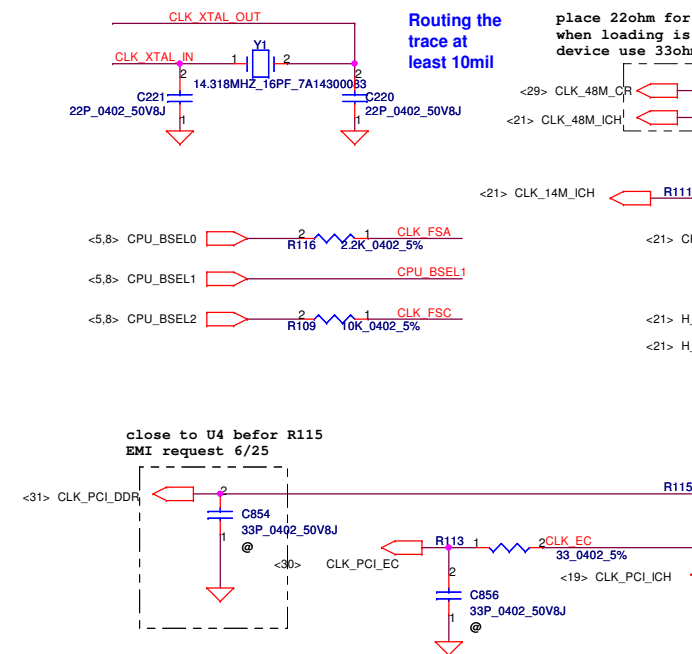
**Layout Note: Place these 4 Caps near Command and Control signals of DIMMB**



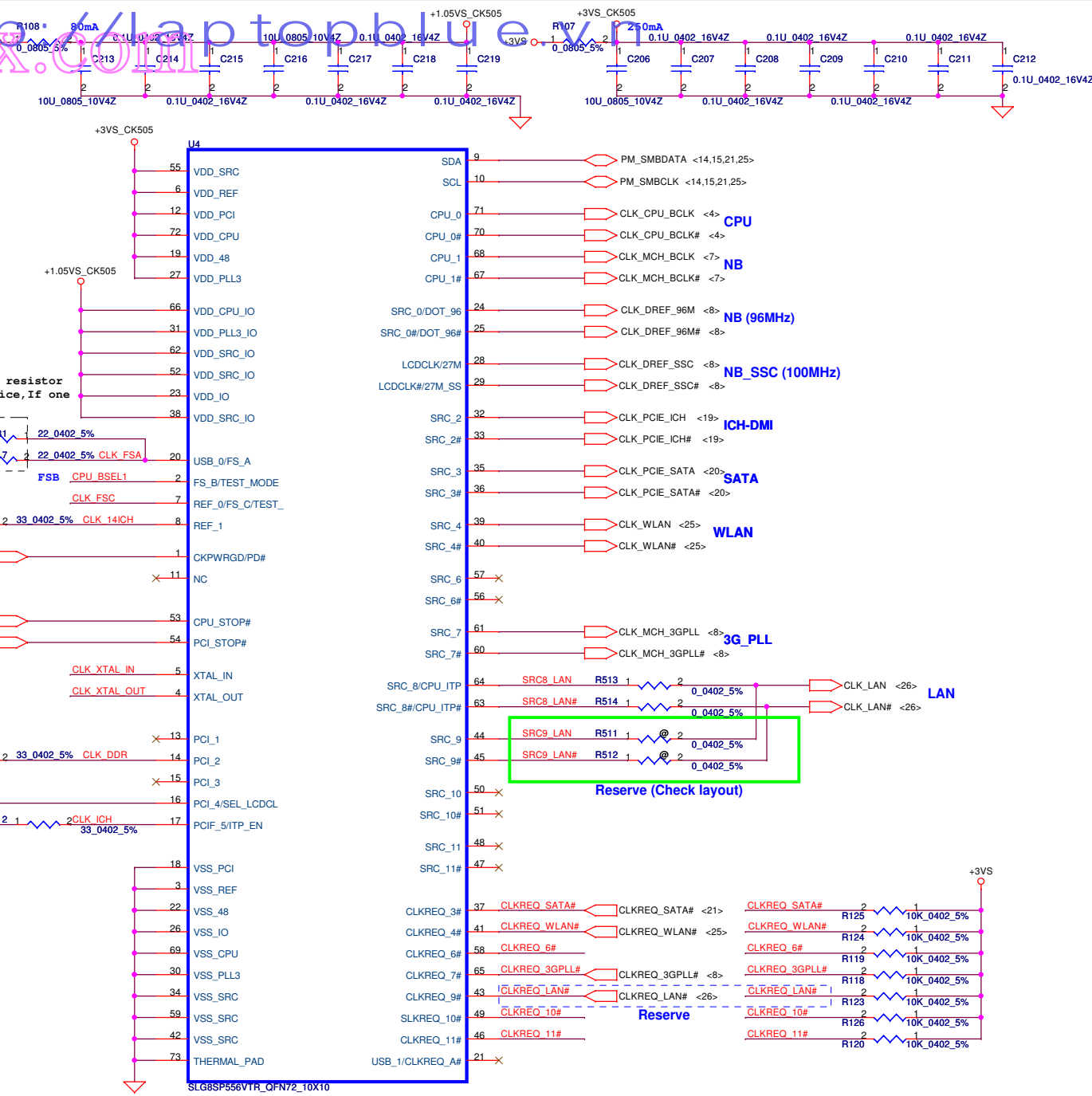
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2009/06/12	Deciphered Date	2010/06/12	Title <b>DDRII-SODIMMO</b>		
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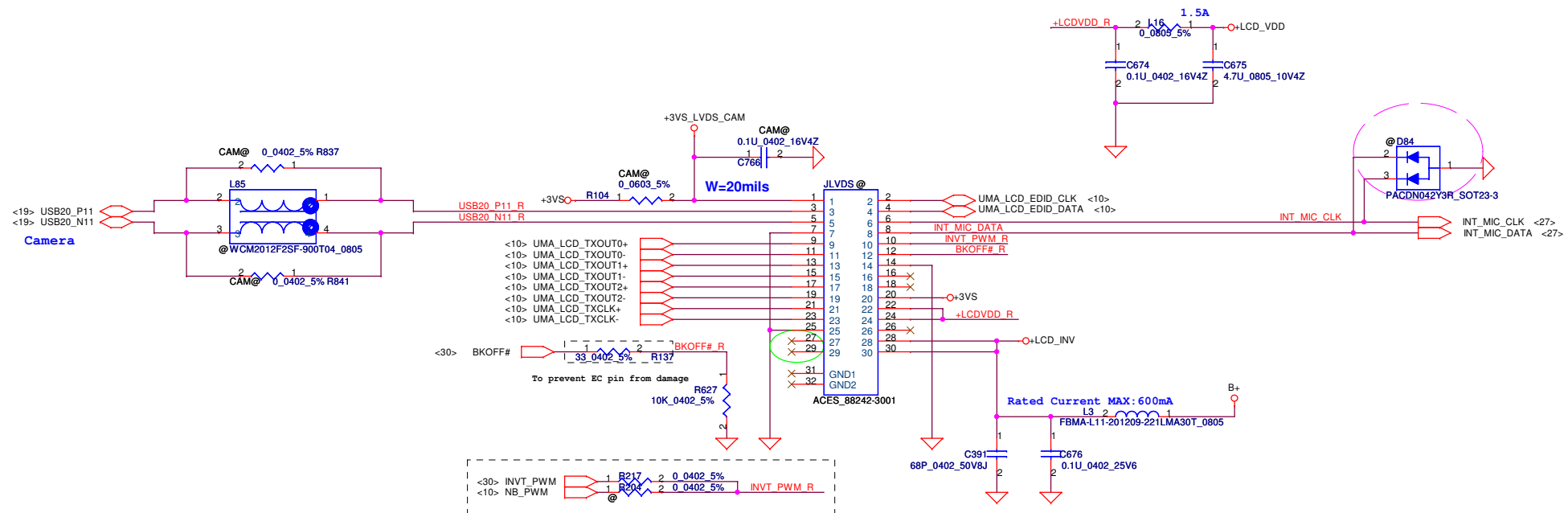
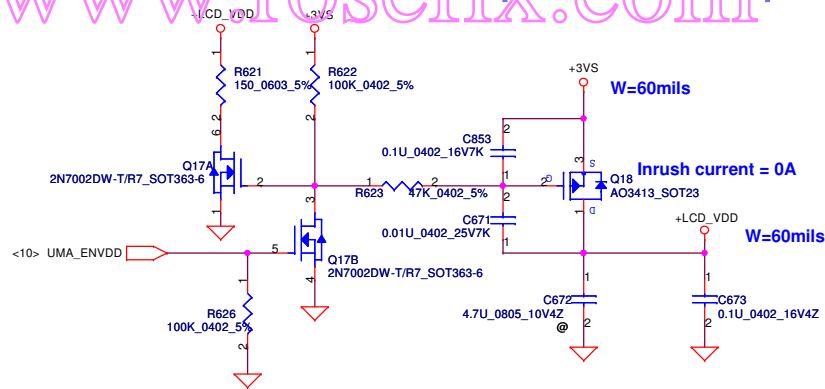
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1 (UMA) 1 = Enable SRC0 & 27MHz (DIS)

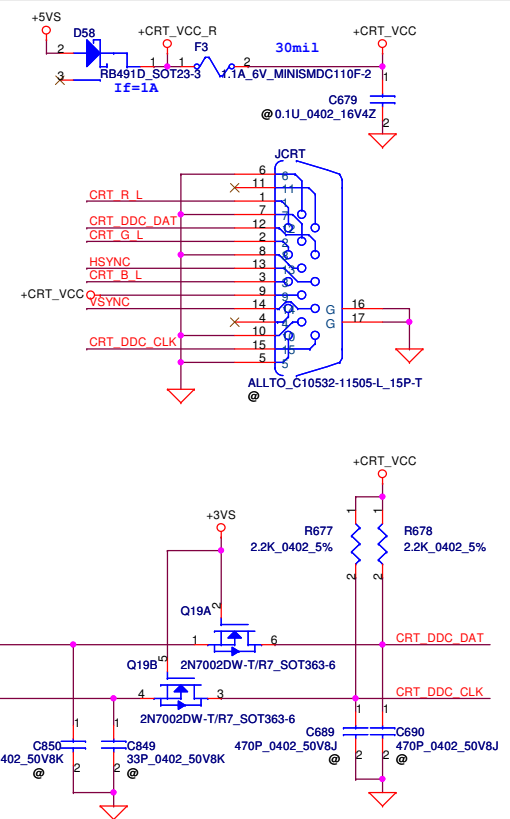


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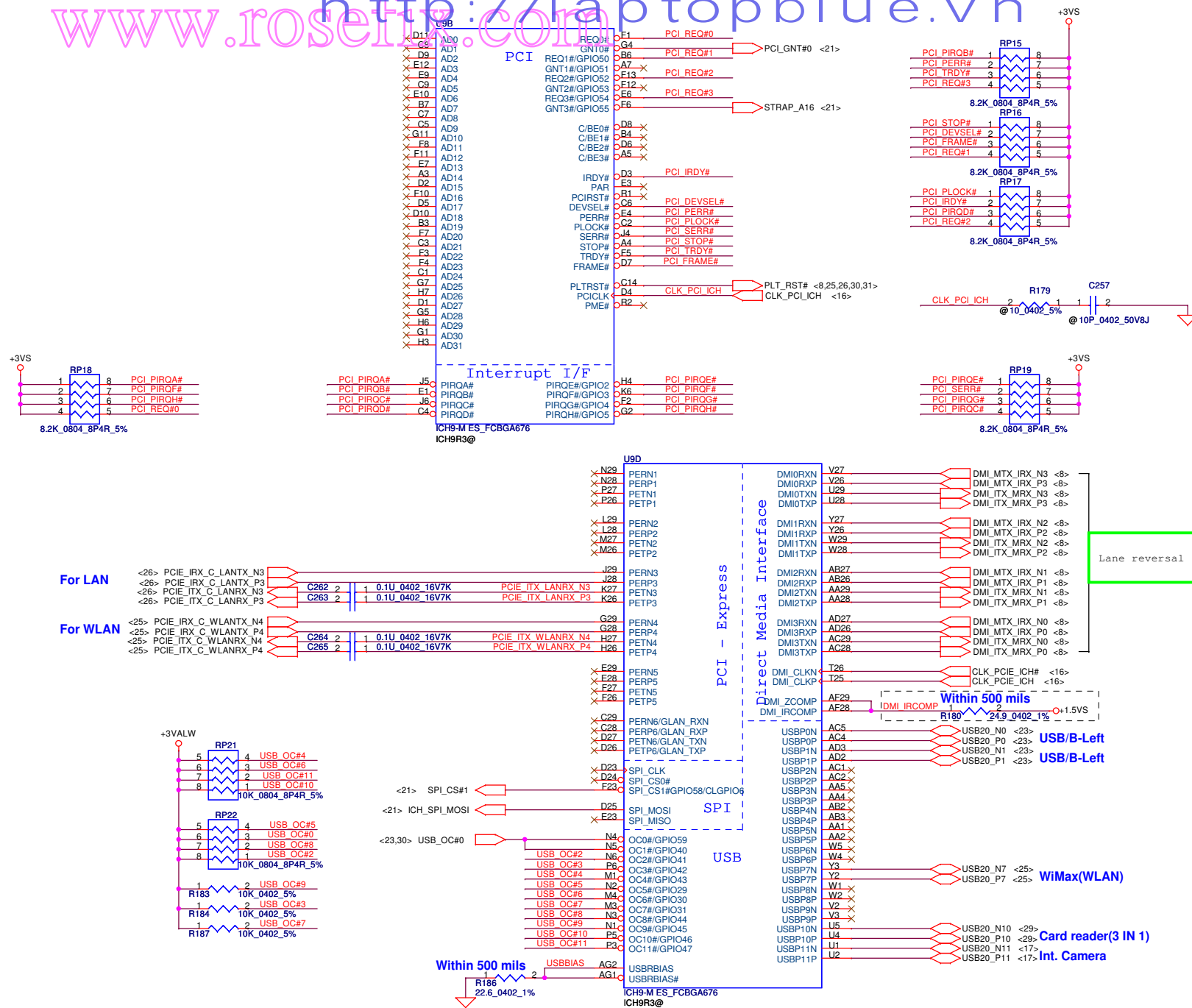


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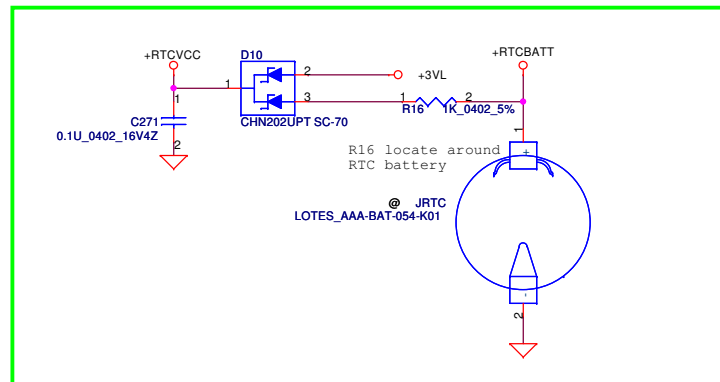
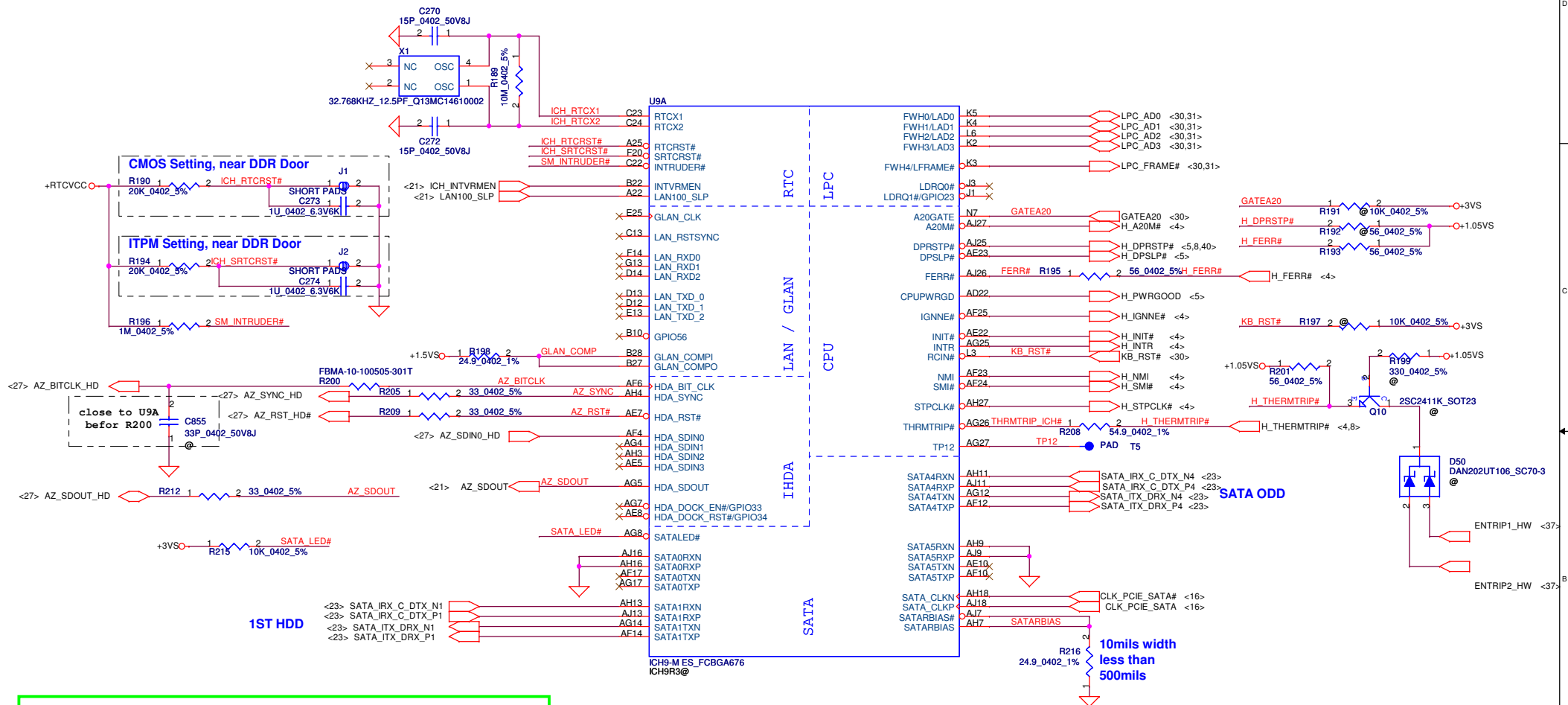
CTOR <http://laptopblue.vn>  
www.rosefix.com



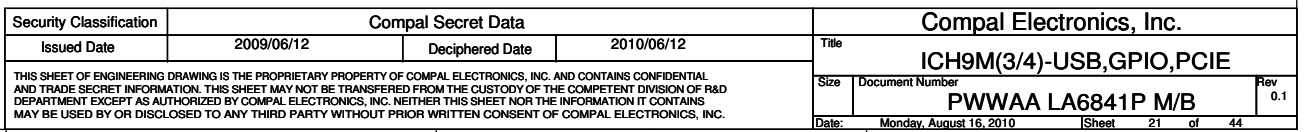
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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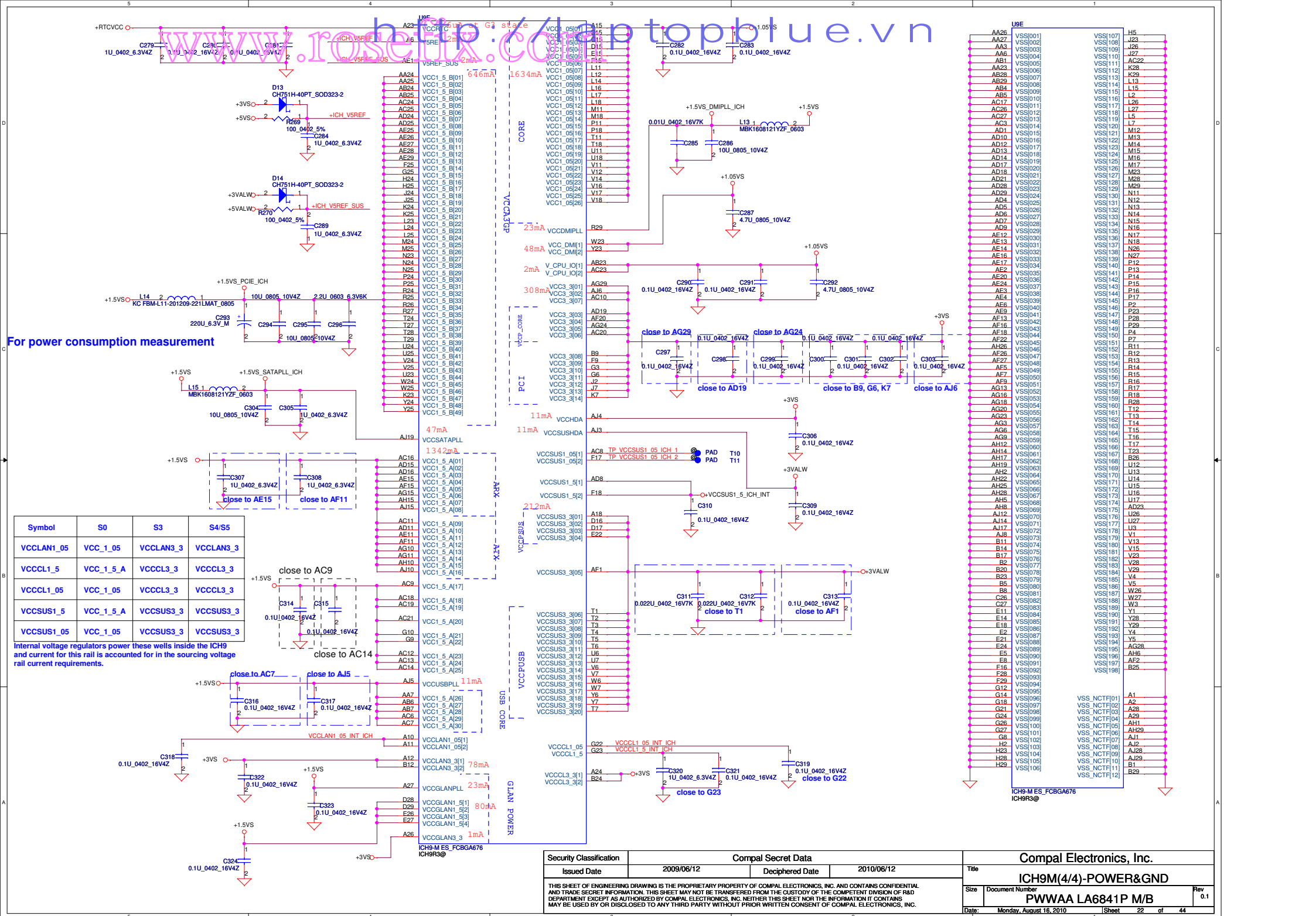
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/06/12	Deciphered Date	2010/06/12	Title	
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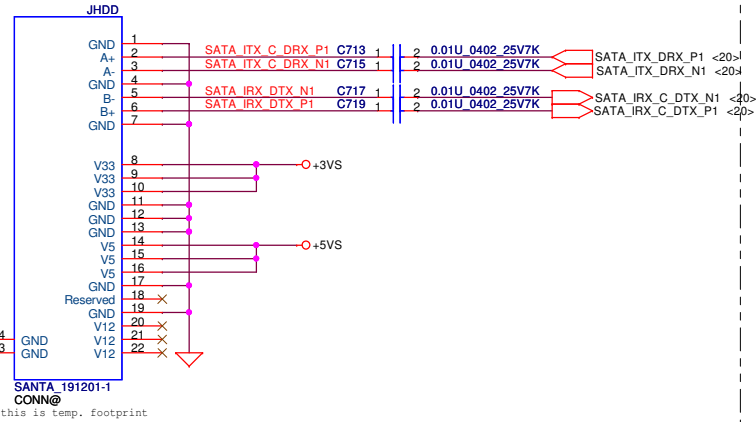
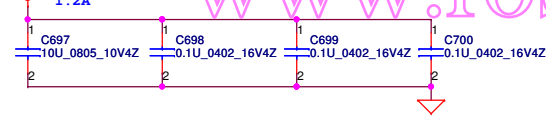




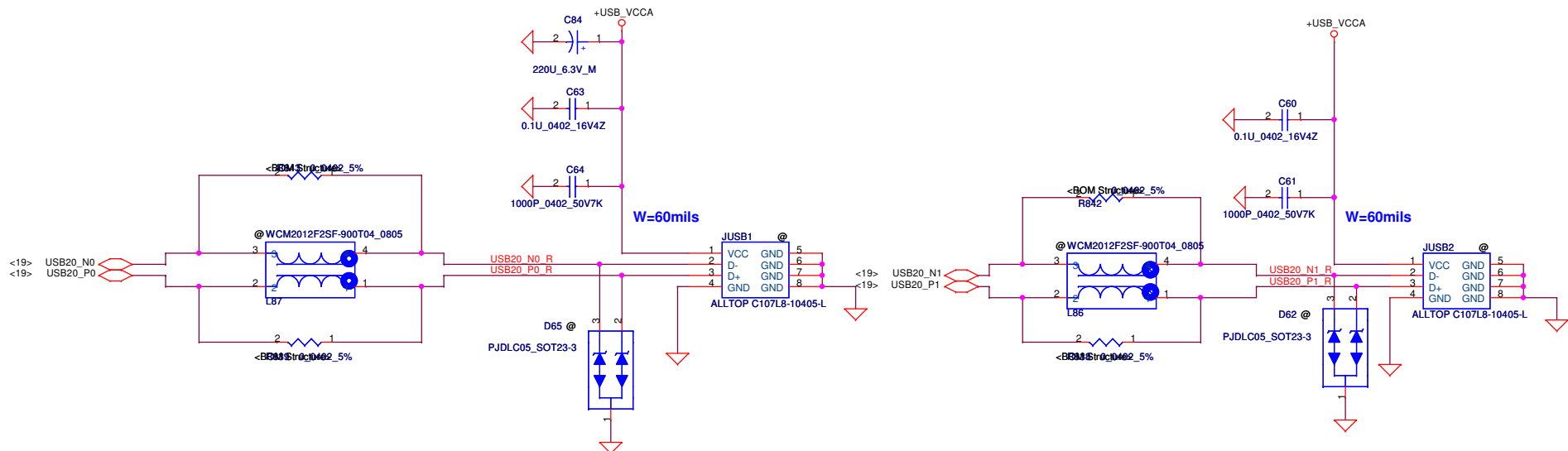


## SATA HDD Conn.

Place closely JHDD SATA COIN

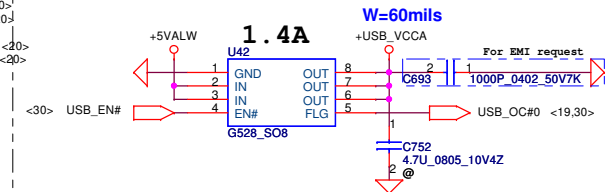
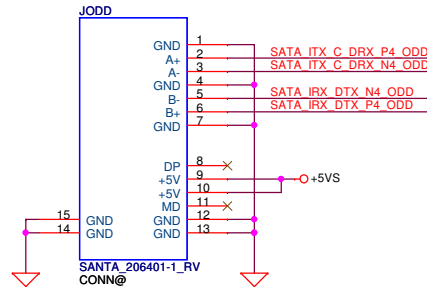
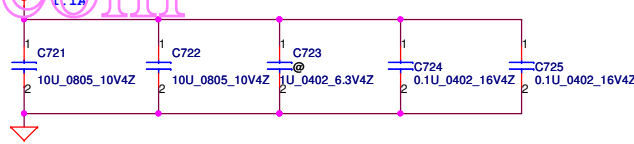


## USB Conn



## SATA ODD Conn

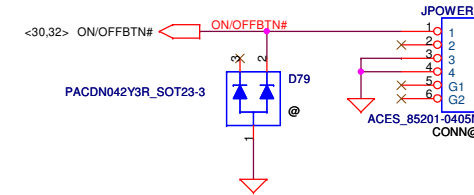
Place components close to ODD CONN.



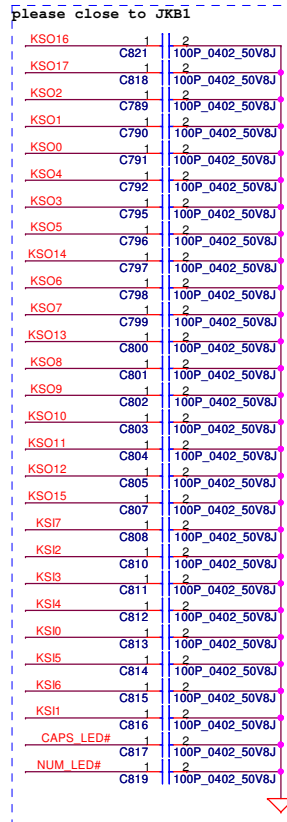
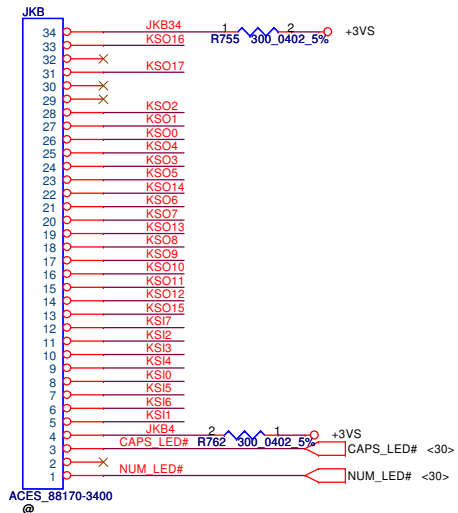
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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										SATA-HDD/ODD/USB	
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## POWER/B Connector Check footprint and pin define

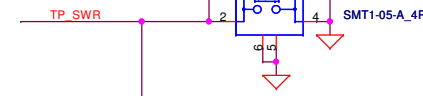


## KEYBOARD CONN

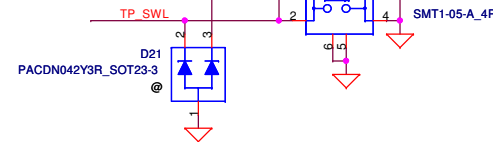


## Touch/B Connector

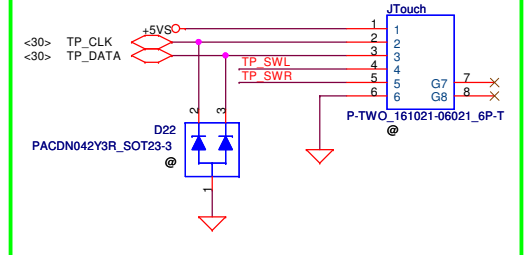
### Right Switch



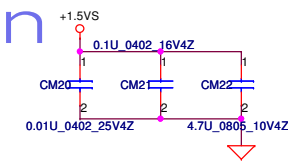
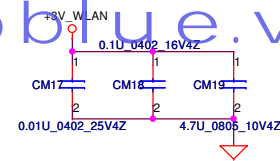
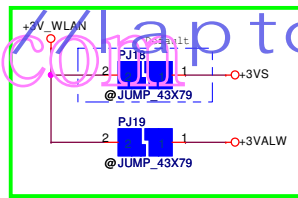
### Left Switch



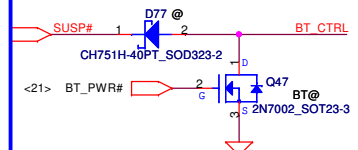
### Check signal to TP module through FFC



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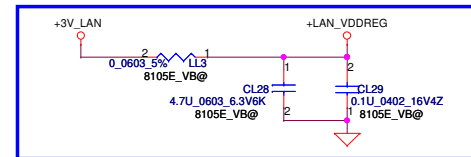
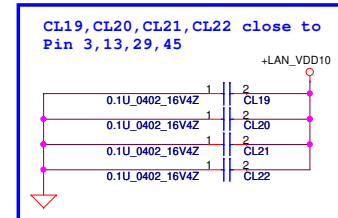
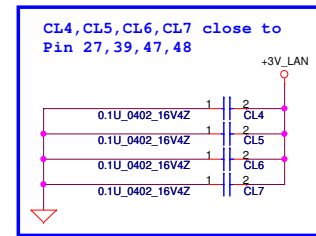


**\*\*If +3V\_WLAN is +3VS, please remove D77**

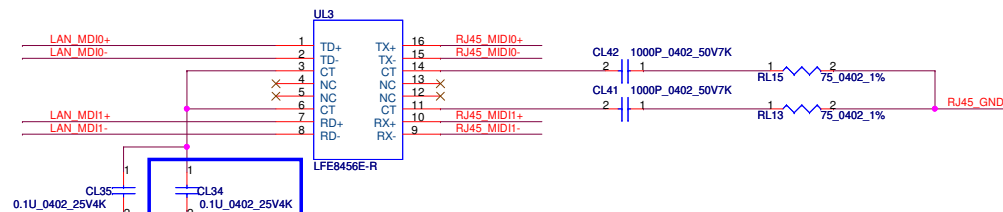
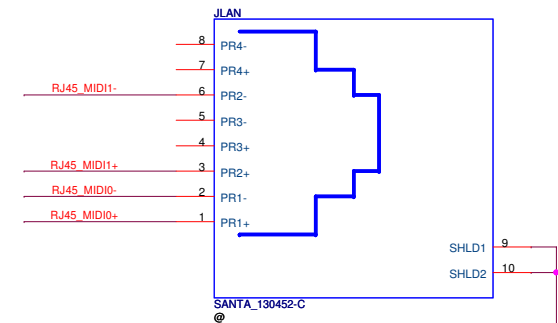


## Add BT\_CTRL for WLAN & BT Combo module at DVT

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				Size	Document Number	Rev
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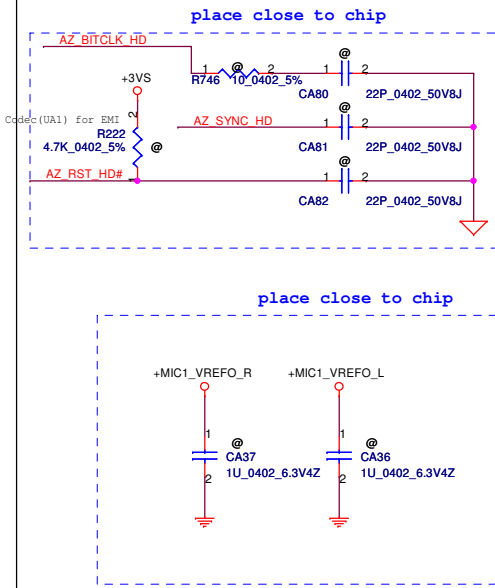
LAN Conn.






CL35 and CL34 for EMI request place near pin 3 and pin 6




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Beep sound



**place close to chip**

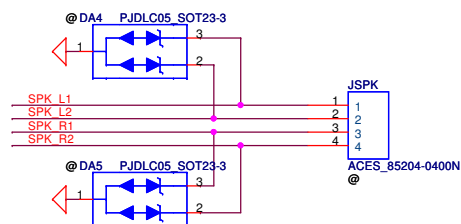
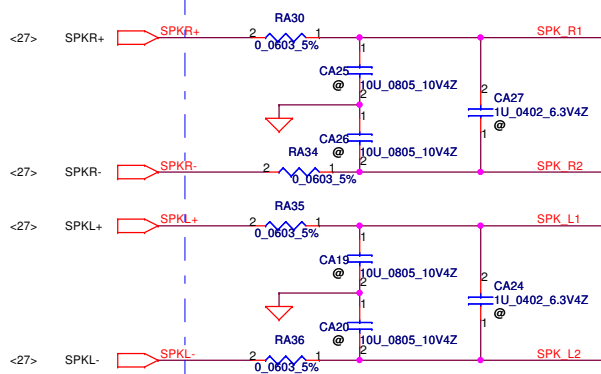
<28> MIC\_SENSE  RA10  20K\_0402\_1%  SENSE\_A

<28> NBA\_PLUG  RA21  39.2K\_0402\_1%  SENSE\_A

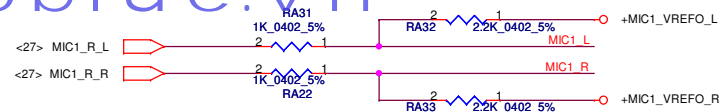
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title HD CODEC ALC272			
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				Date:	Monday, August 16, 2010	Sheet	27 of 44

## Speaker Connector

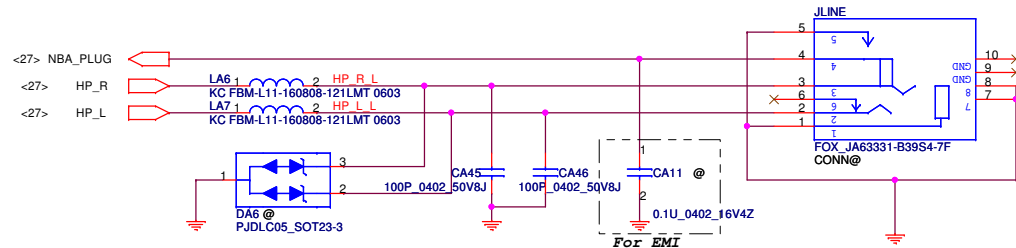
placement near Audio Codec UA1



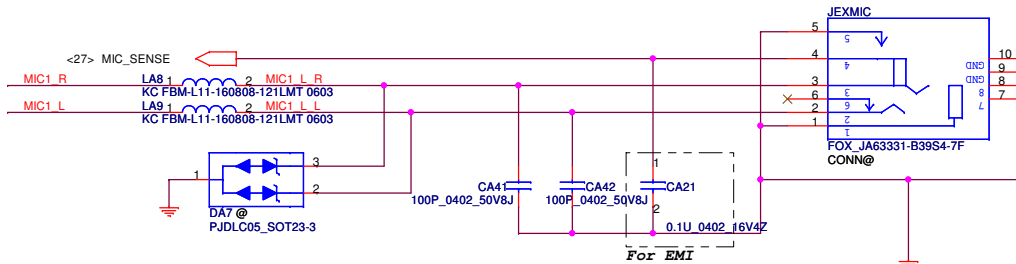
## Ext. Mic



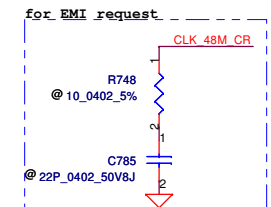
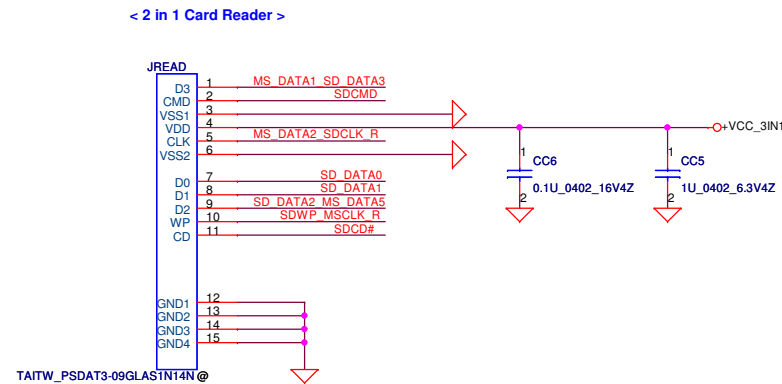
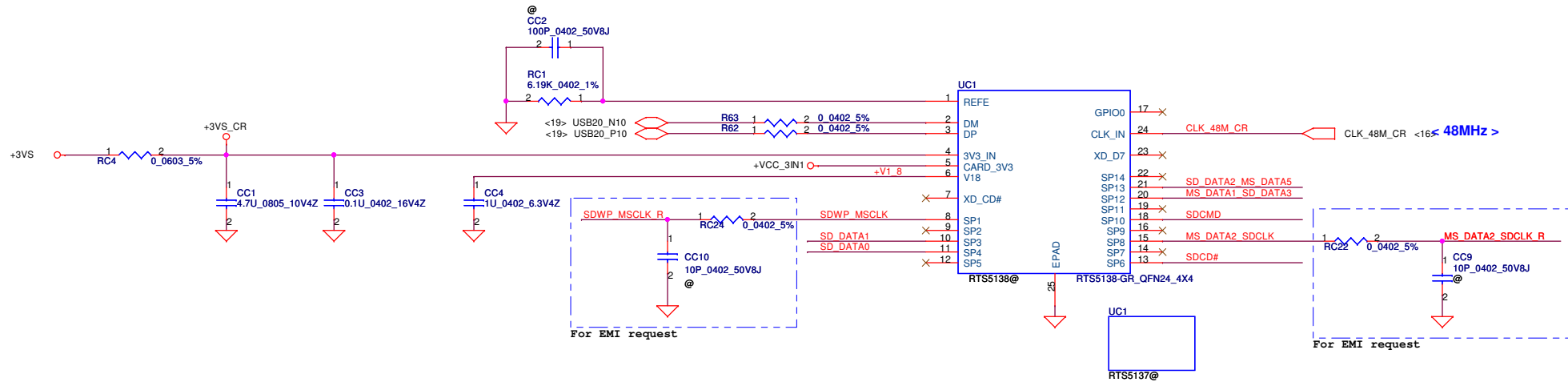
## HeadPhone/LINE Out JACK



## Ext.MIC/LINE IN JACK

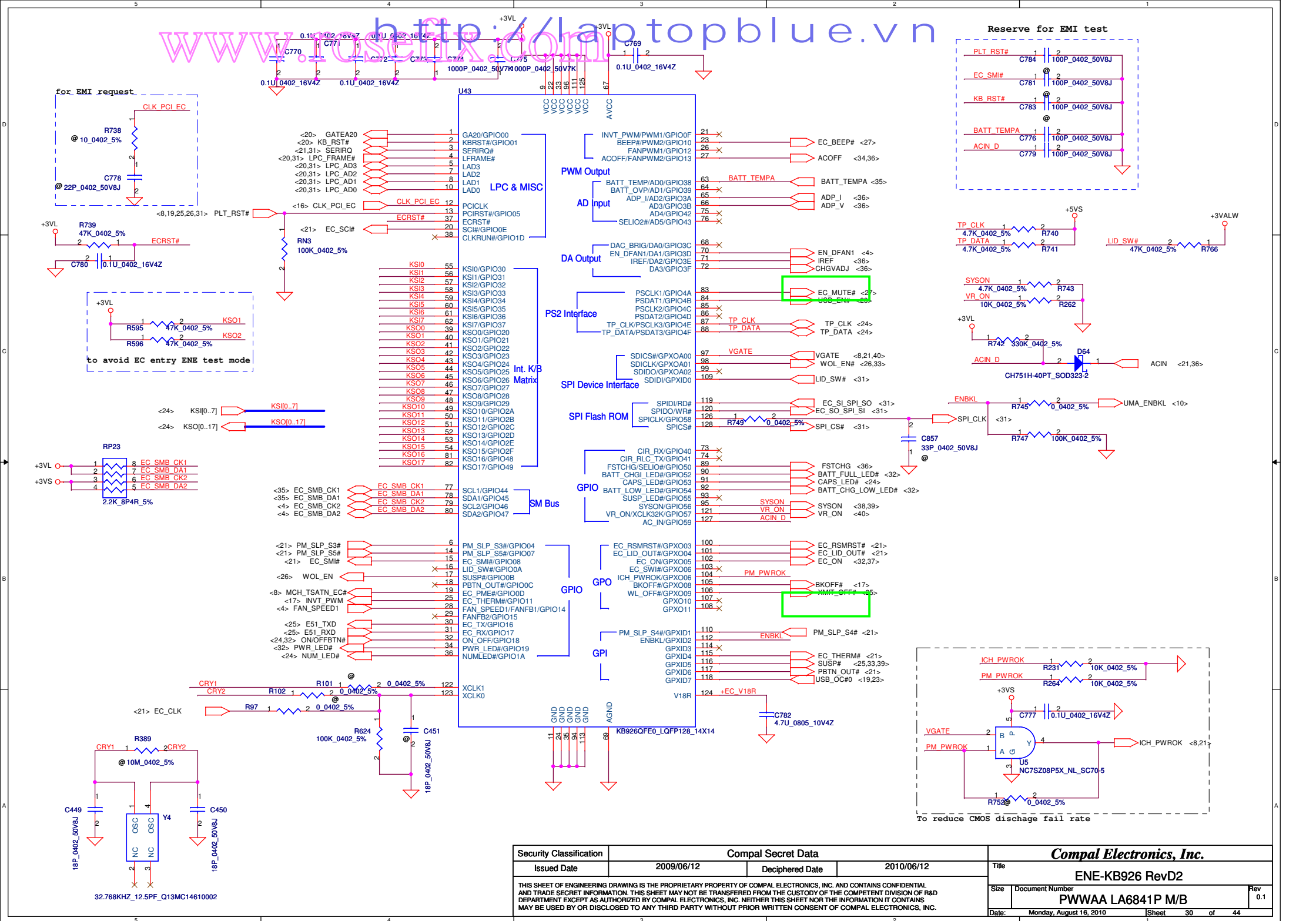


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				Date:	Monday, August 16, 2010	Sheet 28 of 44

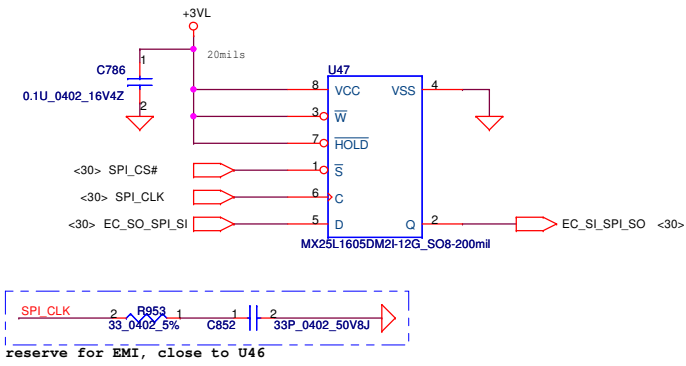


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				Custorn	PWWAA LA6841P M/B	0.1	
				Date:	Monday, August 16, 2010	Sheet 29 of 44	

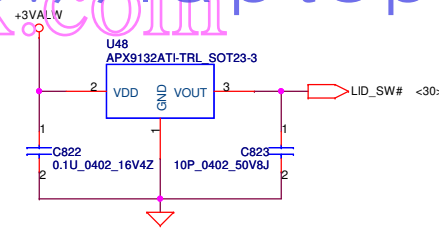




SPI Flash (16M\*1)

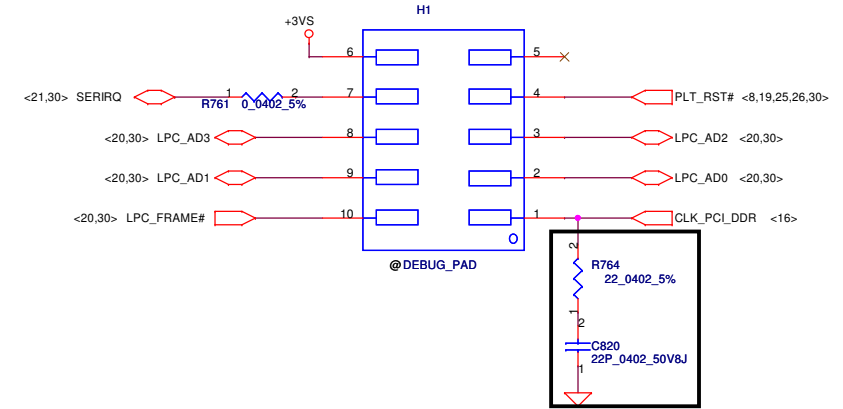


Lid SW

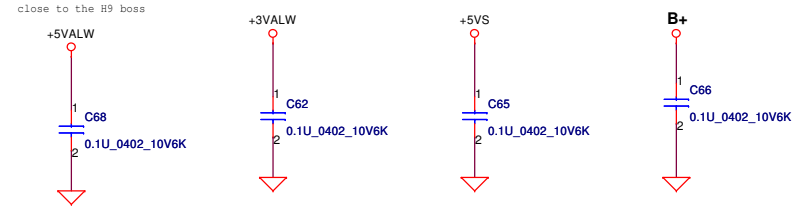


LPC Debug Port

Please place the PAD under DDR DIMM.

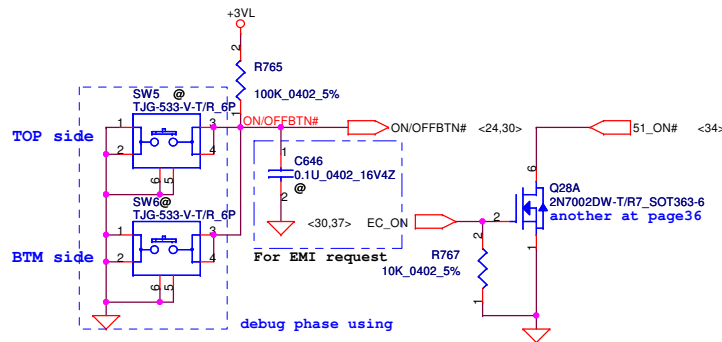


for EMI



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Date:		Monday, August 16, 2010		Sheet	
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		44		0.1	

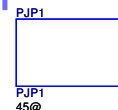
# Power Button



PCB



# DC-IN

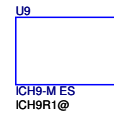
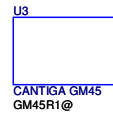
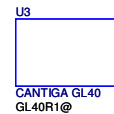


NB\_GL40\_R3

NB\_GL40\_R1

NB\_GM45\_R1

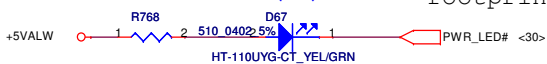
SB\_R1



# DC-IN LED

Vf=2.0V (typ), 2.4V (max)  
If=30mA (max)

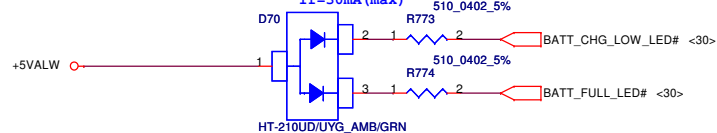
footprint is SC510UYG000



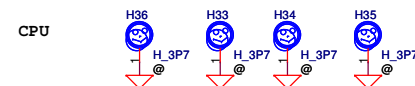
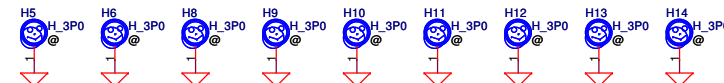
# BATT CHARGE/FULL LED

Vf=1.9V (typ), 2.4V (max) for amber  
Vf=2.0V (typ), 2.4V (max) for green  
If=30mA (max)

footprint is SC510UDG000

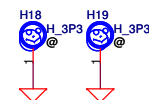


# Screw Hole



SB

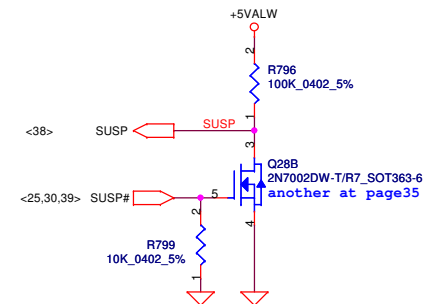
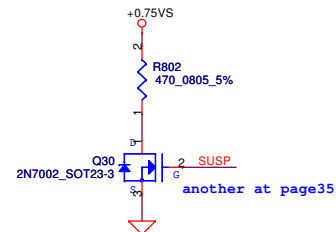
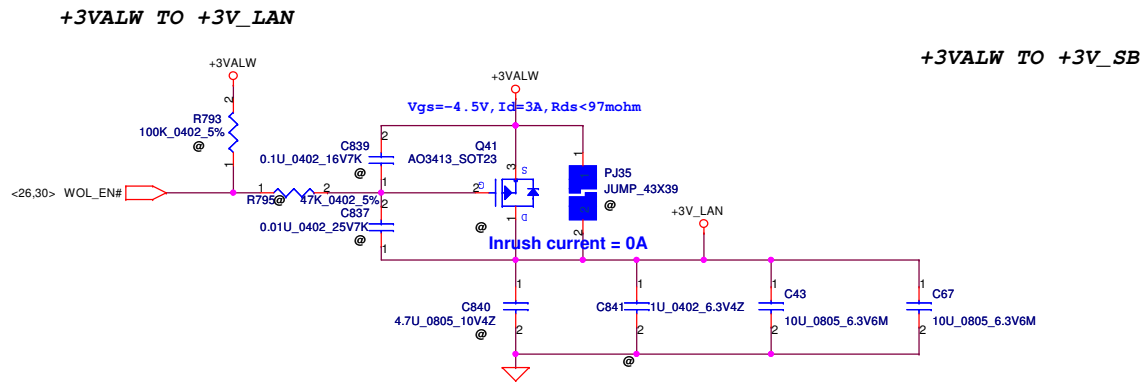
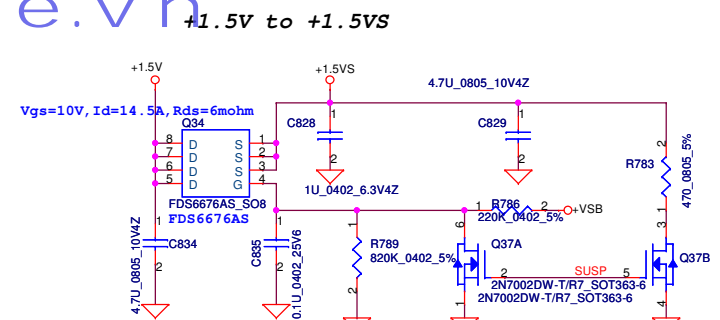
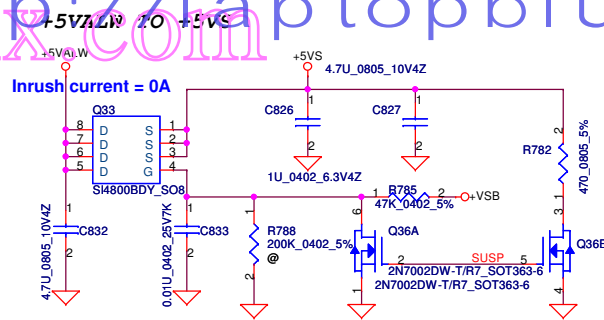
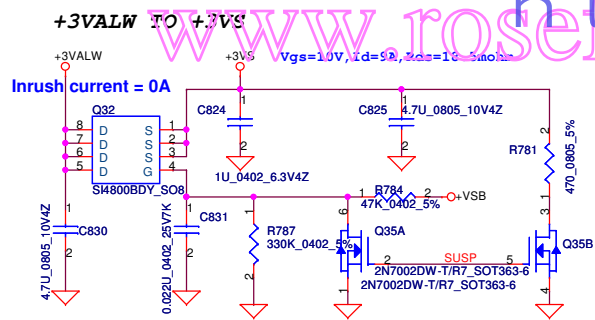
MINI CARD



# PCB Fedcal Mark PAD

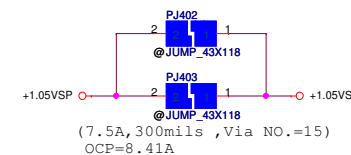
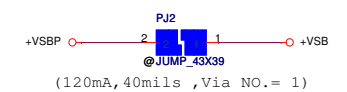
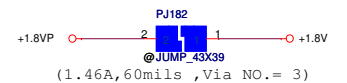
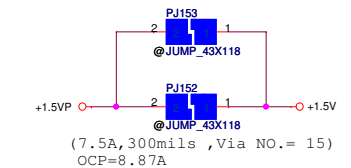
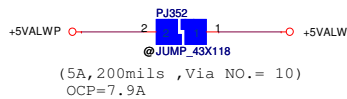
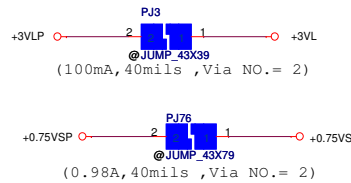
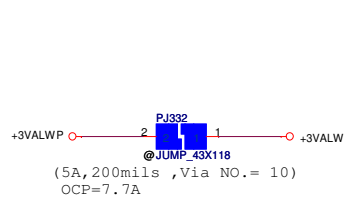
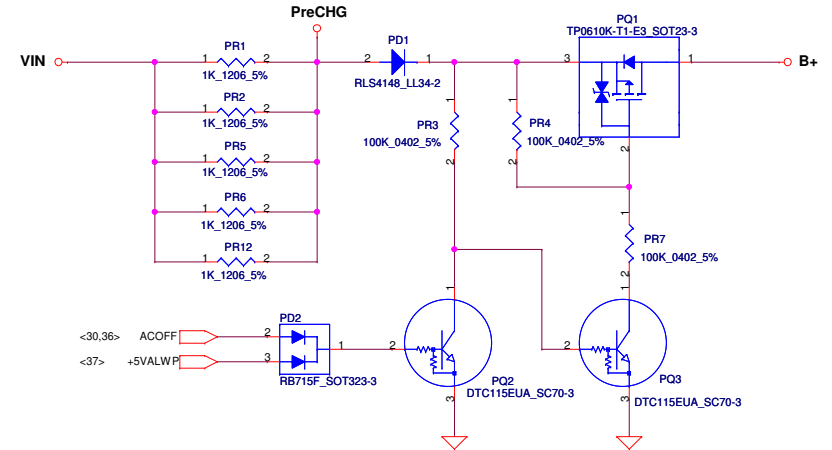
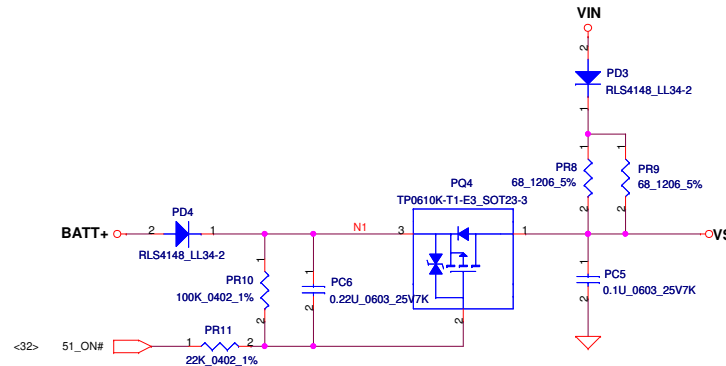
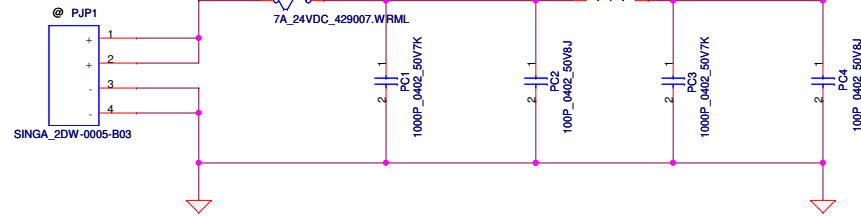


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				Rev	0.1



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Size	Document Number	PSWAA LA6511P M/B		Rev	0.1
Date	Monday, August 16, 2010	Sheet	33	of	44

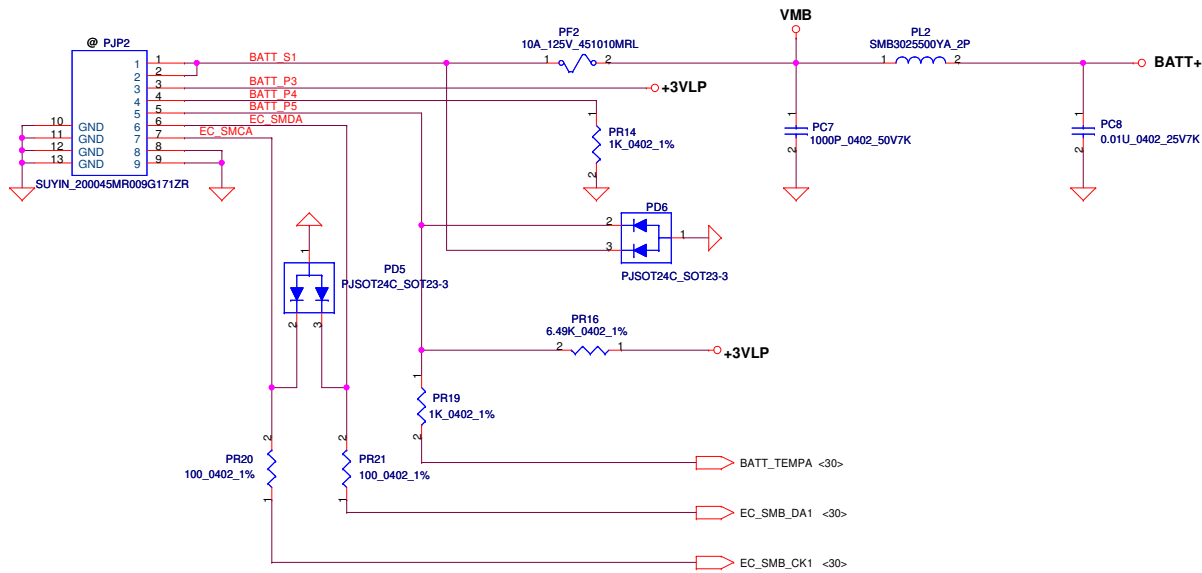
# DC301001M80



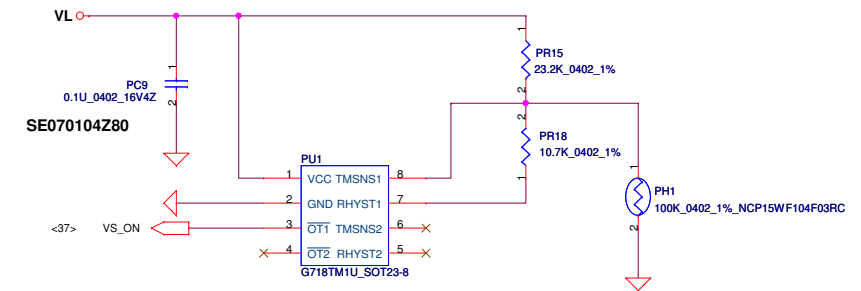
## ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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Size	Document Number	KSWAA			Rev
Date	Monday, August 16, 2010	Sheet	34	of	44
					0.1



PH1 under CPU bottom side :  
CPU thermal protection at 90 degree C  
Recovery at 56 degree C



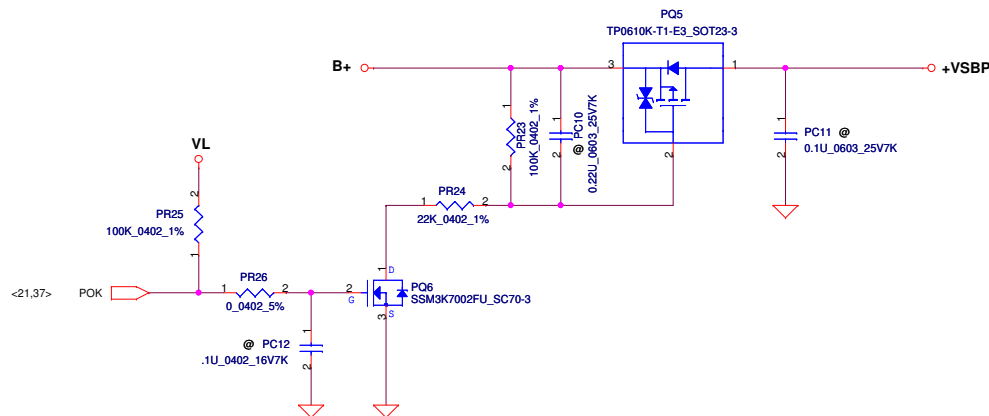
$$R_{set} = 3 * R_{tmh}$$

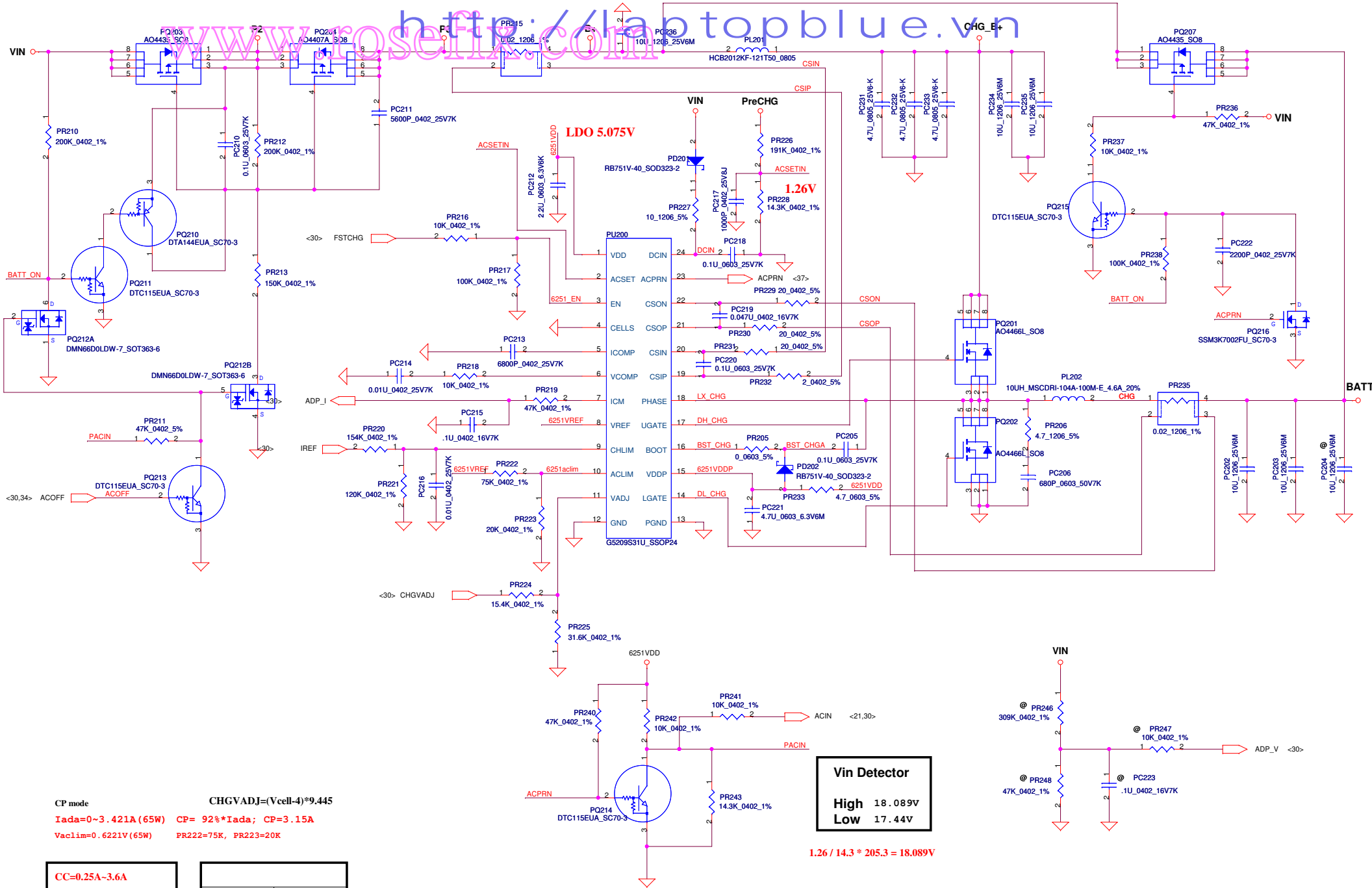
$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.79K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.79K = 23.37K \Rightarrow 23.2K$$

$$R_{hyst} = (23.2K * 26.1K) / (3 * 26.1K - 23.2K) = 10.99K \Rightarrow 10.7K$$





CP mode CHGVADJ=(Vcell-4)\*9.445  
 Iada=0~3.421A (65W) CP= 92%\*Iada; CP=3.15A  
 Vaclim=0.6221V (65W) PR222=75K, PR223=20K

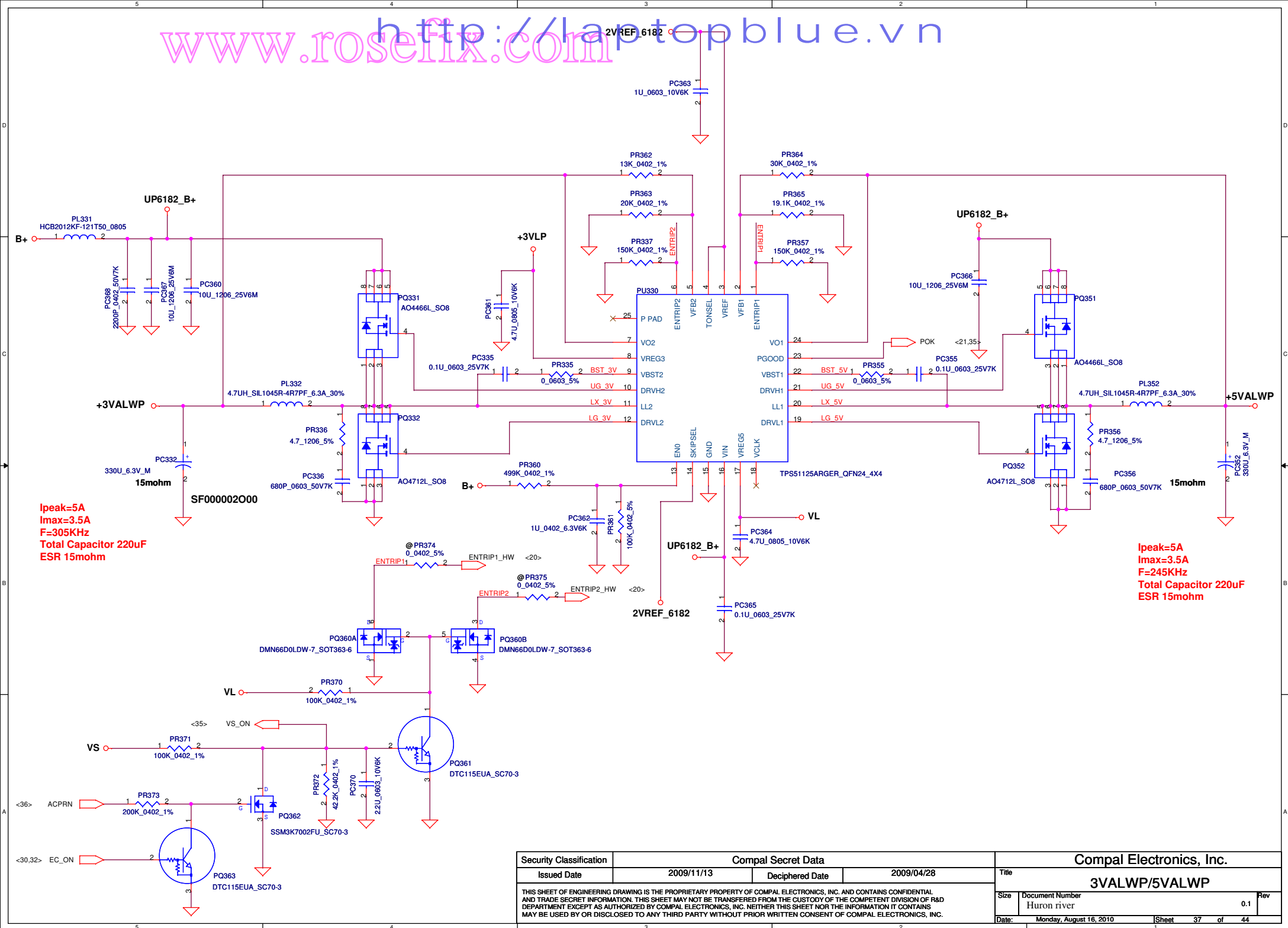
CC=0.25A-3.6A  
 IREF=0.9133\*Icharge  
 IREF=0.228V-3.29V  
 VCHLIM need over 95mV

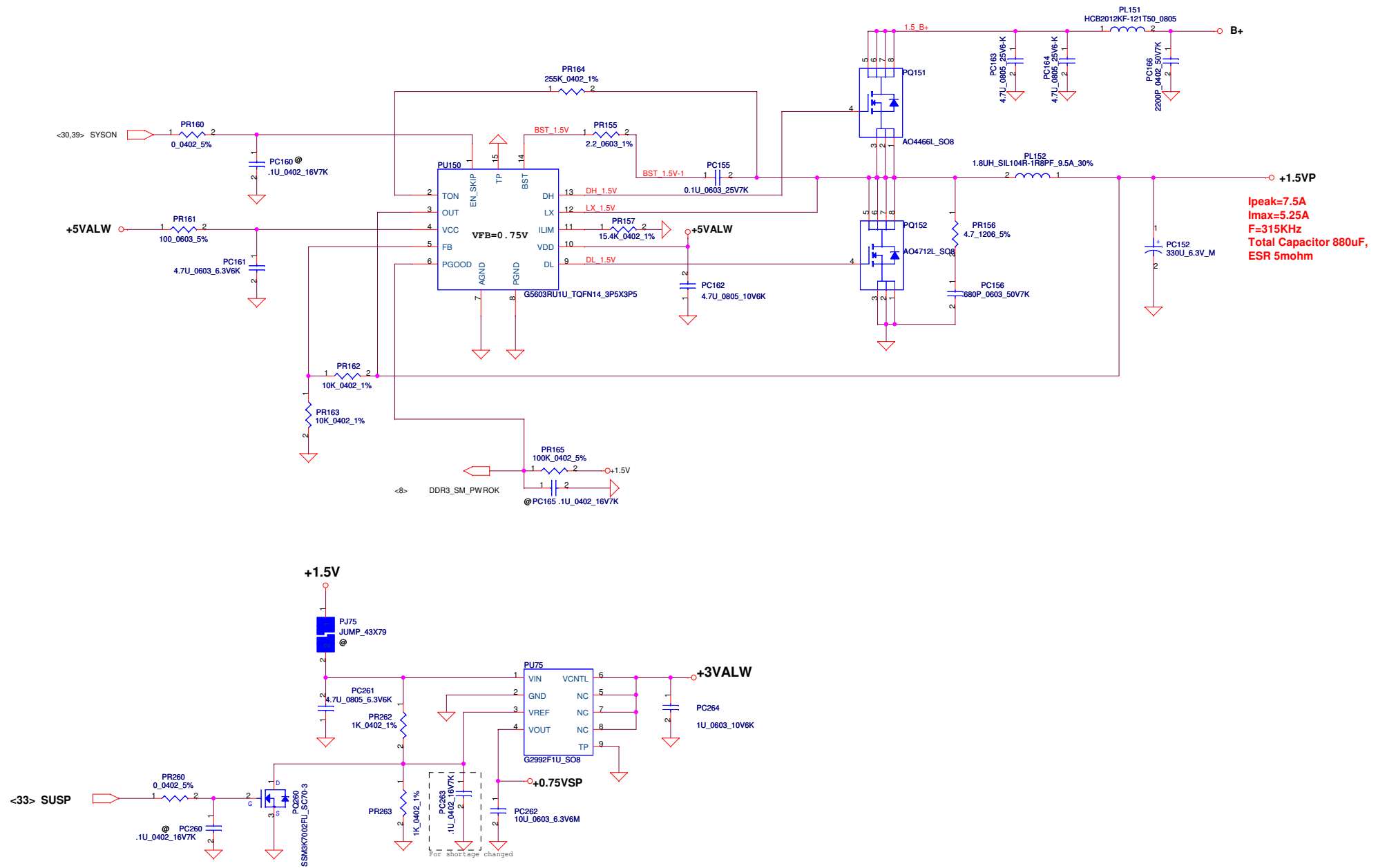
Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

**Vin Detector**  
 High 18.089V  
 Low 17.44V

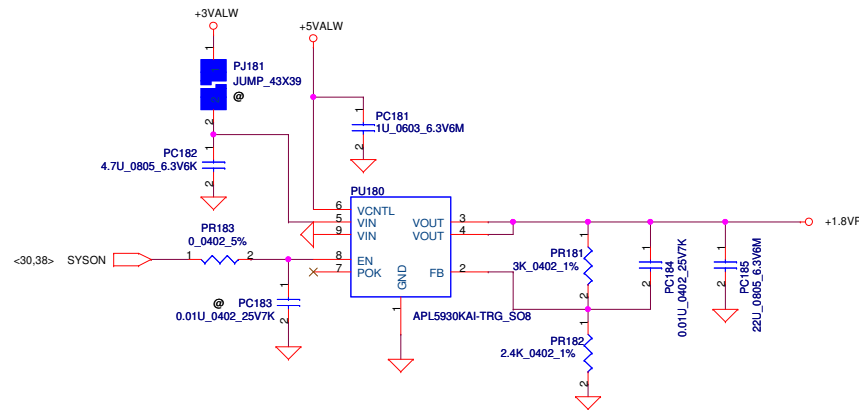
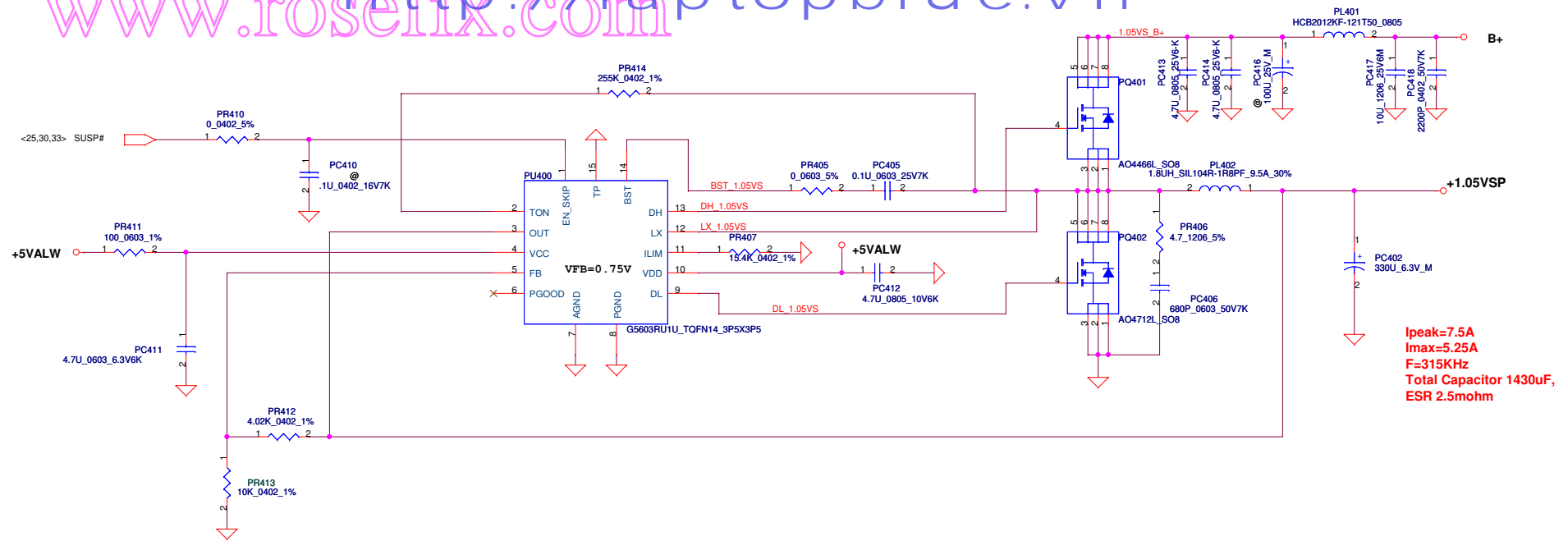
$1.26 / 14.3 * 205.3 = 18.089V$

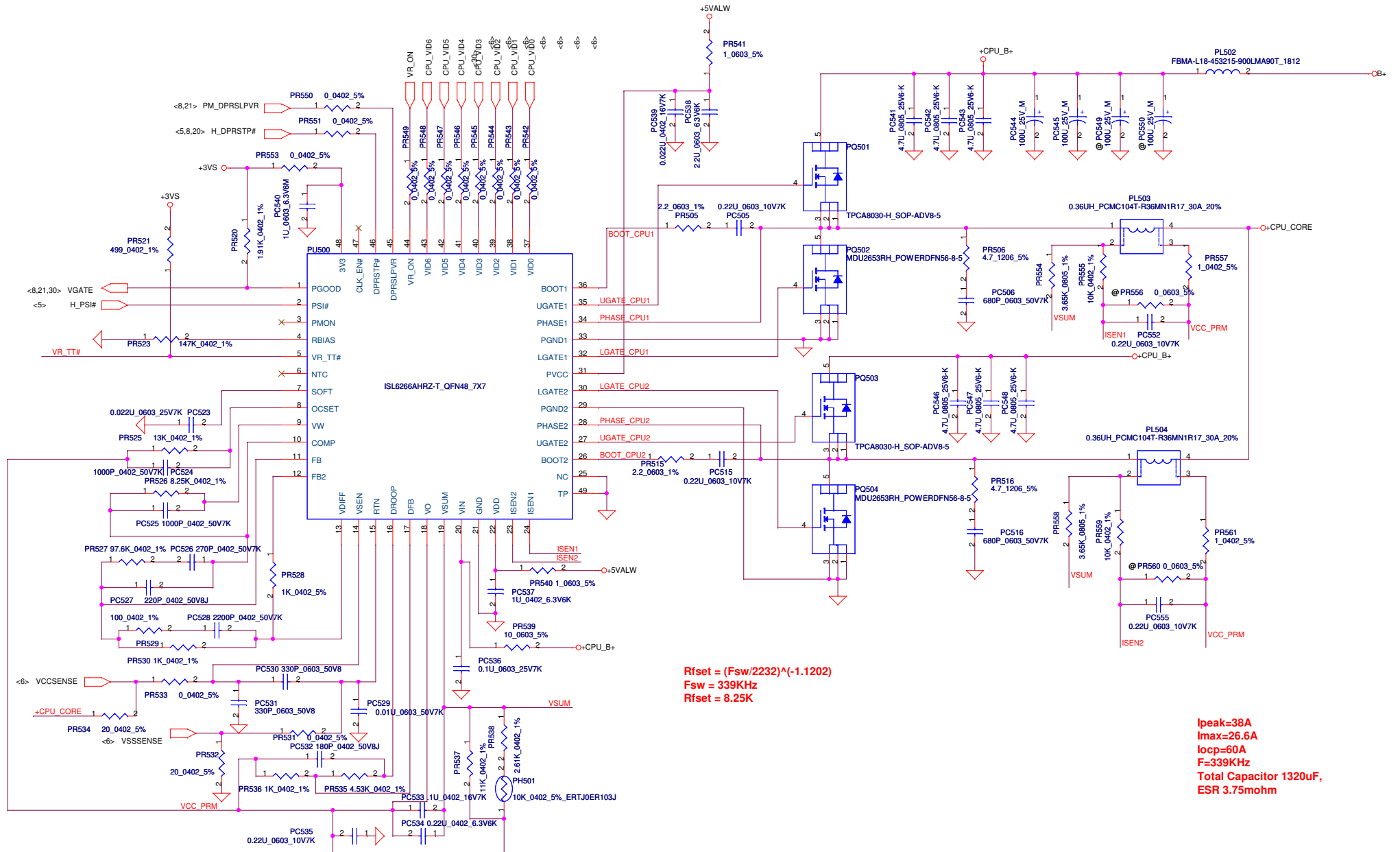






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PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 0.2 EVT

MODIFICATION LIST				PURPOSE
1.	07/23	32	Change R768,R773 from 120 ohm to 510 ohm	for changed 5mA LED
2.	07/23	32	Chage LED power rail from +3valw to +5valw	for changed 5mA LED
3.	07/23	23	del. L86,L87 EMI component	for EMI request
4.	07/23	31	Add 1PCS(C62) 0.1uF_0402 on +3Valw-->GND	for EMI request
5.	07/23	31	Add 1PCS(C65) 0.1uF_0402 on +5Vs-->GND	for EMI request
6.	07/23	31	Add 0.1uF_0402(C66) on B+-->GND close to H8	for EMI request
7.	07/23	28	JLINE and JEXMIC change from DC2300006300 to DC230004L00	for SMT DFx request
8.	07/27	30	change R742 from +3VALW to +3VL	for LED no function issue
9.	07/27	8	add test pad ON U3.E36,U3.AK34	for ATE request
10.	07/27	33	change part number of Q30 (SB770020010)	for Reduce BOM part type
11.	07/27	32	Change D67(power on LED) from SC510UYG000 to SC500009D00	for changed 5mA LED
12.	07/27	32	Change D70(DC in LED) from SC510UDG000 to SC500009800	for changed 5mA LED
13.	07/29	14	un-mount CD7,CD8,CD9,CD10,CD11,CD12,CD30,CD31,CD32,CD34,and mount(22uF) CD29,CD33	for design change
14.	07/29	11	For +1.5V ,C78 from 330uF to 390u (SF000002000)	for design change
15.	07/29	12	Change R82 and R81 from inductor to Bead	for design change
16.	07/29	15	+0.75VS filter un-mount CD22 and CD44	for design change
17.	08/03	25	un-mount D77	for If +3V_WLAN is +3VS, please un-mount D77

PIR (Product Improve Record)

REVISION CHANGE: 0.2 TO 0.3 Pre-MP  
NO DATE PAGE MODIFICATION LIST

- 1. 08/09 29 Change net V1\_8 to +v1\_8
- 2. 08/09 32 add R774
- 3. 08/12 32 un-mount SW5 and SW6
- 4. 08/12 20 add R16 (for RTC battery)
- 5. 08/13 26 add D69 and un-mount CL38
- 6. 08/13 26 CL37 from 0.1uF to 120pF
- 7. 08/13 26 add CL35
- 8. 08/13 27 add CA51
- 9. 08/13 33 add C67 and C43

PURPOSE

- for power trace
- for LED control
- for Pre-MP do need power SW
- for design change
- for EMI request
- for EMI request
- for EMI request
- for EMI request
- for EMI request

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PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 1.0

NO DATE PAGE MODIFICATION

PURPOSE

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Item Title

Solution Description

PVT : modification from EVT		
P35	mount ESD diode	mount PD5, PD6
P36	EMI request	add PC236 10uF
P37	EMI request	add PC367 10uF, PC368 2200pF
P37	change 3/5V IC main source	change PU330 to UP6182
P38	EMI request	add PC166 2200pF
P39	EMI request	add PC417 10uF, PC418 2200pF
P40	adjust loadline	change PR535 to 3.09K
P34	unify source	change PD1 to SC11N414880
P36	unify source	change PQ216 to SB0000009610
P37	unify source	change PQ362 to SB0000009610
P40	unify source	change PL502 to SM010020720
P40	turn on speed too quick	change PQ502, PQ504 to MDU2653RH
P37	change cap to 330uF with same price	change PC332, PC352 to SF0000002000
P38	change cap to 330uF with same price	change PC152 to SF0000002000
P39	change cap to 330uF with same price	change PC402 to SF0000002000
P36	EMI request to mount snubber circuit, ISN caps	add PR206, PC206; PC234, PC235
P37	EMI request to mount snubber circuit	add PR336, PC336; PR356, PC356
P38	EMI request to mount snubber circuit & boost resistor	add PR156, PC156; change PR155 to 2.2ohm
P39	EMI request to mount snubber circuit	add PR406, PC406
P40	EMI request to mount snubber circuit	add PR506, PC506; PR516, PC516
PreMP : modification from PVT		
P34	increase precharge design margin	add PR12 1K
P35	change OTP setting	change PR15 to 23.2K, PR18 to 10.7K
P35	change source	chagne PC9 to SE070104280
P37	change 3/5V IC main source	change PU330 to TP851125A
P38	change 0.75V IC main source	change PU75 to G2992
P40	adjust loadline	change PR535 to 4.53K
P40	adjust transient stability	change PR527 to 220pF