

Compal confidential

LC-Marseille 10AD

PWWAE LA-6843P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

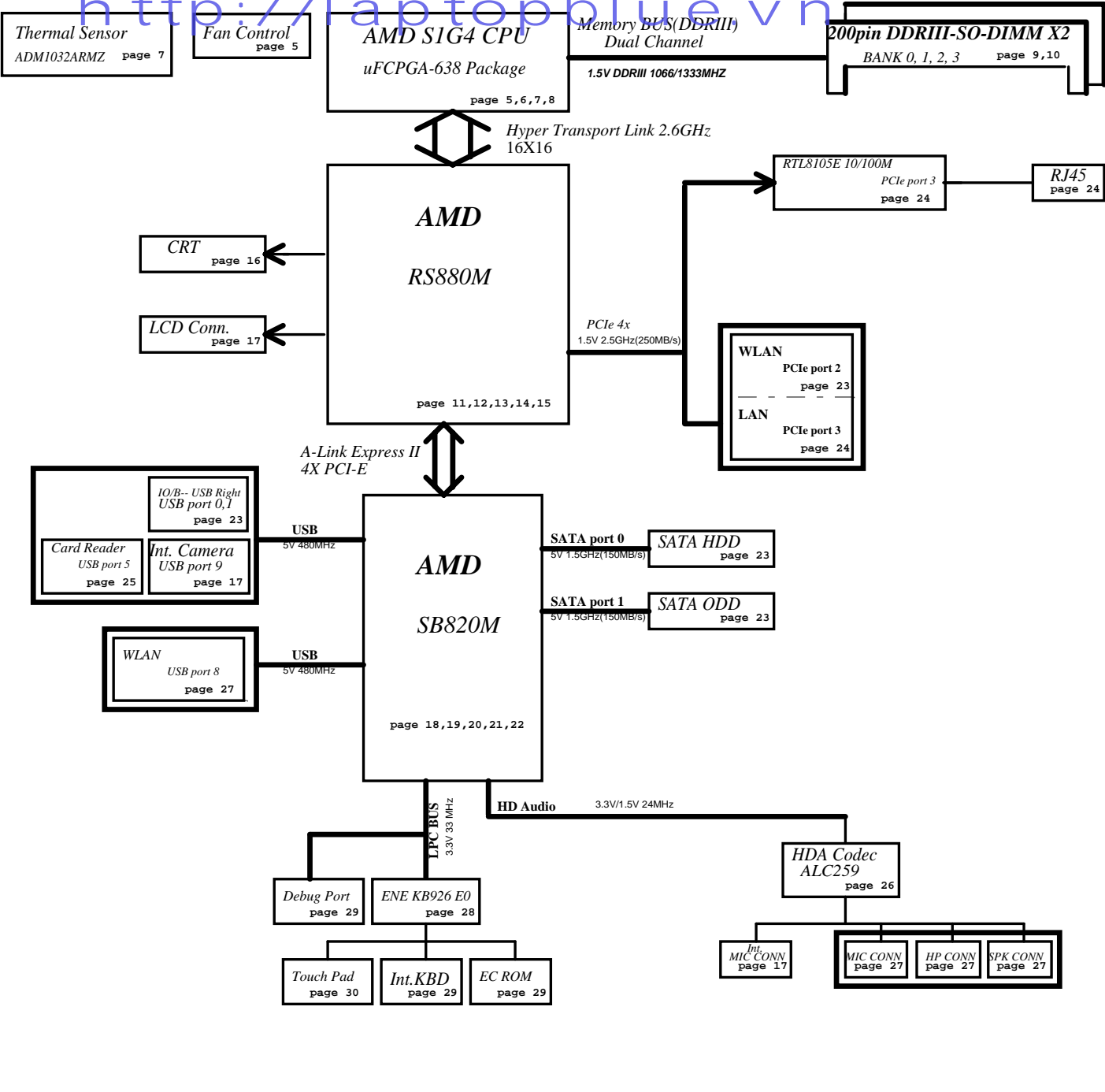
2010-08-16 Rev. 1.0

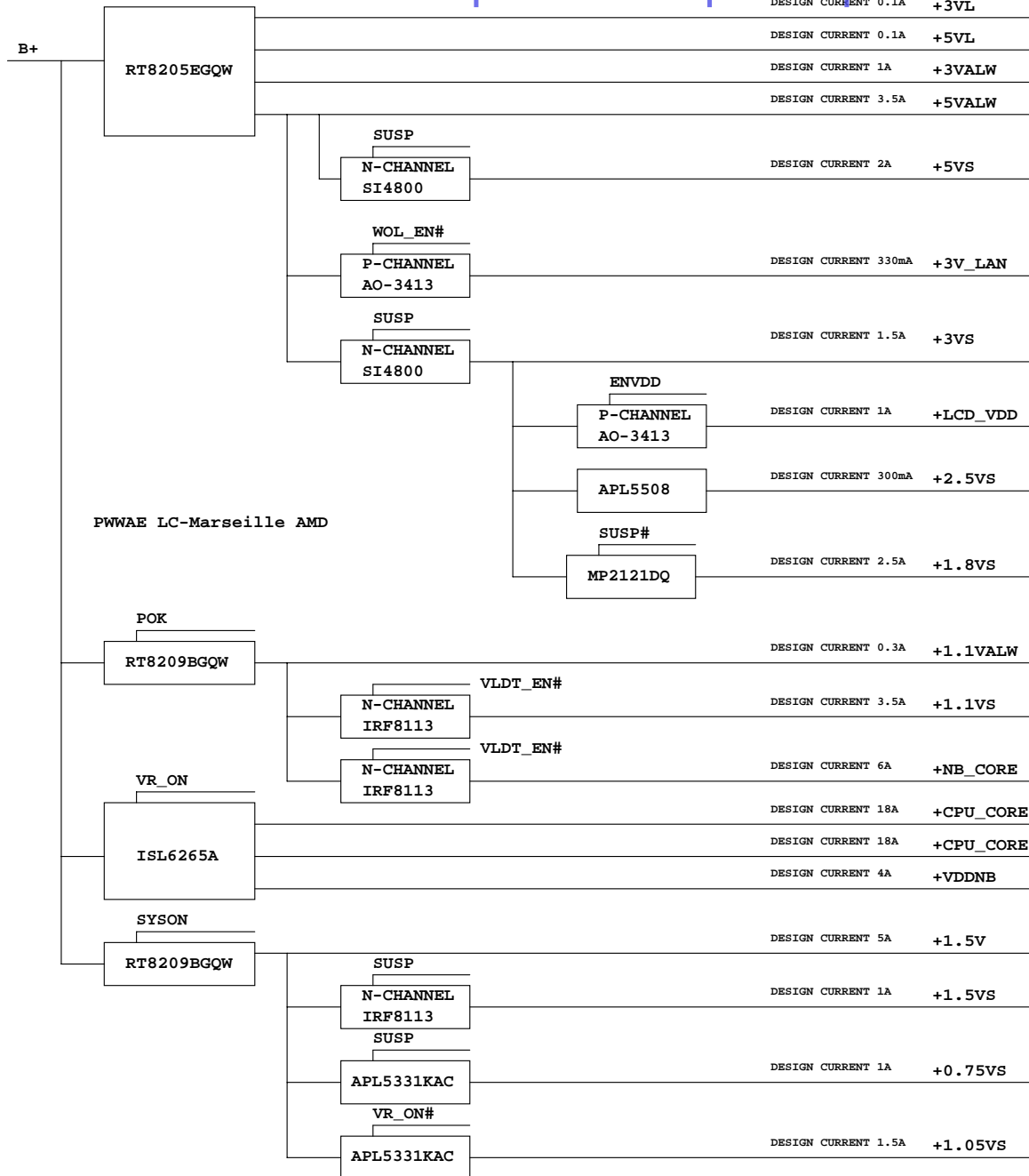
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Issued Date	2010-08-25	Deciphered Date	2010-08-25	Title	SCHEMATICS, MB A6843
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				Date:	Wednesday, September 01, 2010
				Sheet	1 of 40

Compal Confidential

Model Name : PWWAA

File Name : LA-6843P





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				Date	Wednesday, September 01, 2010
				Sheet	3 of 40

Voltage Rails

O : ON
X : OFF

power plane	State	+B +3VL +5VL +RTCVC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
EC KB926E0		

EC SM Bus2 address

Device	HEX	Address
EMC1032-1 CPU 98H		1001 100X b
EC KB926E0		

http://laptopblue.vn

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

@ : just reserve , no build
 SB820MR1@ : just reserve for SB820MR1 only
 R3@ : just reserve for R3 only
 CONN@ : just reserve for Connector only
 CAM@ : just reserve for WebCam only
 BT@ : just reserve for Blue Tooth only
 880MR1@: just reserve for 880MR1 only
 8105E_VC@: just reserve for 10/100 LAN VC version only
 8105E_VB@: just reserve for 10/100 LAN VBversion only

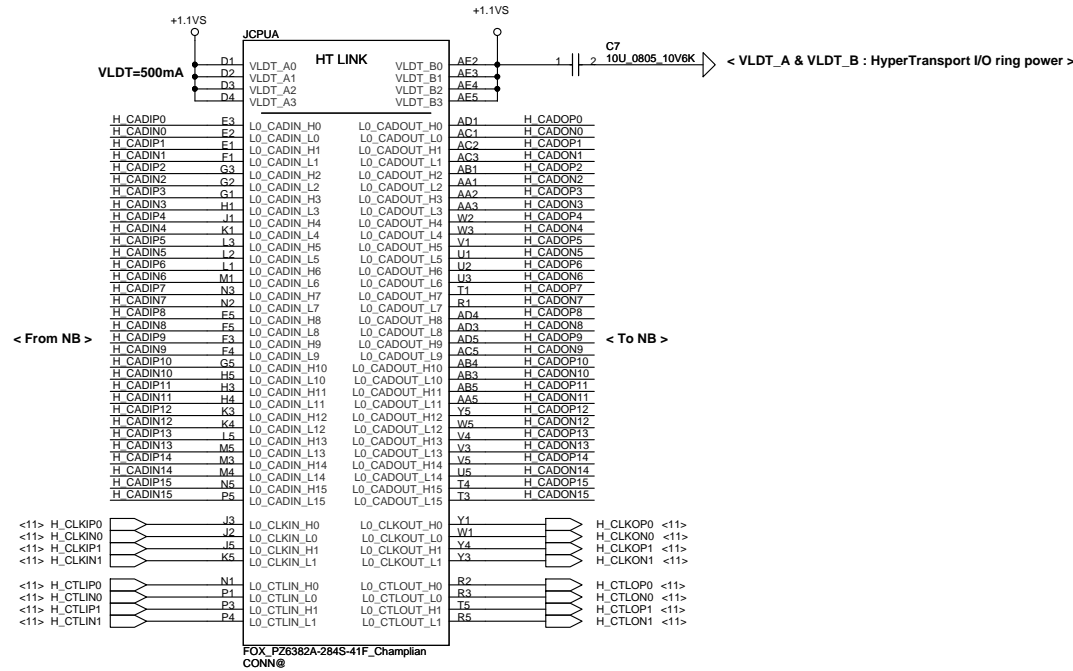
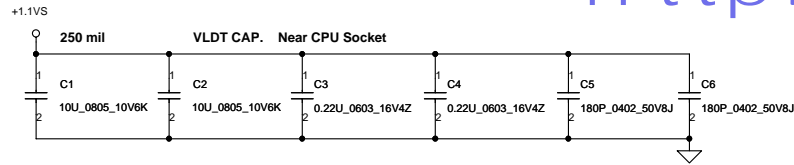
BTO (Build-To-Order) Option Table

Function	Camera					
Description	(C)					
Explain						
BTO	CAM@					

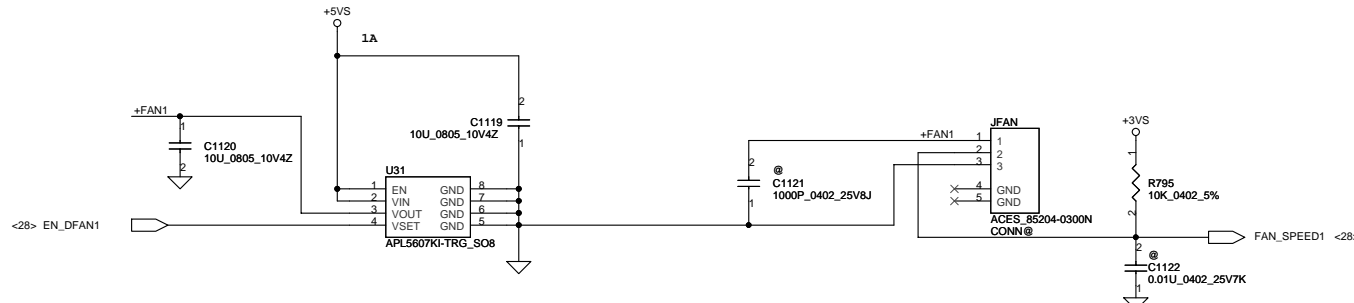
SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V					
EC_SMB_CK2 EC_SMB_DA2	KB926		V				
I2C_CLK I2C_DATA	RS880M						V
DDC_CLK0 DDC_DATA0	RS880M						
SCL0 SDA0	SB820			V	V		
SCL1 SDA1	SB820					V	

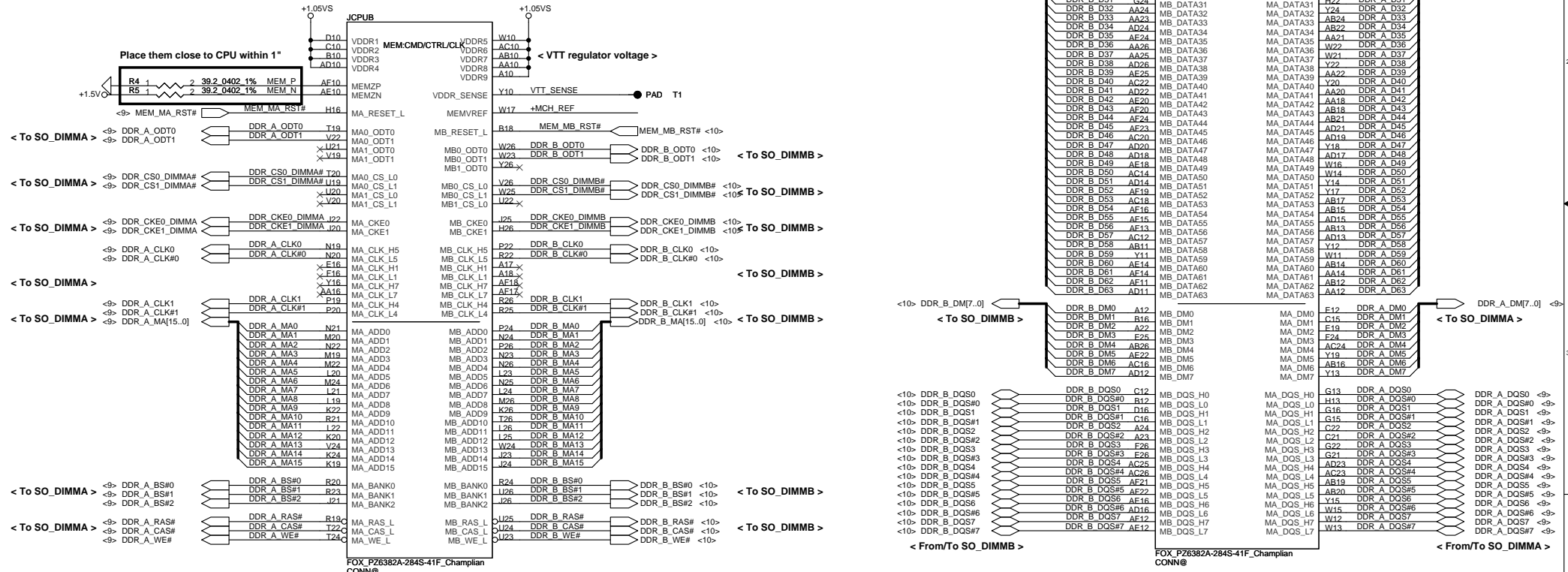
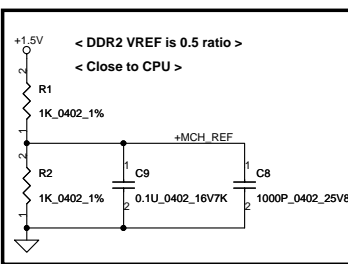
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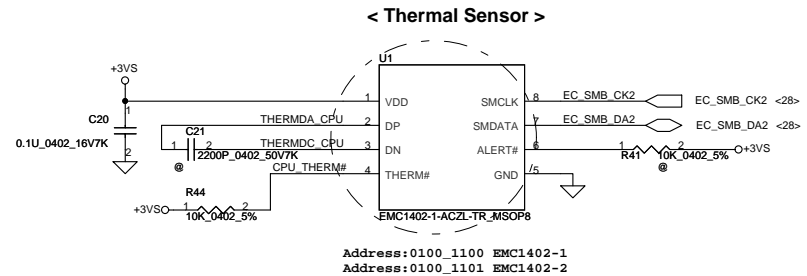
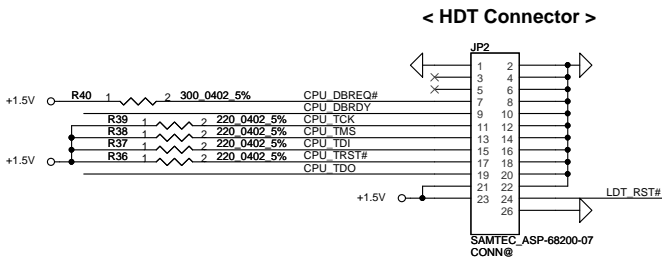
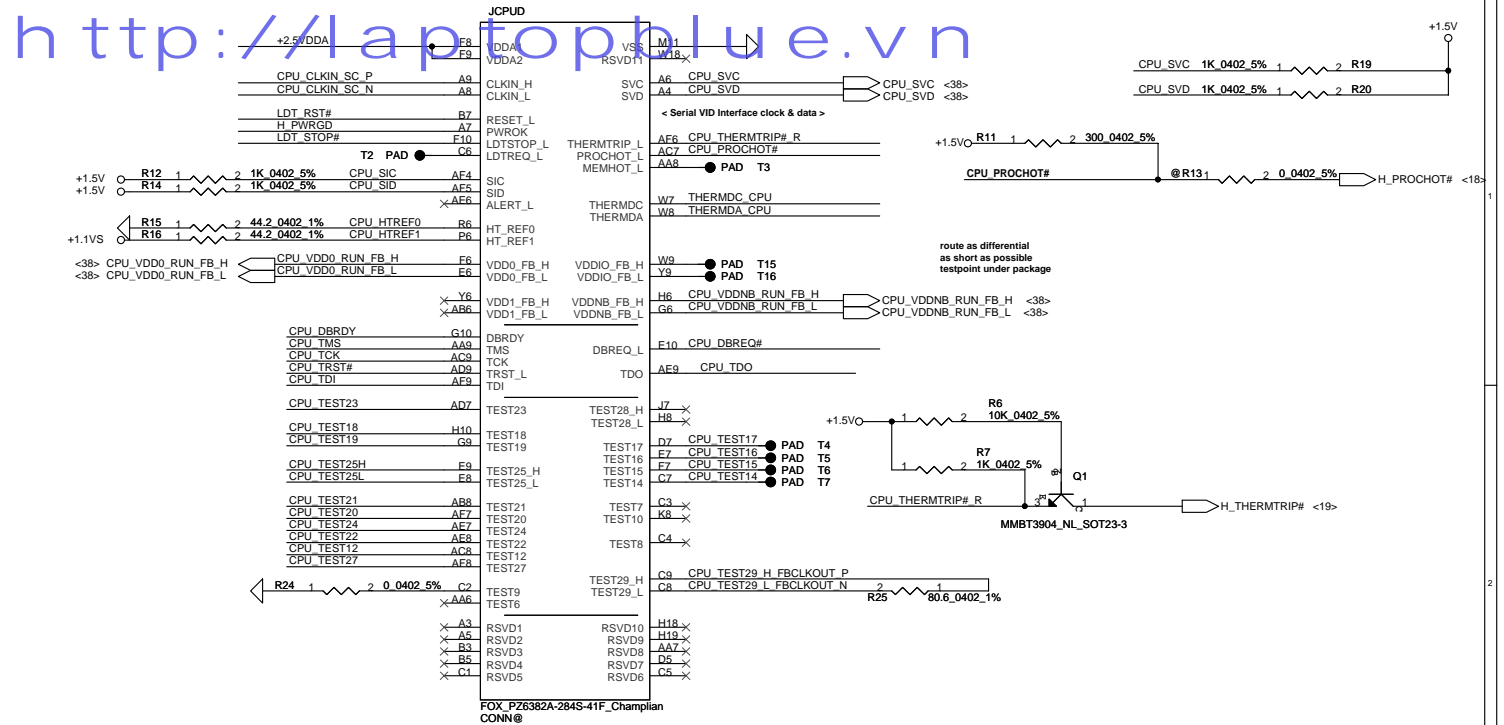
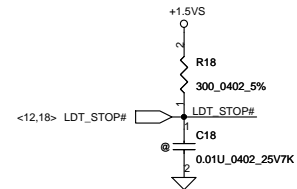
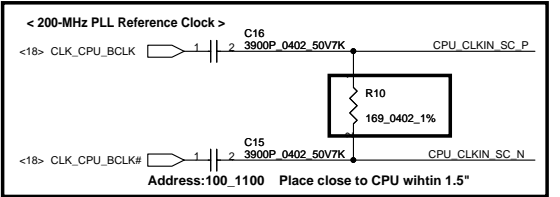


< FAN Control Circuit : Vout = 1.6 x Vset >



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						B	401982	B
						Date:	Wednesday, September 01, 2010	Sheet 5 of 40





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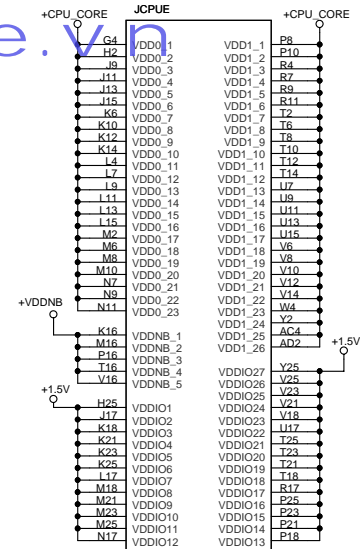
The diagram shows a laptop with the URL `http://laptopblue.vn` overlaid on its screen. To the right of the laptop is a detailed pinout diagram for a CPU. The diagram is divided into two main sections: **+CPU_CORE** and **JCPU**.

+CPU_CORE pins include:

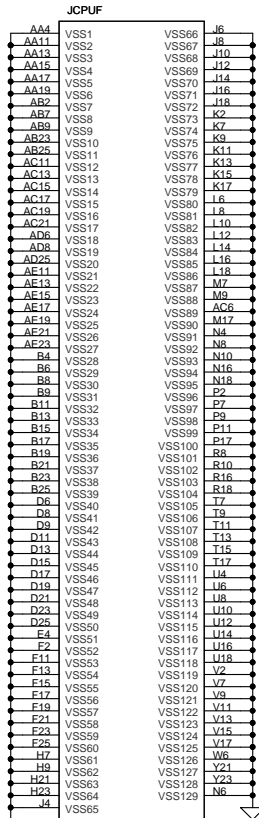
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- Pin 2: G2
- Pin 3: G3
- Pin 4: G1

JCPU pins include:

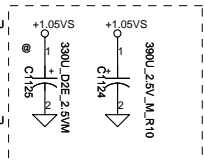
- Pin 1: VDD0_1
- Pin 2: VDD0_2
- Pin 3: VDD0_3
- Pin 4: VDD0_4
- Pin 5: VDD0_5
- Pin 6: VDD0_6
- Pin 7: VDD0_7
- Pin 8: VDD0_8
- Pin 9: VDD0_9
- Pin 10: VDD0_10
- Pin 11: VDD0_11
- Pin 12: VDD0_12
- Pin 13: VDD0_13
- Pin 14: VDD0_14
- Pin 15: VDD0_15
- Pin 16: VDD0_16
- Pin 17: VDD0_17
- Pin 18: VDD0_18
- Pin 19: VDD0_19
- Pin 20: VDD0_20
- Pin 21: VDD0_21
- Pin 22: VDD0_22
- Pin 23: VDD0_23
- Pin 24: VDD0_24
- Pin 25: VDD0_25
- Pin 26: VDD0_26
- Pin 27: VDD0_27
- Pin 28: VDD0_28
- Pin 29: VDD0_29
- Pin 30: VDD0_30
- Pin 31: VDD0_31
- Pin 32: VDD0_32
- Pin 33: VDD0_33
- Pin 34: VDD0_34
- Pin 35: VDD0_35
- Pin 36: VDD0_36
- Pin 37: VDD0_37
- Pin 38: VDD0_38
- Pin 39: VDD0_39
- Pin 40: VDD0_40
- Pin 41: VDD0_41
- Pin 42: VDD0_42
- Pin 43: VDD0_43
- Pin 44: VDD0_44
- Pin 45: VDD0_45
- Pin 46: VDD0_46
- Pin 47: VDD0_47
- Pin 48: VDD0_48
- Pin 49: VDD0_49
- Pin 50: VDD0_50
- Pin 51: VDD0_51
- Pin 52: VDD0_52
- Pin 53: VDD0_53
- Pin 54: VDD0_54
- Pin 55: VDD0_55
- Pin 56: VDD0_56
- Pin 57: VDD0_57
- Pin 58: VDD0_58
- Pin 59: VDD0_59
- Pin 60: VDD0_60
- Pin 61: VDD0_61
- Pin 62: VDD0_62
- Pin 63: VDD0_63
- Pin 64: VDD0_64
- Pin 65: VDD0_65
- Pin 66: VDD0_66
- Pin 67: VDD0_67
- Pin 68: VDD0_68
- Pin 69: VDD0_69
- Pin 70: VDD0_70
- Pin 71: VDD0_71
- Pin 72: VDD0_72
- Pin 73: VDD0_73
- Pin 74: VDD0_74
- Pin 75: VDD0_75
- Pin 76: VDD0_76
- Pin 77: VDD0_77
- Pin 78: VDD0_78
- Pin 79: VDD0_79
- Pin 80: VDD0_80
- Pin 81: VDD0_81
- Pin 82: VDD0_82
- Pin 83: VDD0_83
- Pin 84: VDD0_84
- Pin 85: VDD0_85
- Pin 86: VDD0_86
- Pin 87: VDD0_87
- Pin 88: VDD0_88
- Pin 89: VDD0_89
- Pin 90: VDD0_90
- Pin 91: VDD0_91
- Pin 92: VDD0_92
- Pin 93: VDD0_93
- Pin 94: VDD0_94
- Pin 95: VDD0_95
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- Pin 98: VDD0_98
- Pin 99: VDD0_99
- Pin 100: VDD0_100



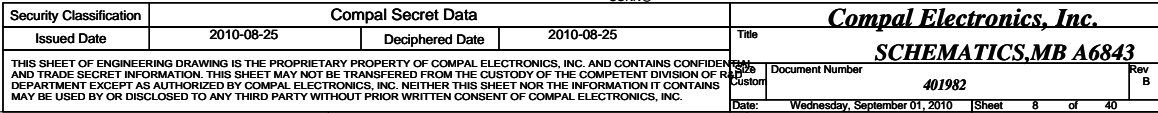
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CONN@

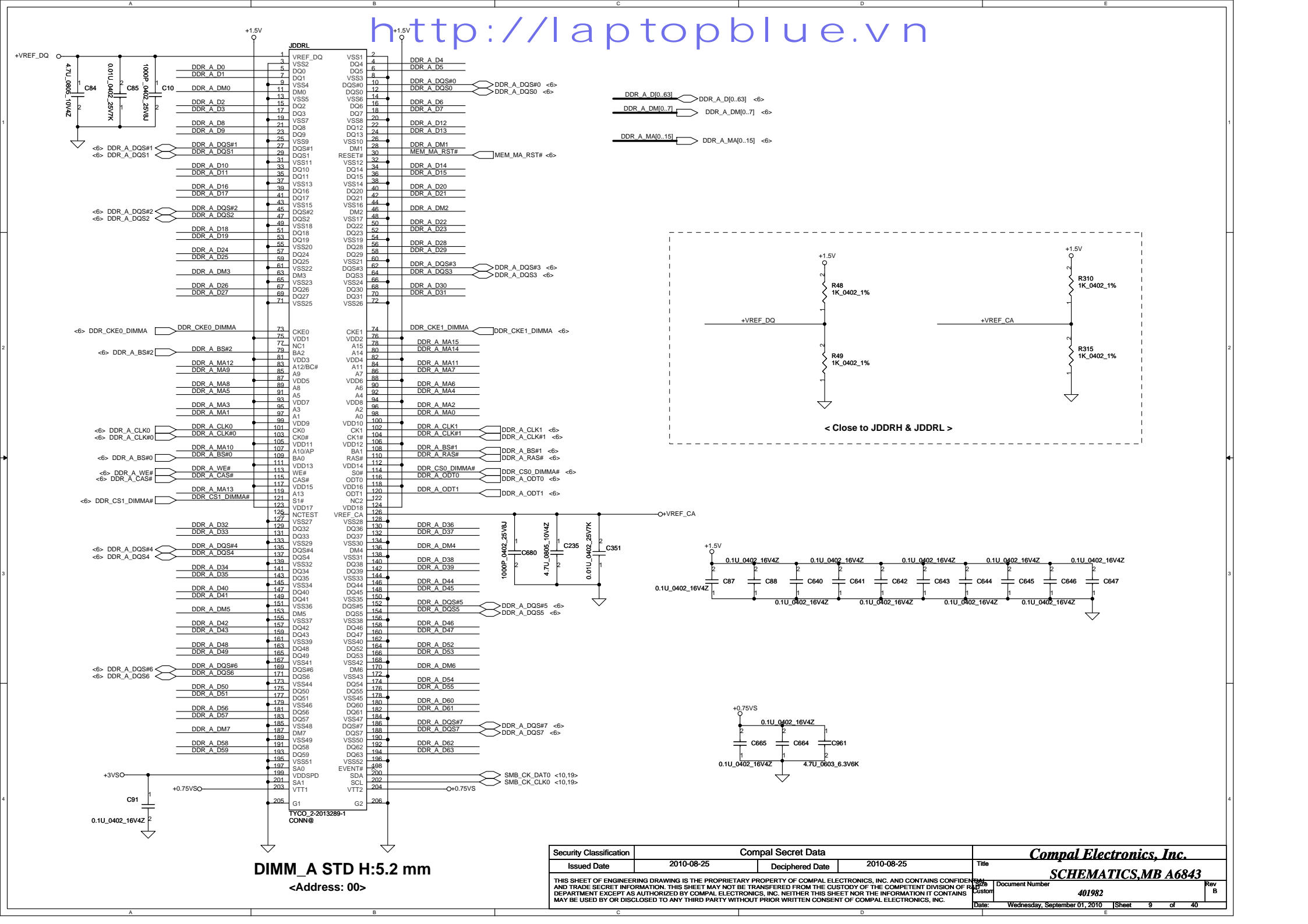
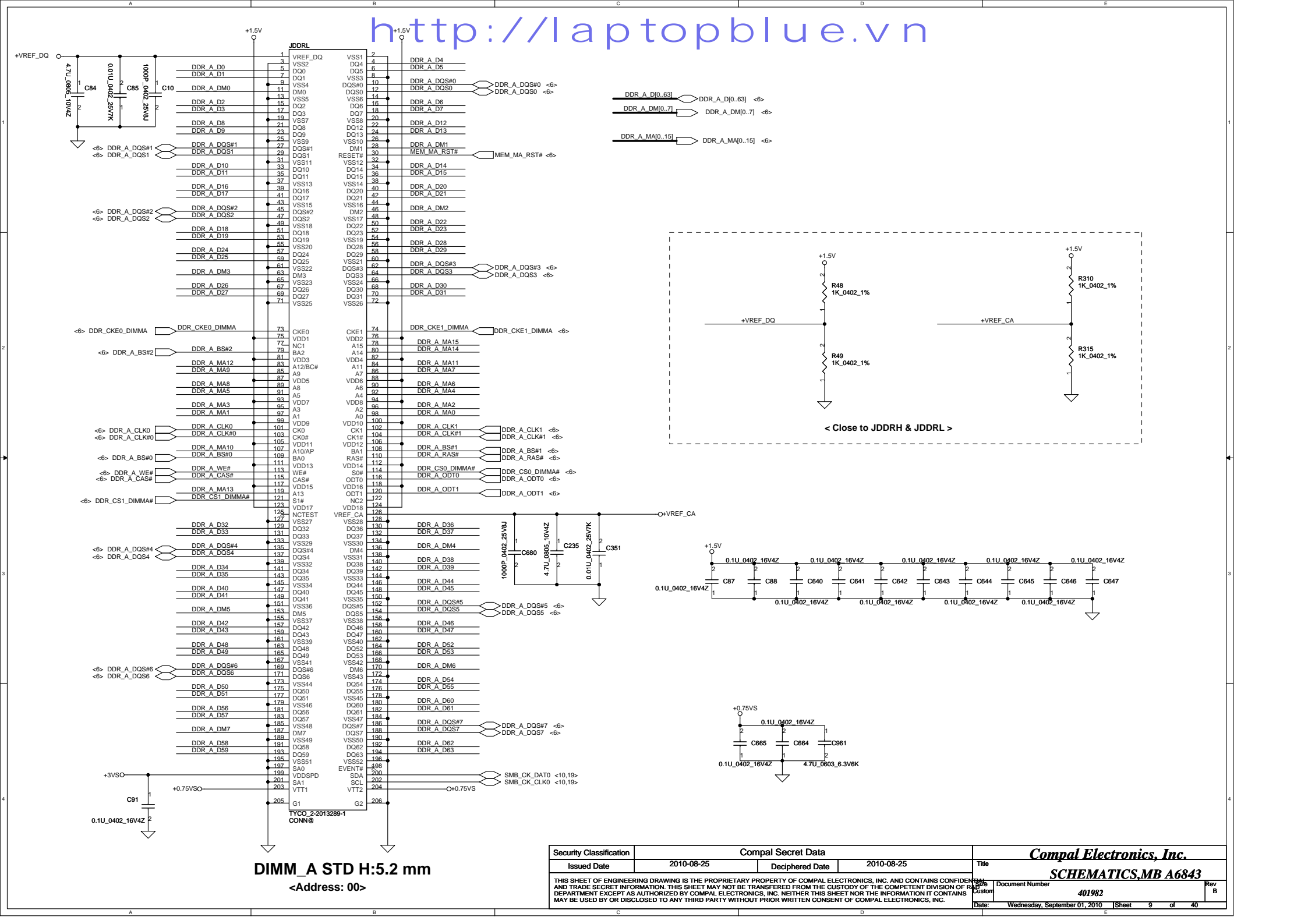


C1124 Co-layout with C1125



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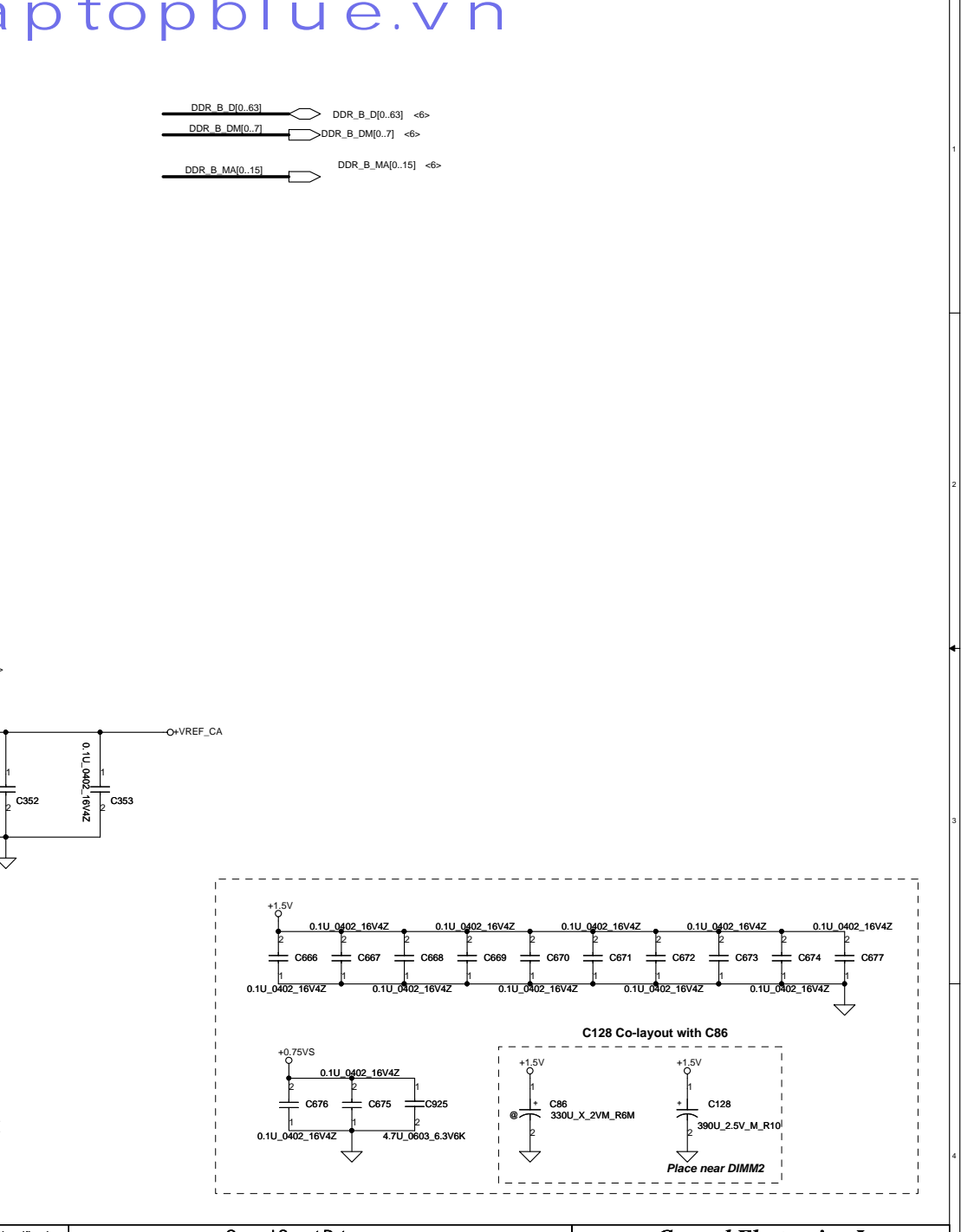
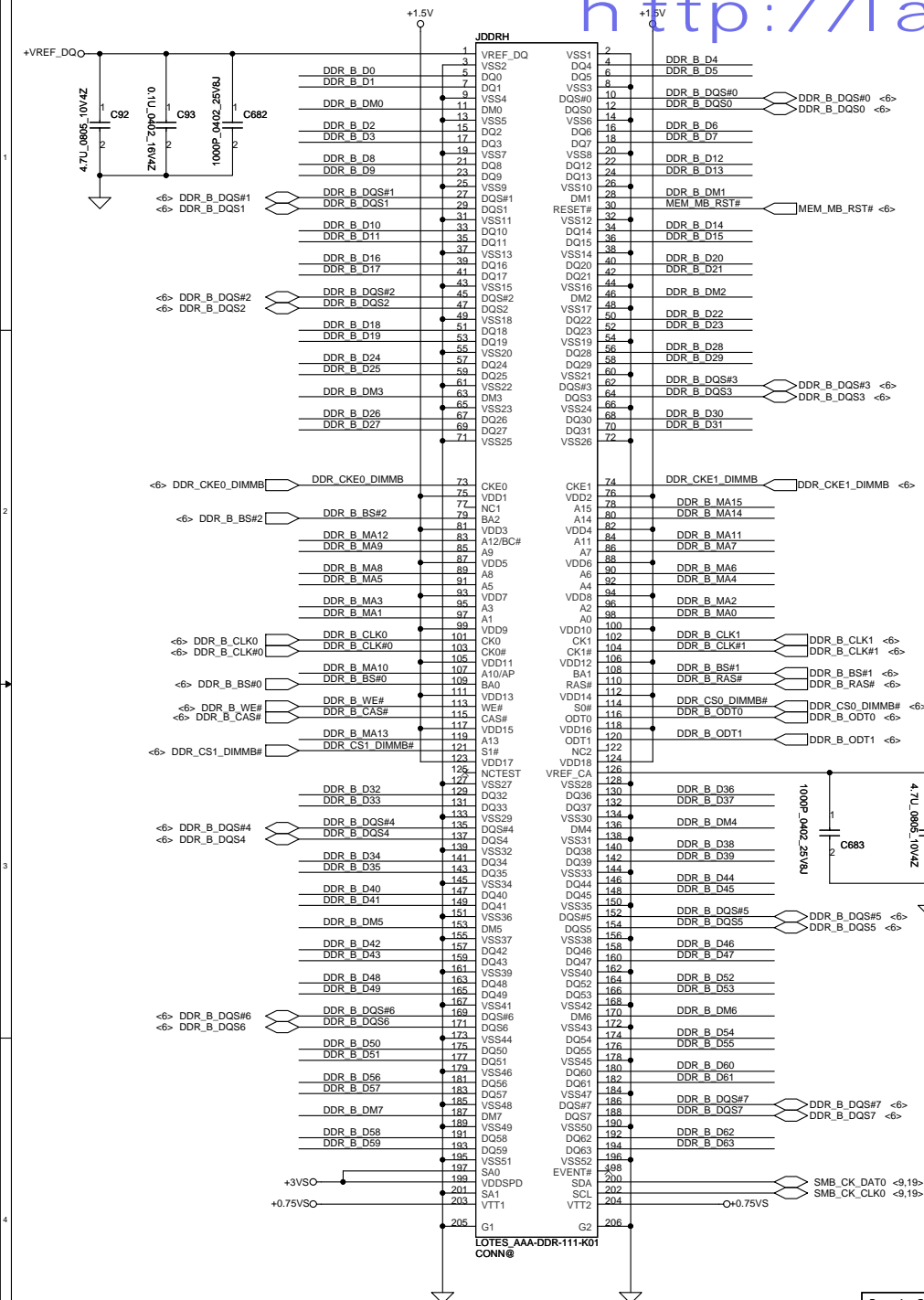


http://laptopblue.vn

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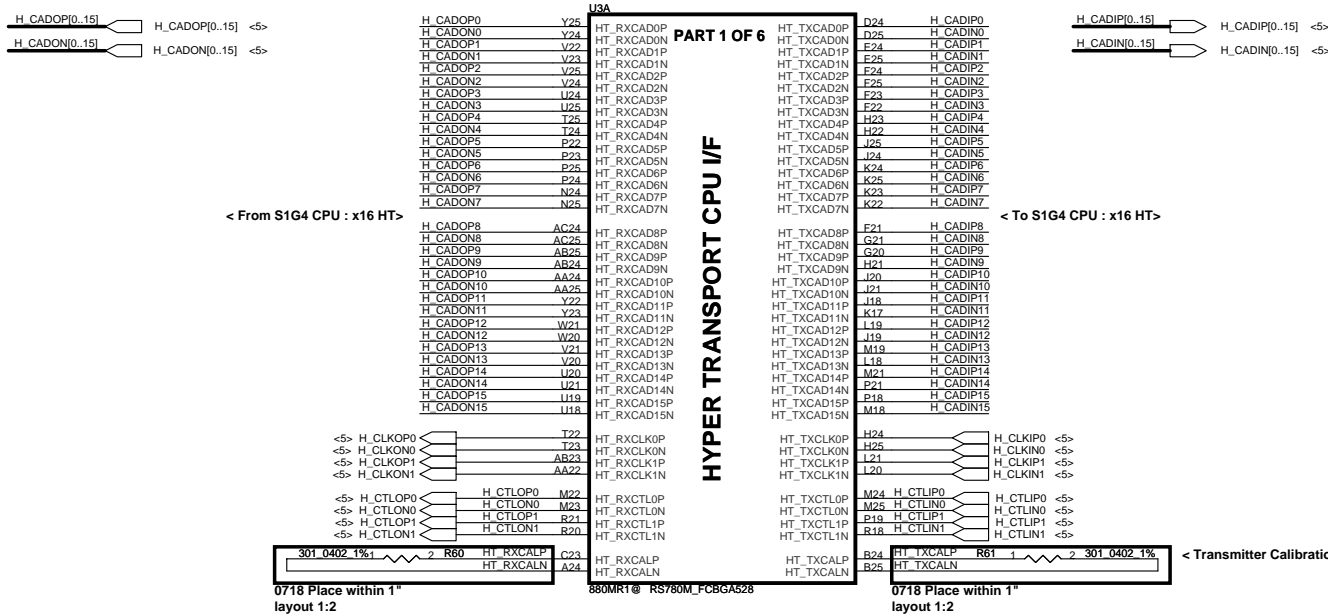
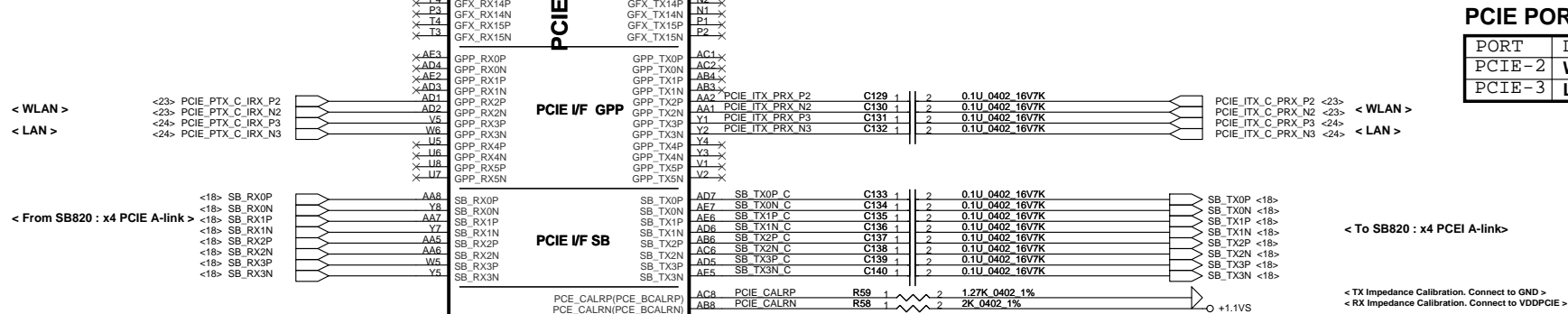
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5	VREF_DQ	135	QD36
6	VREF_DQ	136	QD37
7	VREF_DQ	137	QD38
8	VREF_DQ	138	QD39
9	VREF_DQ	139	QD40
10	VREF_DQ	140	QD41
11	VREF_DQ	141	QD42
12	VREF_DQ	142	QD43
13	VREF_DQ	143	QD44
14	VREF_DQ	144	QD45
15	VREF_DQ	145	QD46
16	VREF_DQ	146	QD47
17	VREF_DQ	147	QD48
18	VREF_DQ	148	QD49
19	VREF_DQ	149	QD50
20	VREF_DQ	150	QD51
21	VREF_DQ	151	QD52
22	VREF_DQ	152	QD53
23	VREF_DQ	153	QD54
24	VREF_DQ	154	QD55
25	VREF_DQ	155	QD56
26	VREF_DQ	156	QD57
27	VREF_DQ	157	QD58
28	VREF_DQ	158	QD59
29	VREF_DQ	159	QD60
30	VREF_DQ	160	QD61
31	VREF_DQ	161	QD62
32	VREF_DQ	162	QD63
33	VREF_DQ	163	QD64
34	VREF_DQ	164	QD65
35	VREF_DQ	165	QD66
36	VREF_DQ	166	QD67
37	VREF_DQ	167	QD68
38	VREF_DQ	168	QD69
39	VREF_DQ	169	QD70
40	VREF_DQ	170	QD71
41	VREF_DQ	171	QD72
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50	VREF_DQ	180	QD81
51	VREF_DQ	181	QD82
52	VREF_DQ	182	QD83
53	VREF_DQ	183	QD84
54	VREF_DQ	184	QD85
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58	VREF_DQ	188	QD89
59	VREF_DQ	189	QD90
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http://laptopblue.vn

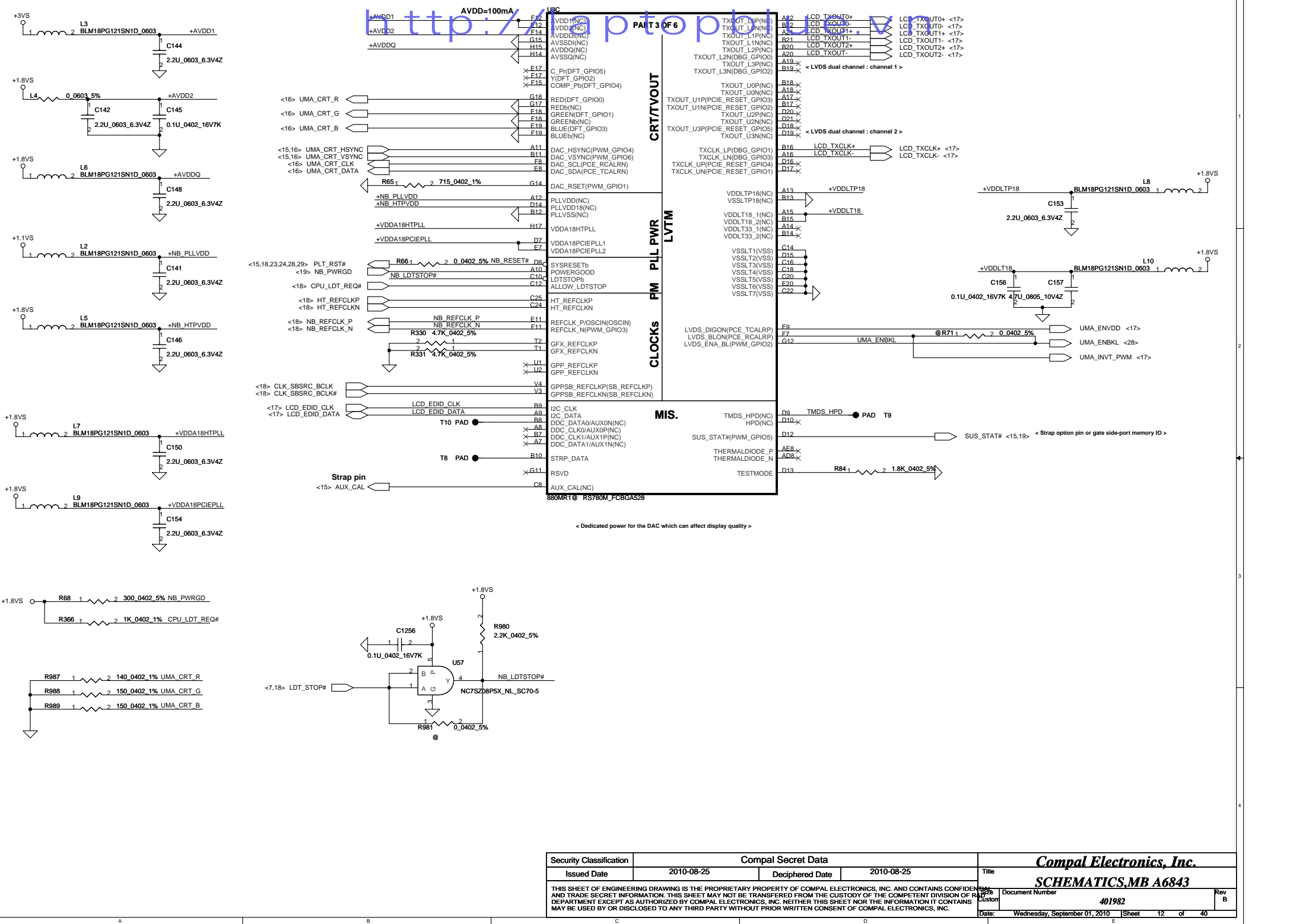


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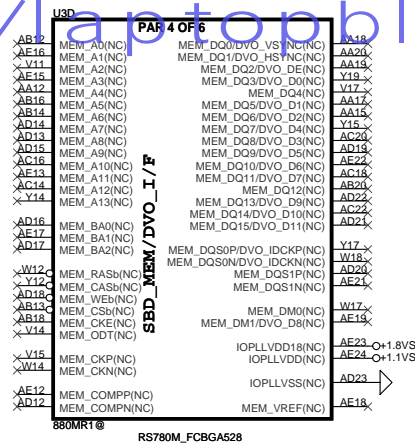
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				401982	
Date: Wednesday, September 01, 2010				Sheet 10	of 40



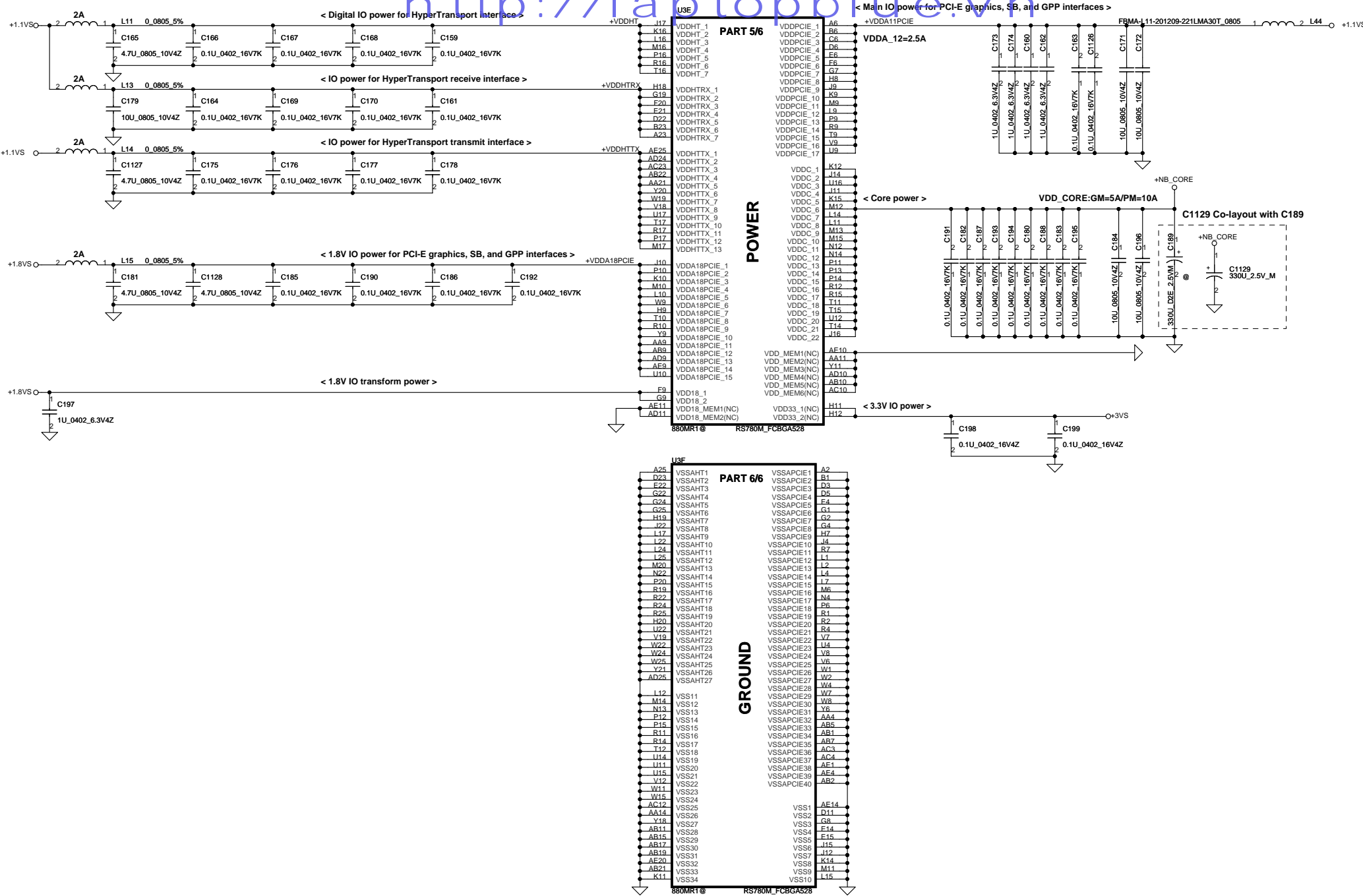
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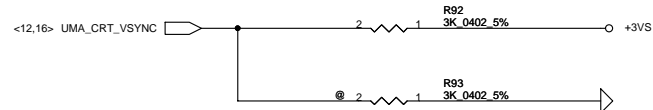
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				Date	Wednesday, September 01, 2010
				Sheet	13 of 40
				Rev	B



< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

PIN: RS880--> VSYNC#

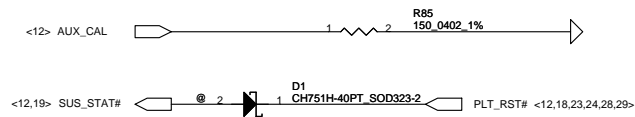
< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



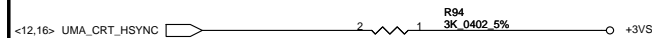
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

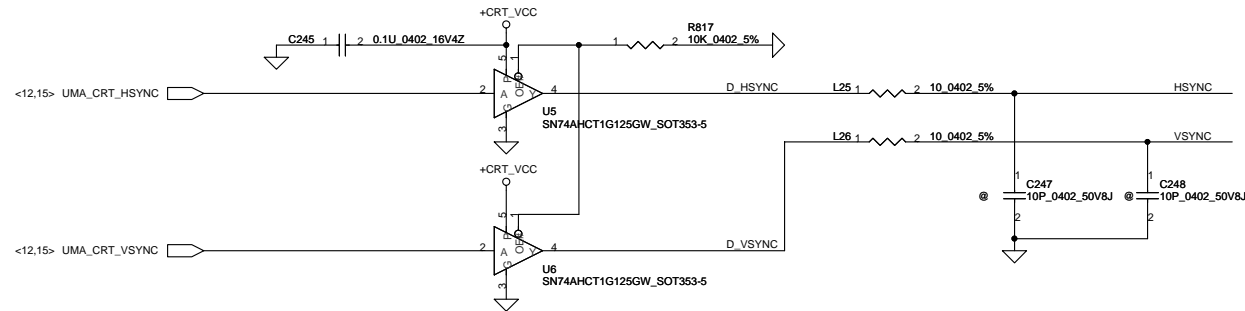
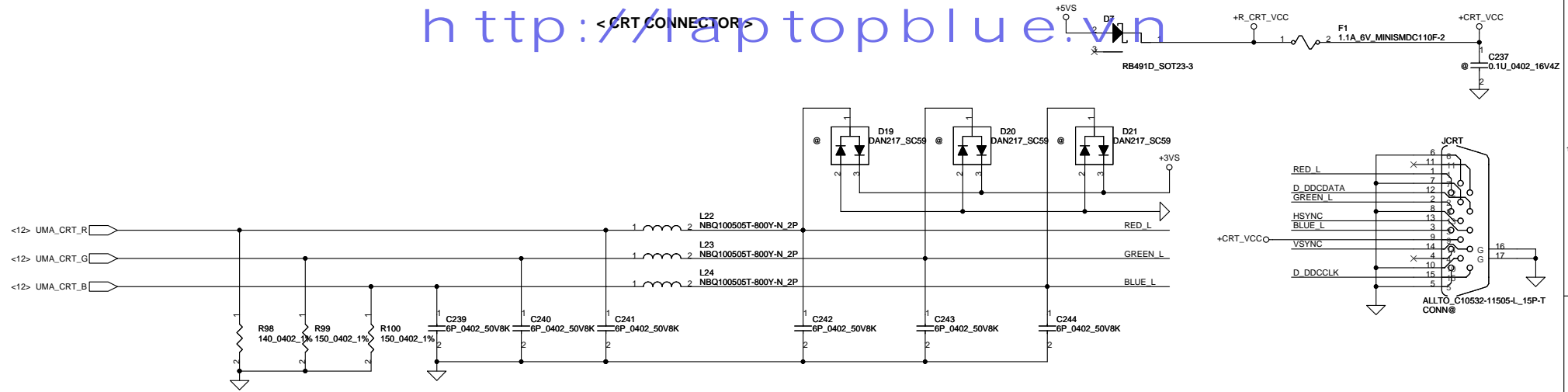
RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

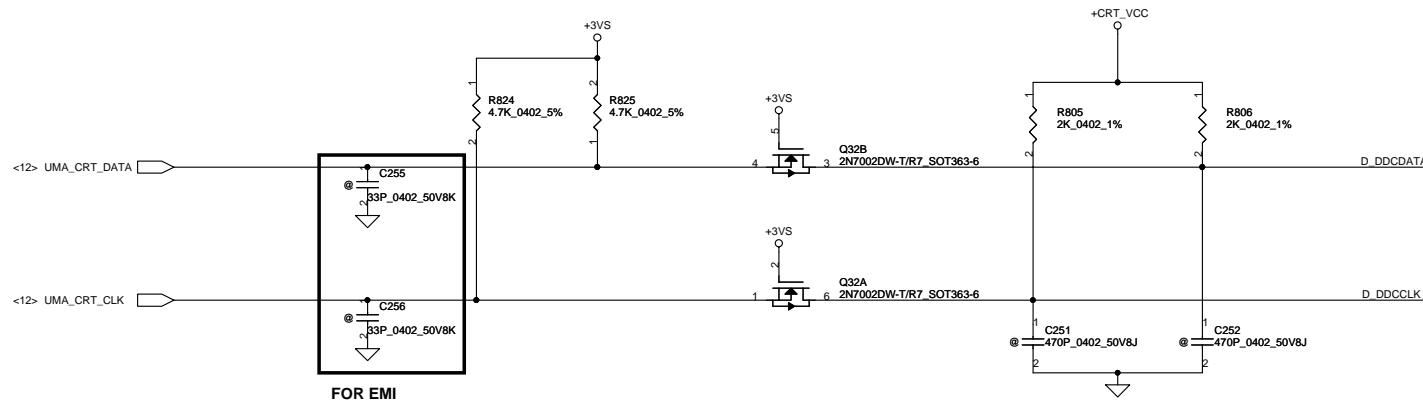
RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

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				Date	Wednesday, September 01, 2010
				Sheet	15 of 40



< SYNC SIGNAL >

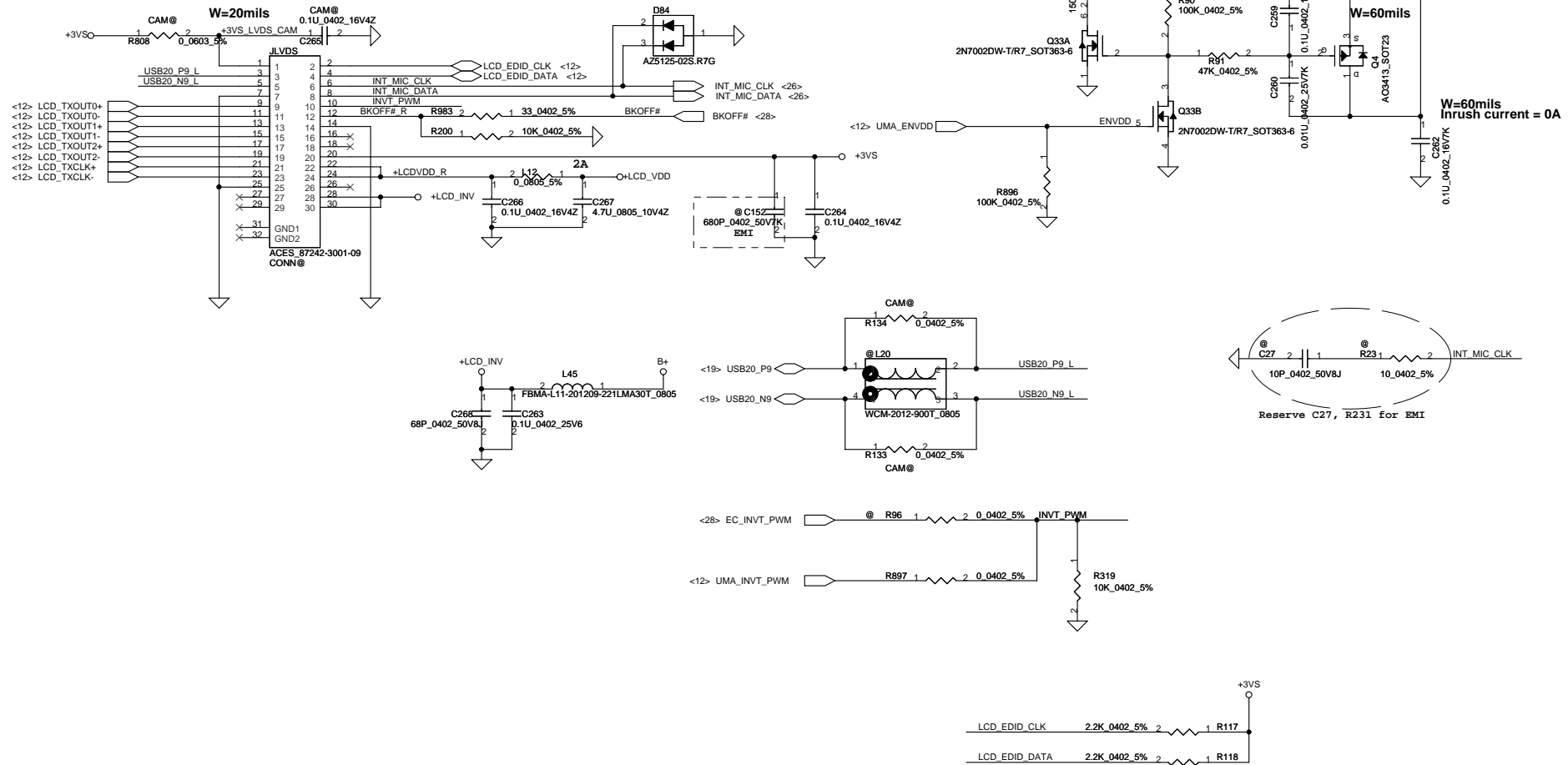


< Display Data Channel >

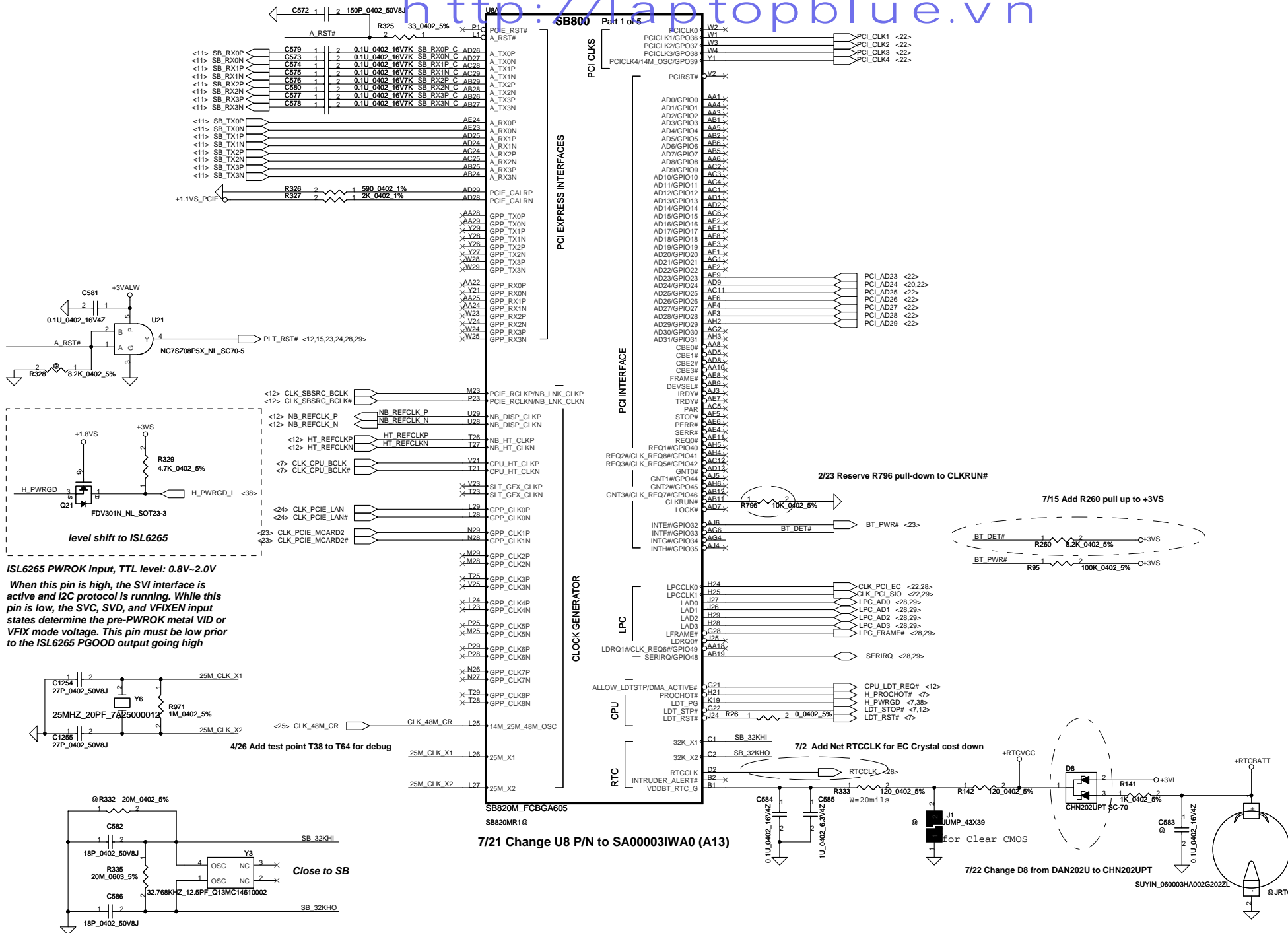
FOR EMI

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Date:	Wednesday, September 01, 2010	Sheet	16	of	40

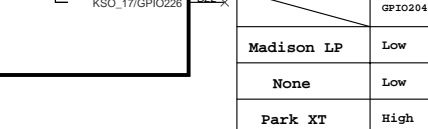
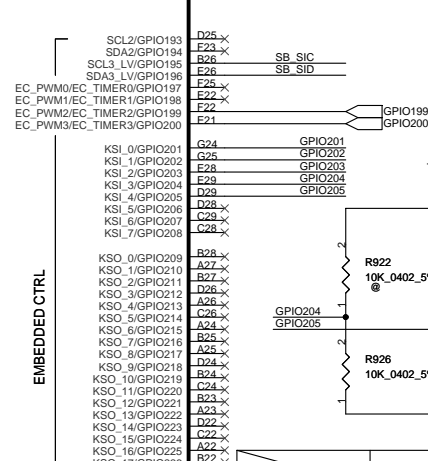
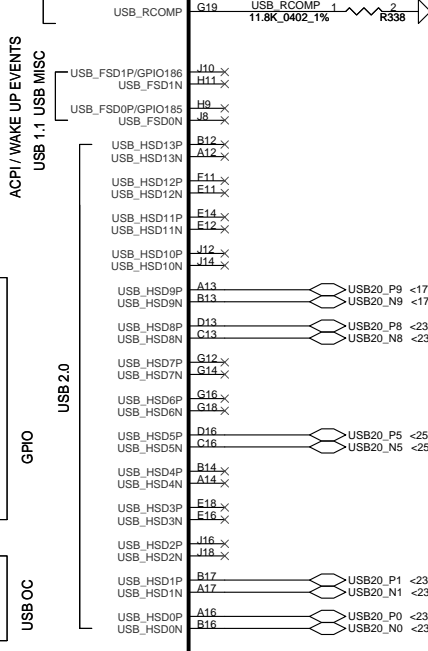
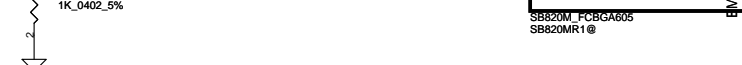
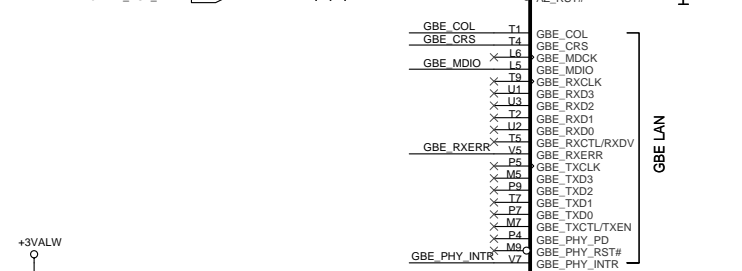
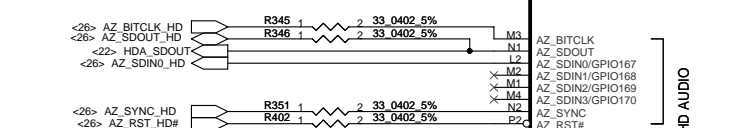
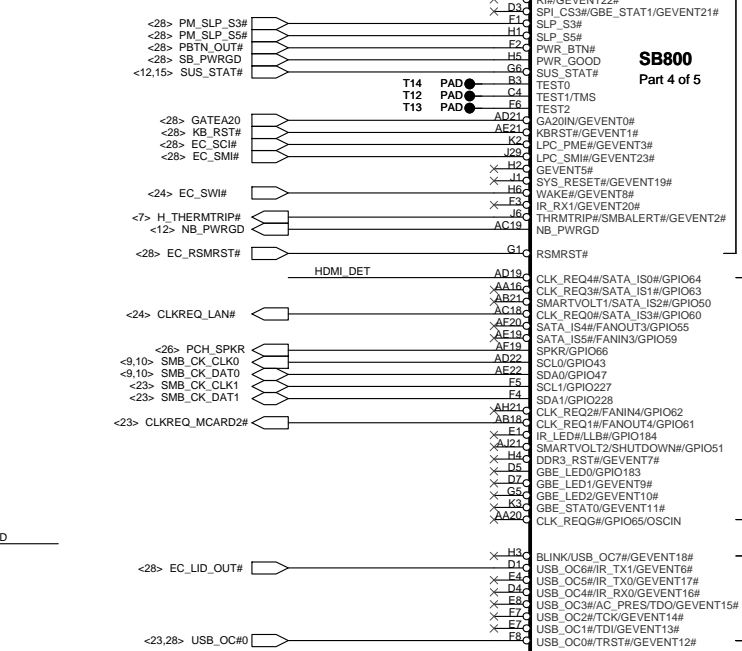
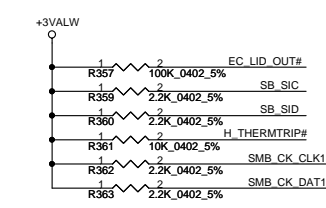
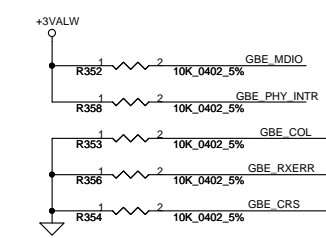
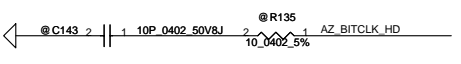
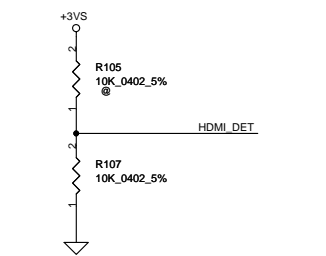
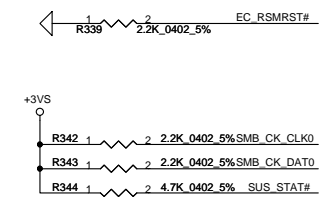
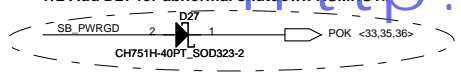
LCD/PANEL BD. Conn.



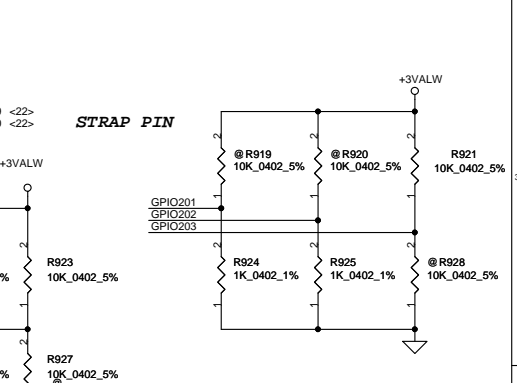
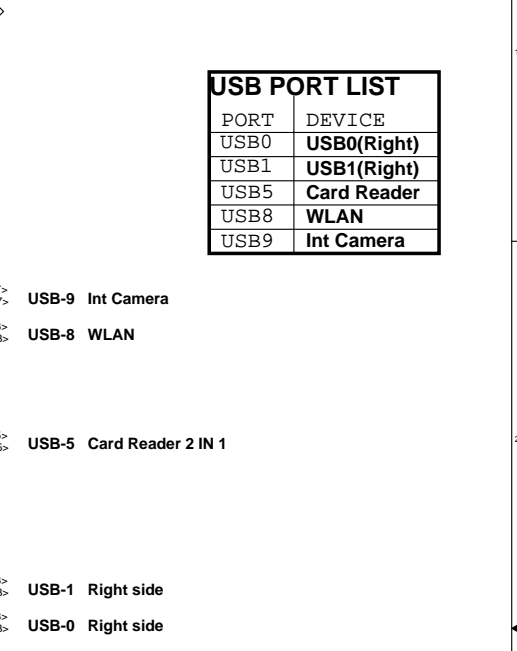
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				401982	
				Date:	Wednesday, September 01, 2010
				Sheet	17 of 40



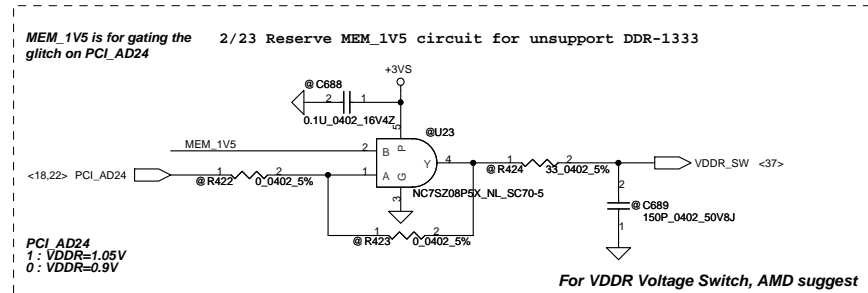
7/2 Add D27 for abnormal shutdown RSMRST#



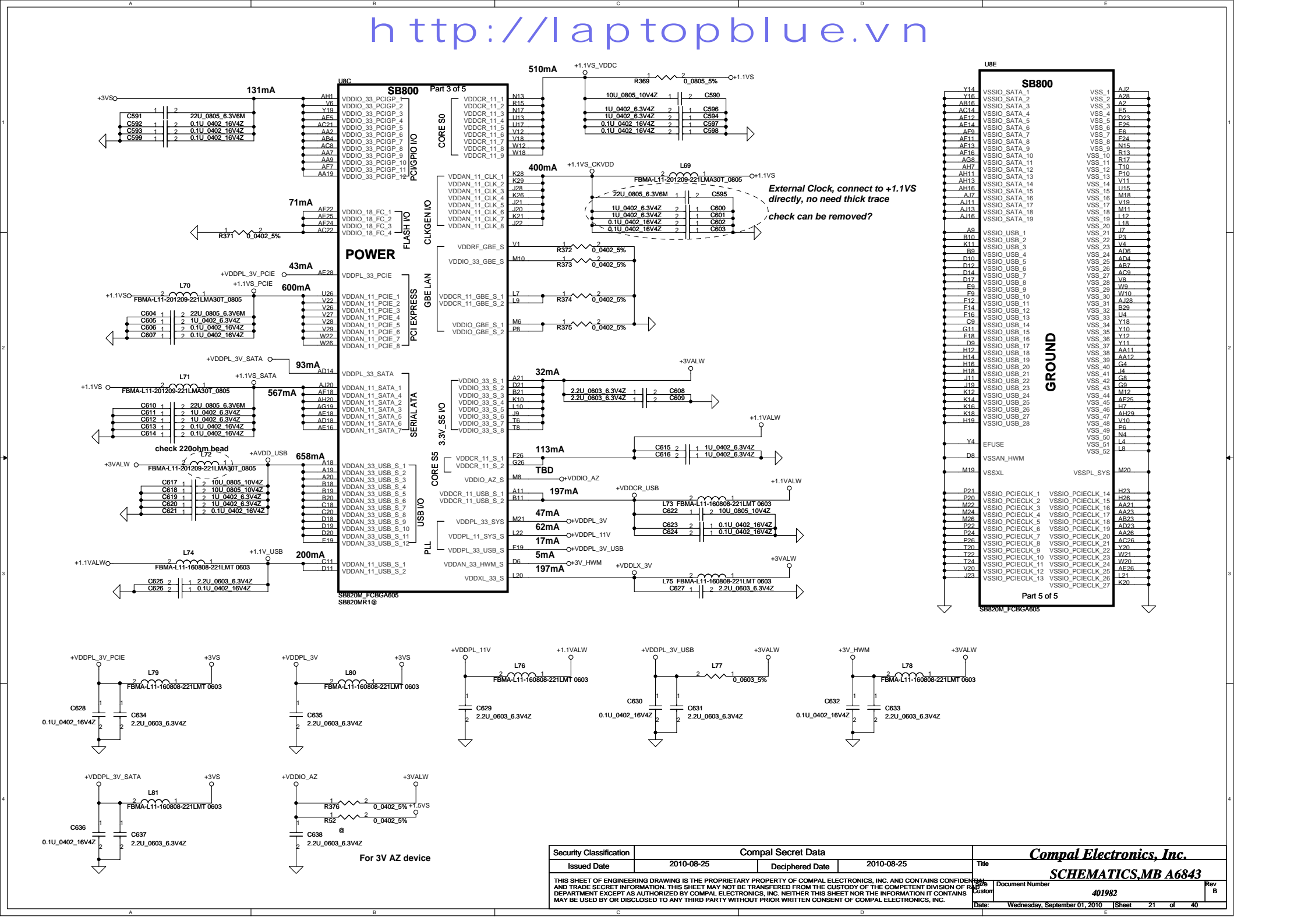
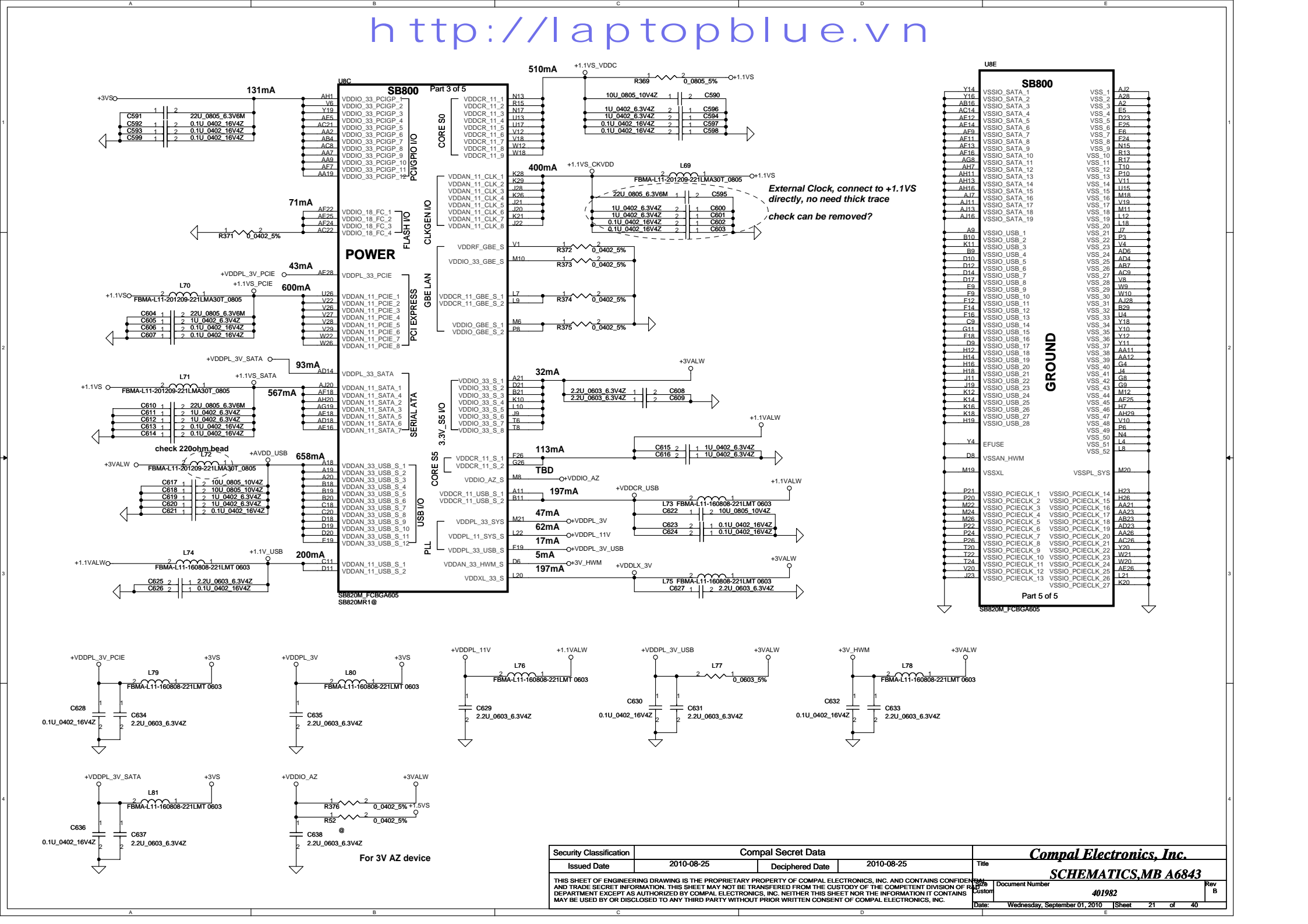
USB PORT LIST	
PORT	DEVICE
USB0	USB0(Right)
USB1	USB1(Right)
USB5	Card Reader
USB8	WLAN
USB9	Int Camera



	GPIO201	GPIO202	GPIO203
Nile-M	High	High	High
Nile-S	High	High	Low
Danube Marseille	Low	Low	Low
Danube Hamburg	Low	Low	High
Danube LC Marseille	Low	Low	High



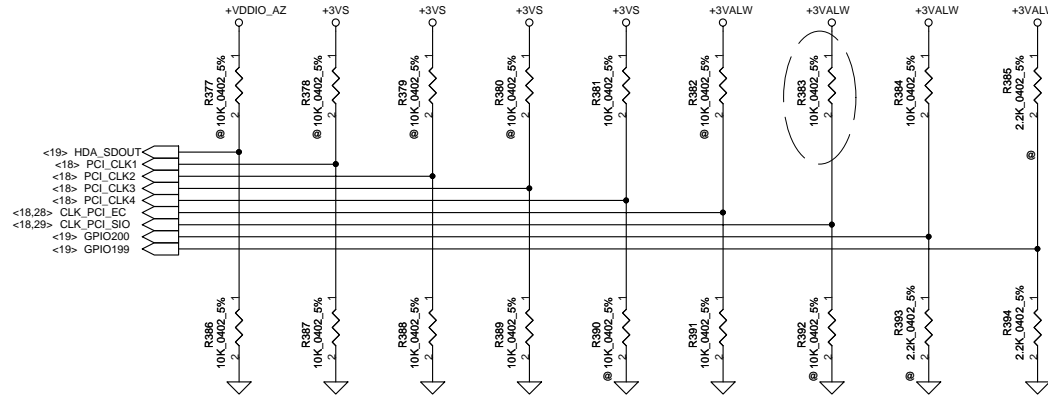
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				Rev B	401982
				Date:	Wednesday, September 01, 2010

[illegible]

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE	L,H = LPC ROM L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



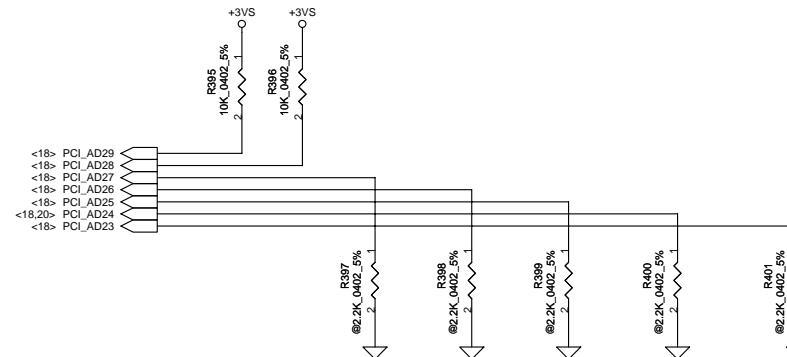
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

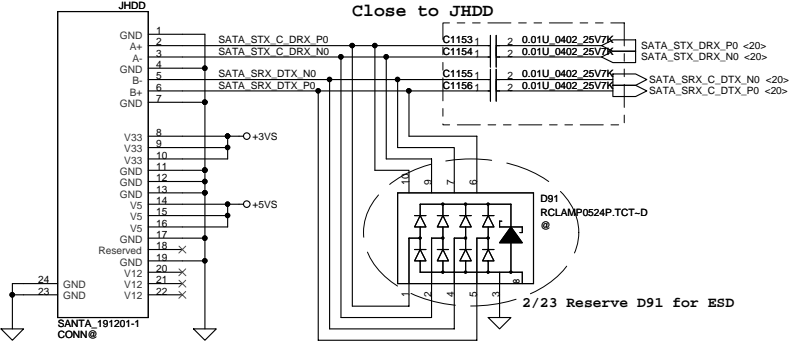
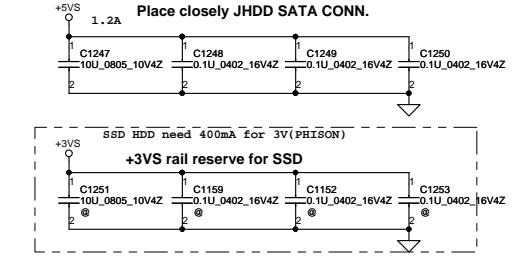
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

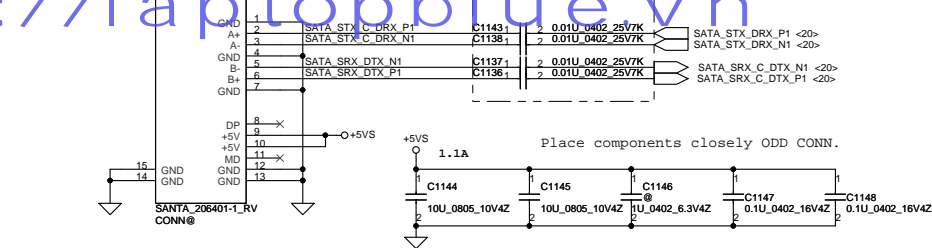
check default



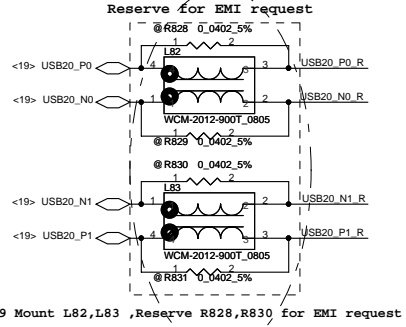
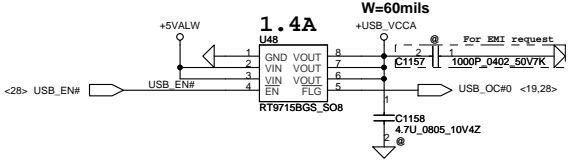
SATA HDD Conn.



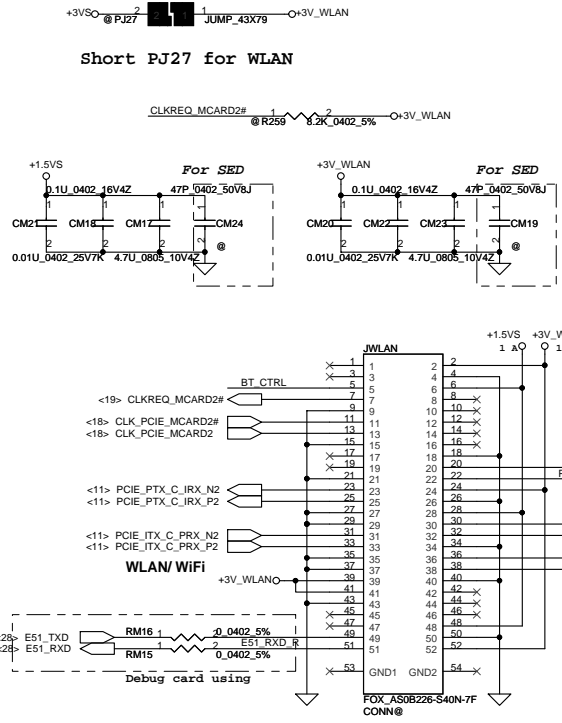
SATA HDD Conn



USB Port 0 & Port1



Slot#1 Half PCIe Mini Card-WLAN



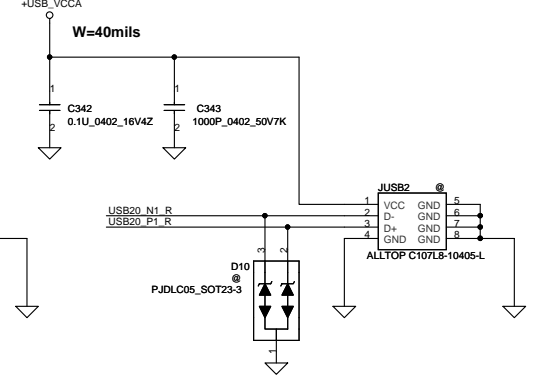
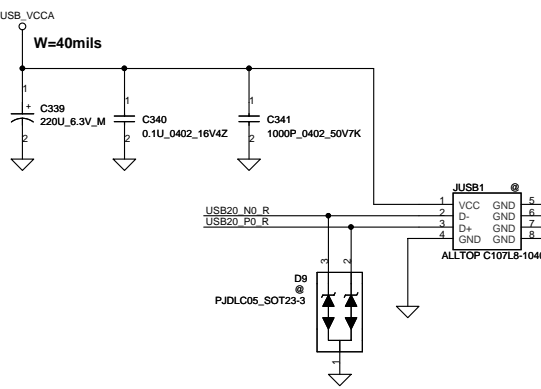
WLAN&BT Combo module circuits

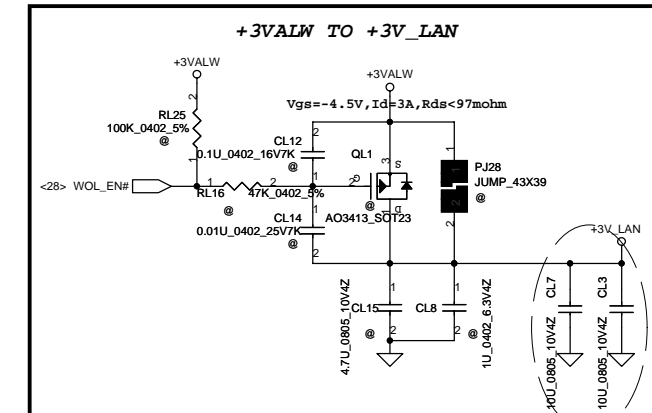
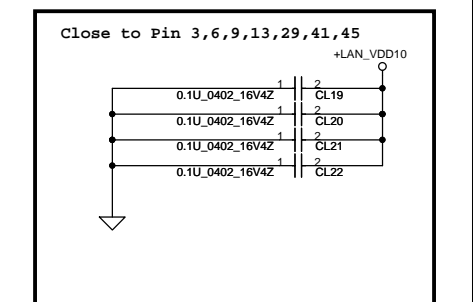
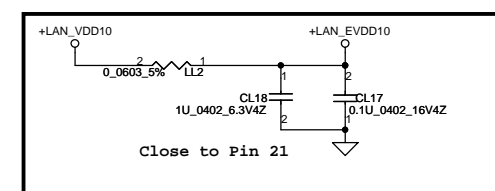
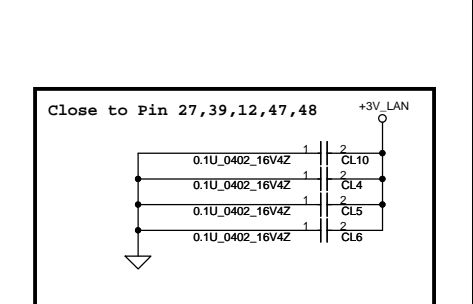
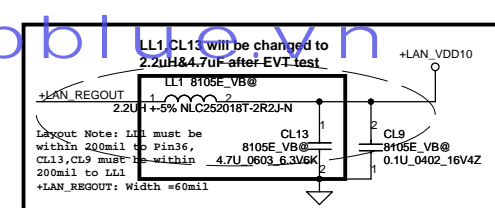
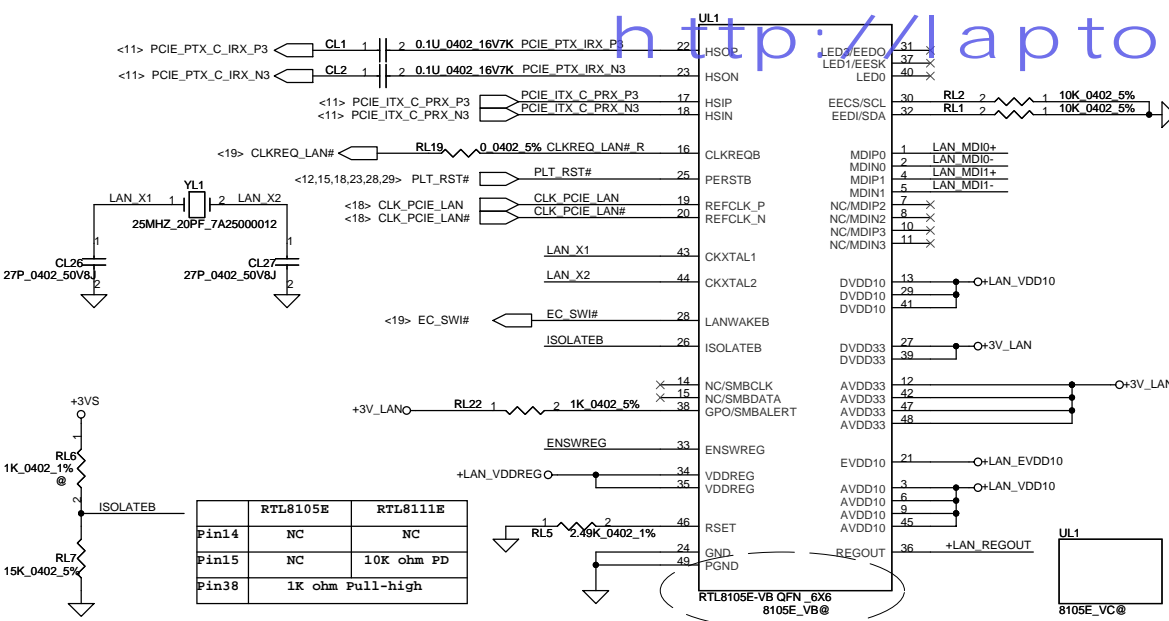
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove DM2

7/25 Reserver DM2 for +3V_WLAN is +3VS

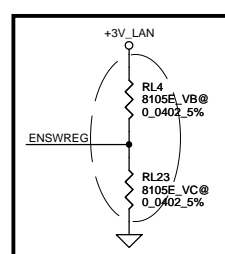
7/25 Add R50 for Intel Rainbow Peak module





7/16 Change UL1 from RTL8105E-VB (SA00003PO10) to RTL8105E-VC (SA00003PO20)

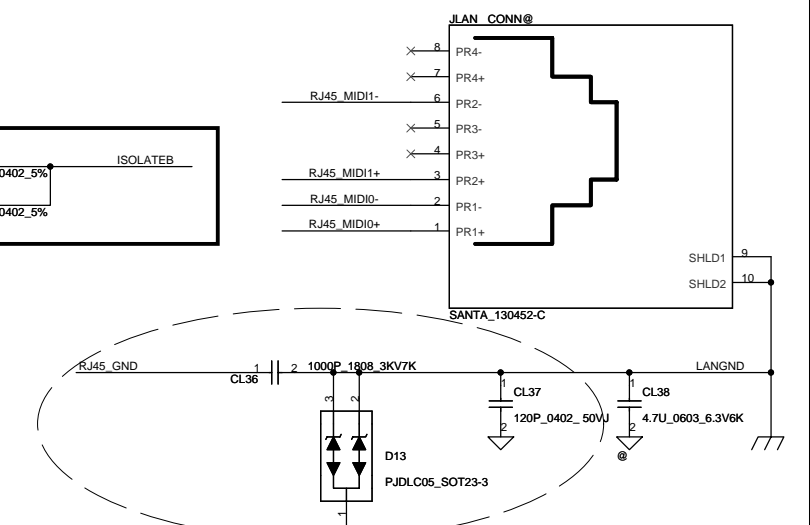
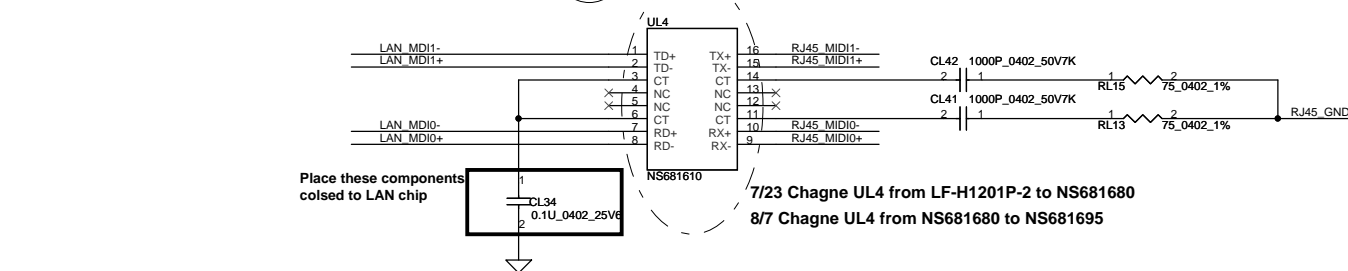
7/16 For LDO mode :
1. Remove RL4, mount RL23.
2. Remove LL1, CL13, CL9, LL3, CL28, CL29.



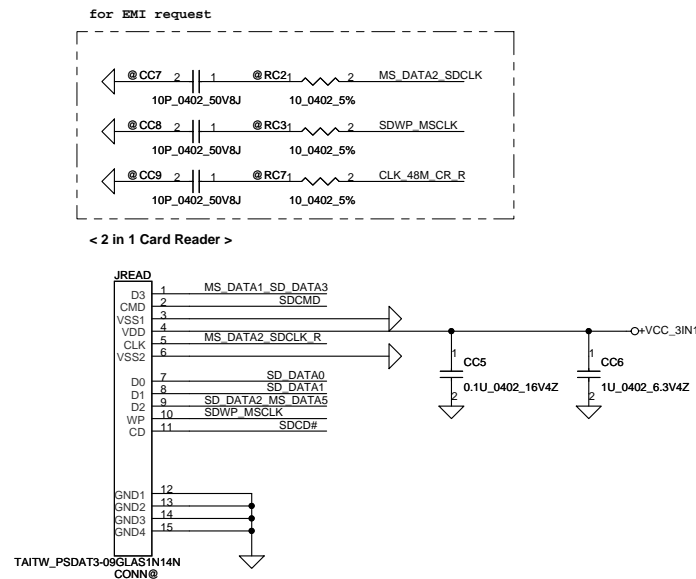
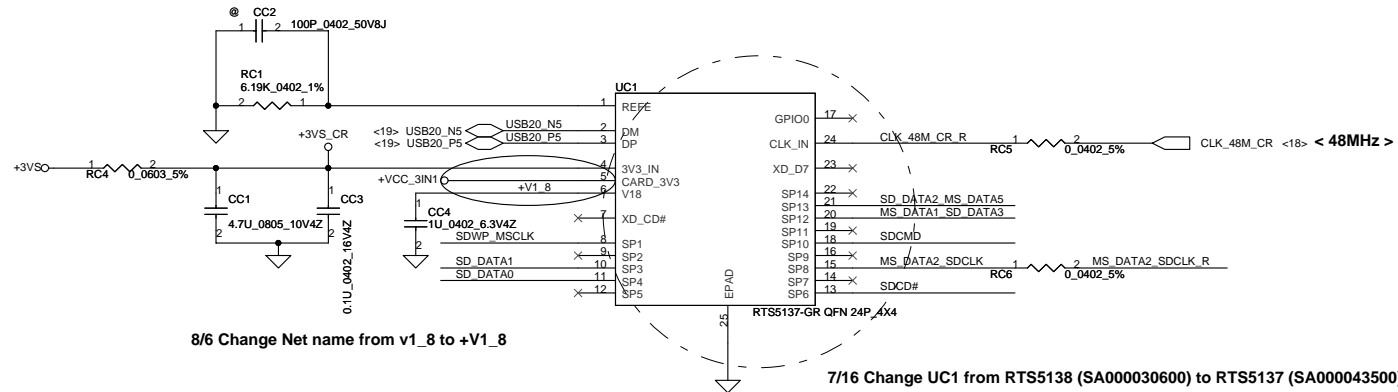
LAN Conn.

change connector to w/o LED
(use NPVAA LAN conn. before LAN symbol ready)

8/7 Chagne UL4 from NS681680 to NS681695

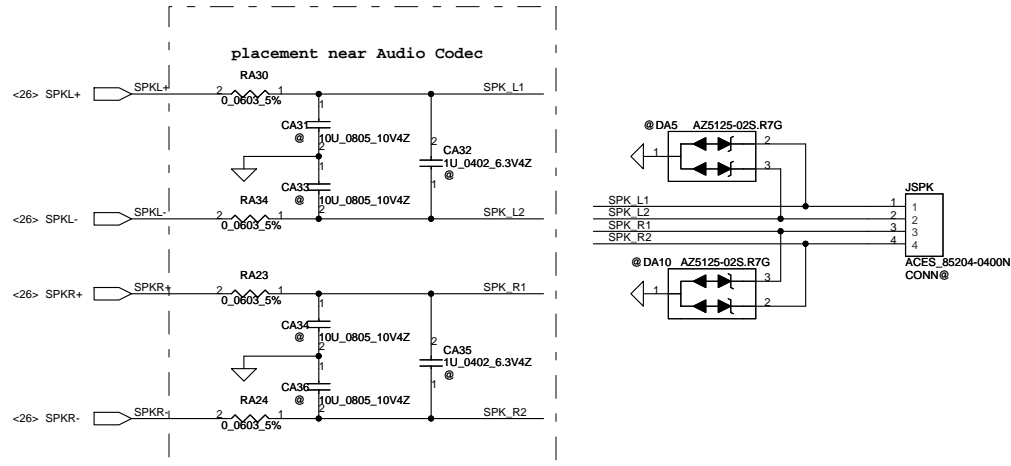


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				Rev	B
				Date	Wednesday, September 01, 2010
				Sheet	24 of 40

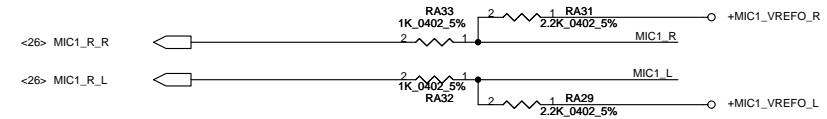


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				401982
				Rev B
				Date: Wednesday, September 01, 2010
				Sheet 25 of 40

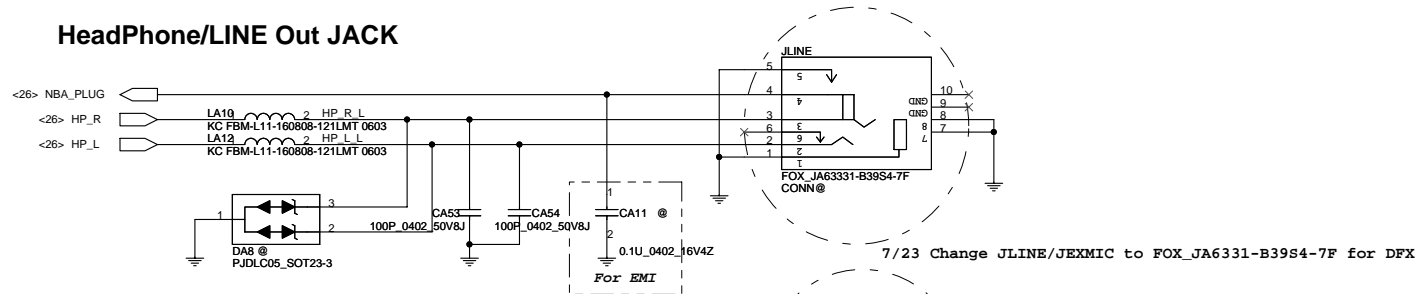
Speaker Connector



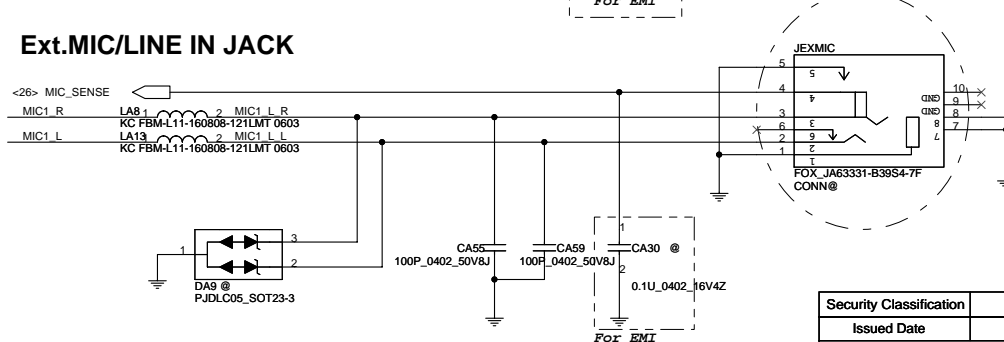
Ext.MIC/LINE IN JACK



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



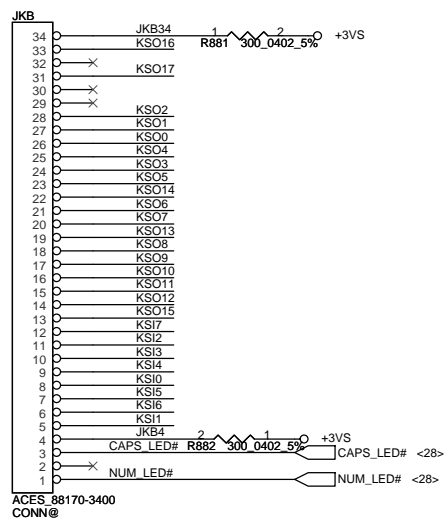
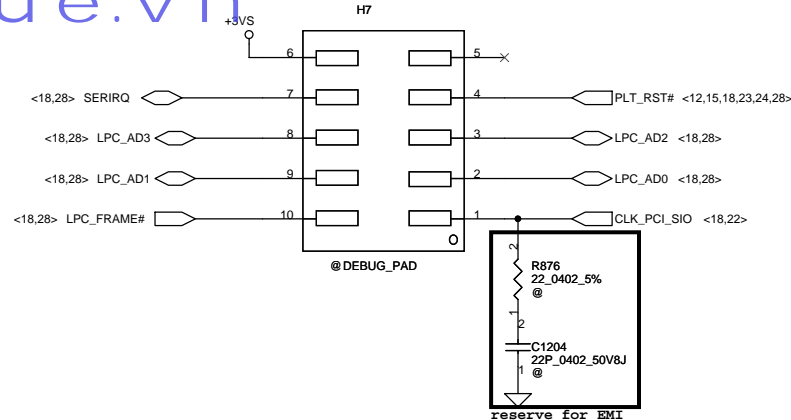
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								401982			
								Date: Wednesday, September 01, 2010			
								Sheet 27 of 40			

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t Please place the PAD under DDR DIMM.

SPI CLK 1 R877 @ 10_0402_5% C1205 1 || 2 @ 10P_0402_50V8J

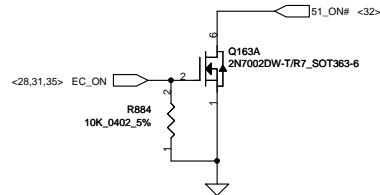
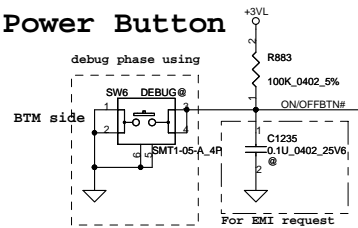
reserve for EMI, close to U13



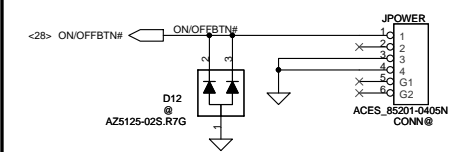
KS016	C1207	100P_0402_50V8J
KS017	C1208	100P_0402_50V8J
KS02	C1209	100P_0402_50V8J
KS01	C1210	100P_0402_50V8J
KS00	C1211	100P_0402_50V8J
KS04	C1212	100P_0402_50V8J
KS03	C1213	100P_0402_50V8J
KS05	C1214	100P_0402_50V8J
KS014	C1215	100P_0402_50V8J
KS06	C1216	100P_0402_50V8J
KS07	C1217	100P_0402_50V8J
KS013	C1218	100P_0402_50V8J
KS08	C1219	100P_0402_50V8J
KS09	C1220	100P_0402_50V8J
KS010	C1221	100P_0402_50V8J
KS011	C1222	100P_0402_50V8J
KS012	C1223	100P_0402_50V8J
KS015	C1224	100P_0402_50V8J
KS17	C1225	100P_0402_50V8J
KS12	C1226	100P_0402_50V8J
KS13	C1227	100P_0402_50V8J
KS14	C1228	100P_0402_50V8J
KS10	C1229	100P_0402_50V8J
KS15	C1230	100P_0402_50V8J
KS16	C1231	100P_0402_50V8J
KS11	C1232	100P_0402_50V8J
CAPS_LED#	C1233	100P_0402_50V8J
NUM_LED#	C1234	100P_0402_50V8J

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					401982
				Date:	Wednesday, September 01, 2010
				Sheet	29 of 40

Power Button

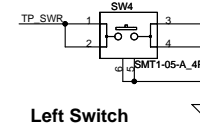


< Power / B Connector >

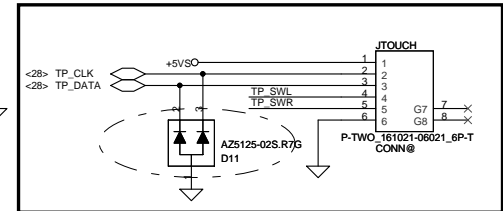
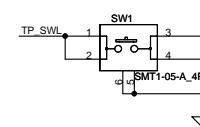


< Touch / B Connector >

Right Switch



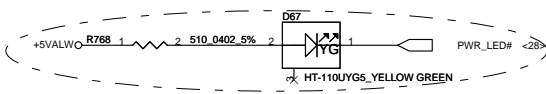
Left Switch



7/13 For ESD request

POWER/SUSPEND LED

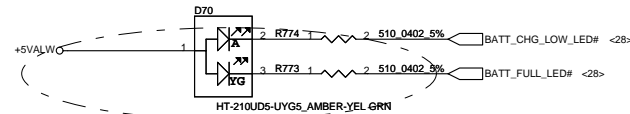
Vf=1.9V(typ), 2.4V(max)
If=20mA(max)



7/6 For Power LED PWM function
7/15 Change D67/D70 to 5mA type
7/23 Change R773 from 120 to 510 ohm
7/23 Change Net name from +3VALW to +5VALW

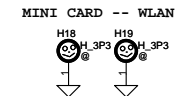
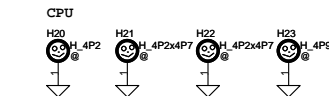
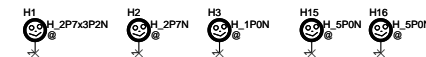
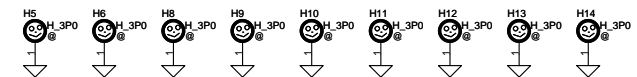
DC IN/ BATT CHARGE

Vf=1.8V(typ), 2.0V(max) for amber
Vf=1.8V(typ), 2.0V(max) for green
If=20mA(max)

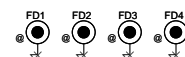


7/23 Change R773 from 120 to 510 ohm
7/23 Change Net name from +3VALW to +5VALW
8/6 Add R774 link to BATT_CHG_LOW_LED#
8/6 Change R773 link to BATT_FULL_LED#

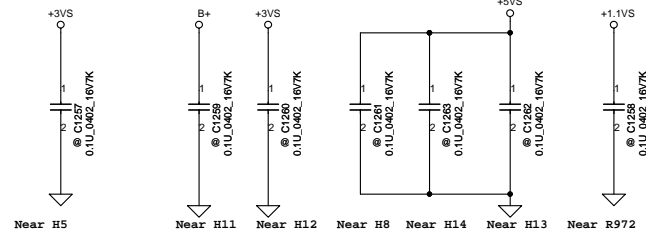
Screw Hole



PCB Fedical Mark PAD



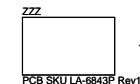
ESD reserved



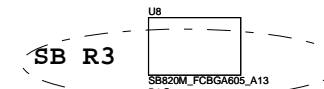
ISPD

7/13 Change P/N to DC30100A400

PCB



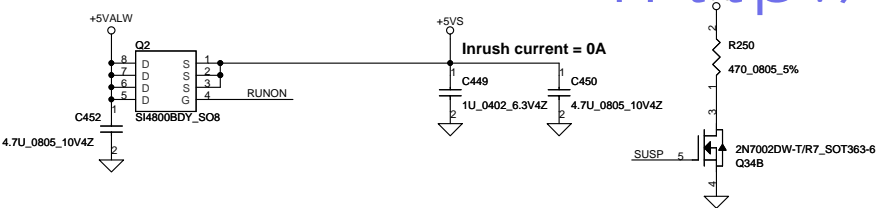
NB R3



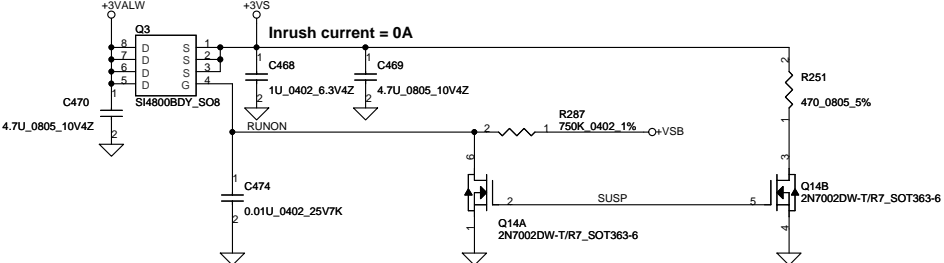
7/21 Change P/N to SA00003IWB0

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Size	Document Number	401982	Rev	B	
Date	Wednesday, September 01, 2010	Sheet	30	of	40

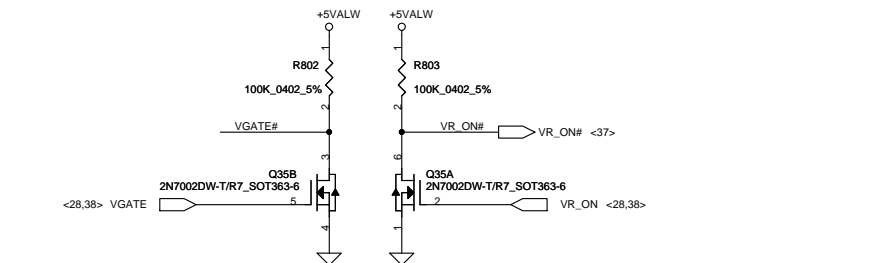
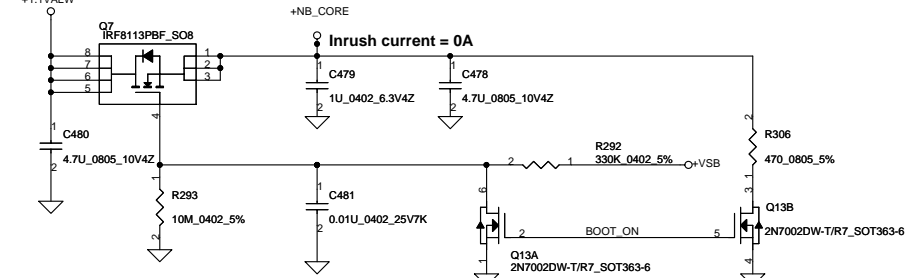
< +5VALW TO +5VS >



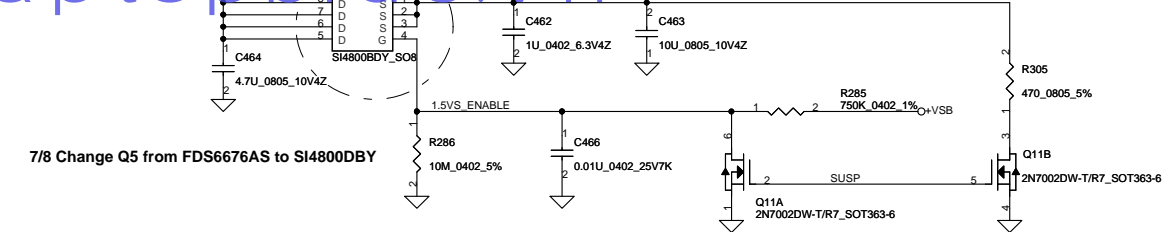
< +3VALW TO +3VS >



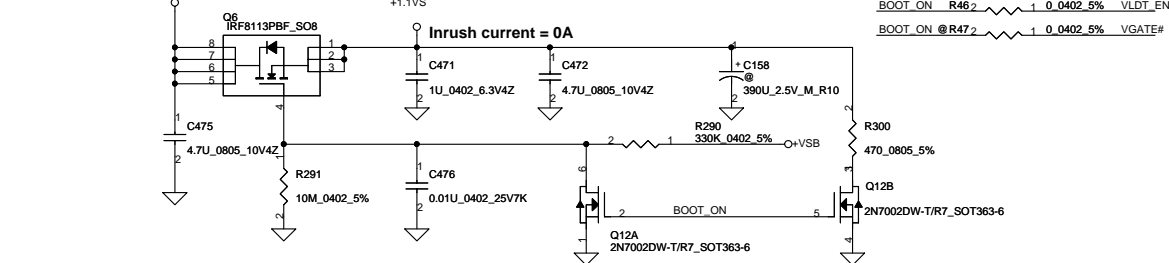
< +1.1VALW TO +NB_CORE >



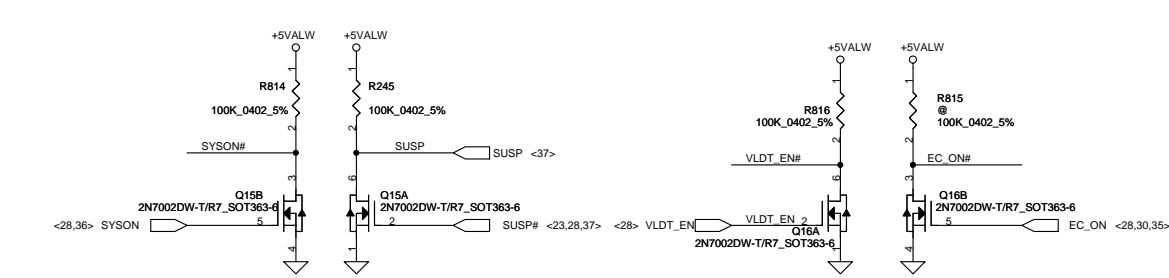
< +1.5V TO +1.5VS >



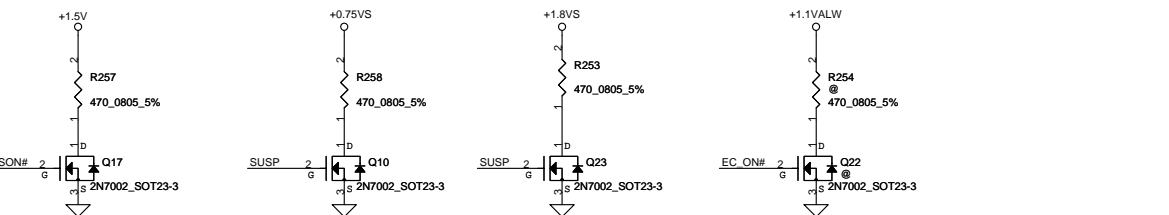
< +1.1VALW TO +1.1VS >



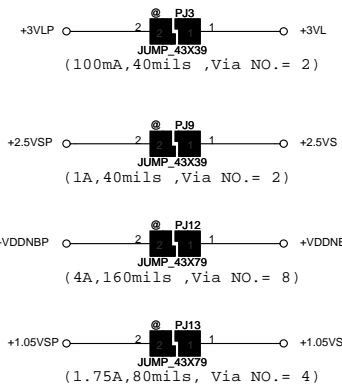
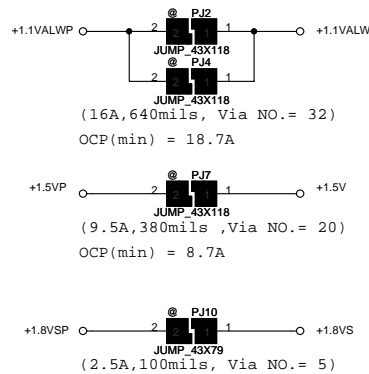
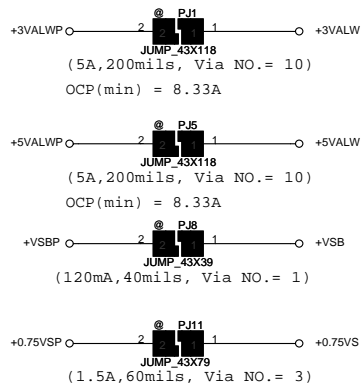
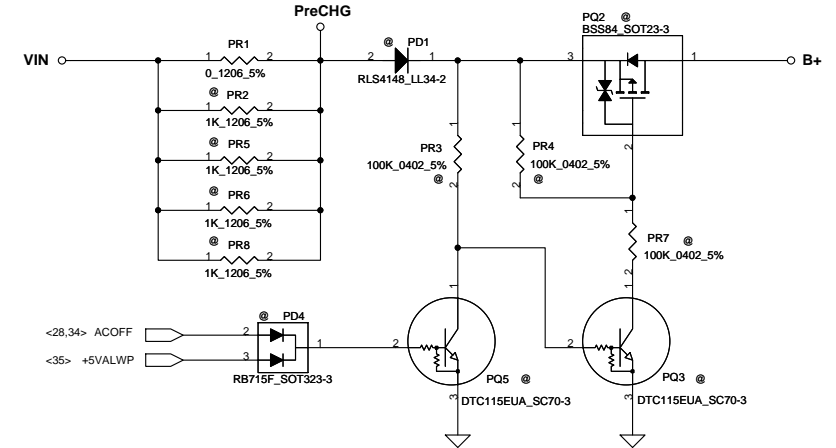
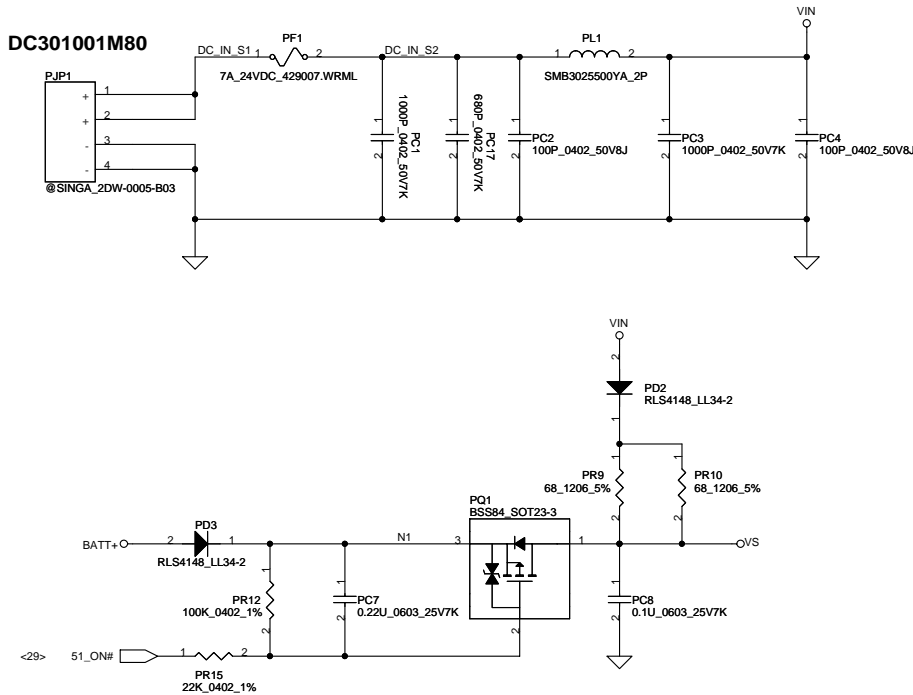
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



< Discharge circuit >



DC301001M80



Precharge detector
15.97V/14.84V FOR
ADAPTOR

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				Date	Wednesday, September 01, 2010
				Sheet	32 of 40
				Rev	B

PH1 under CPU bottom side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

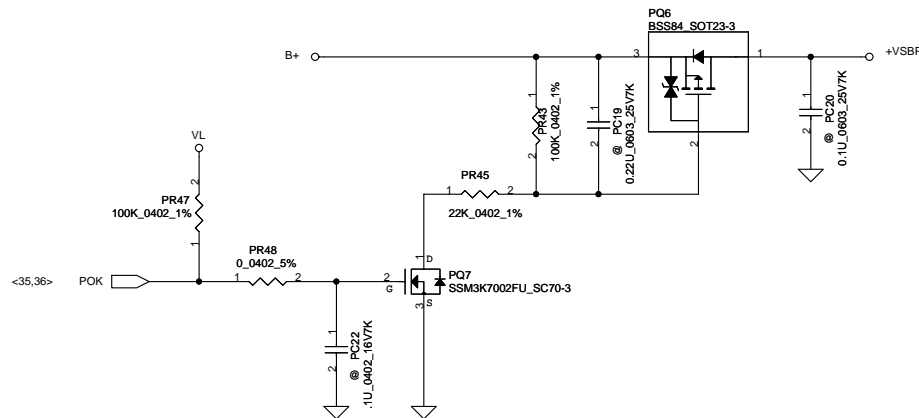
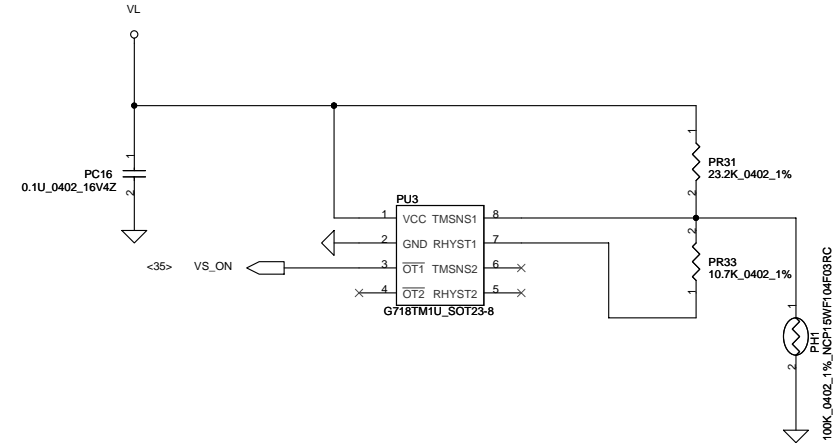
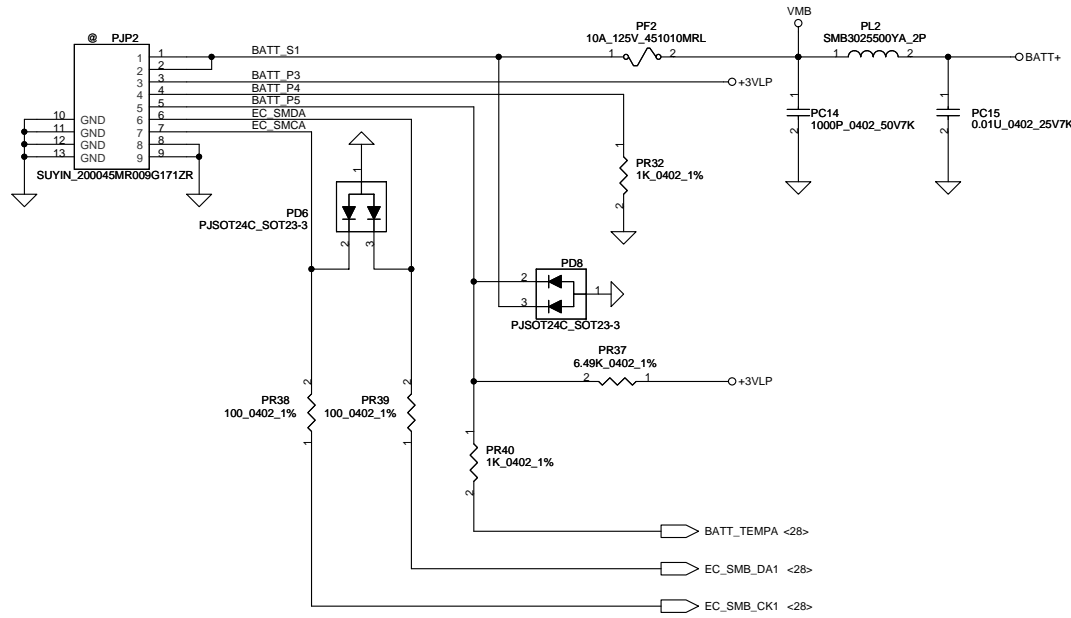
$$R_{set} = 3 * R_{tmh}$$

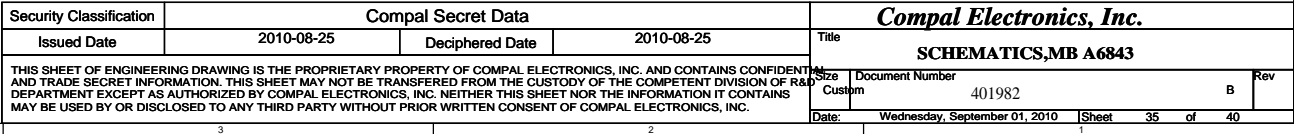
$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

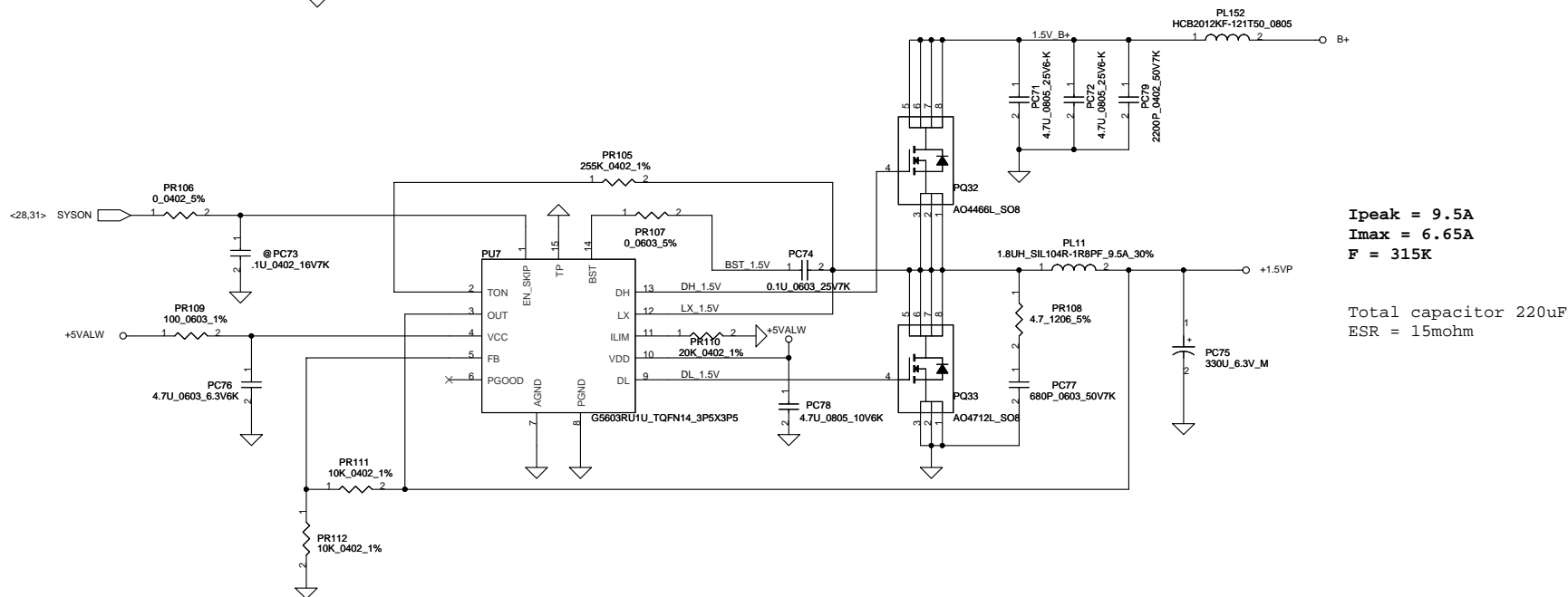
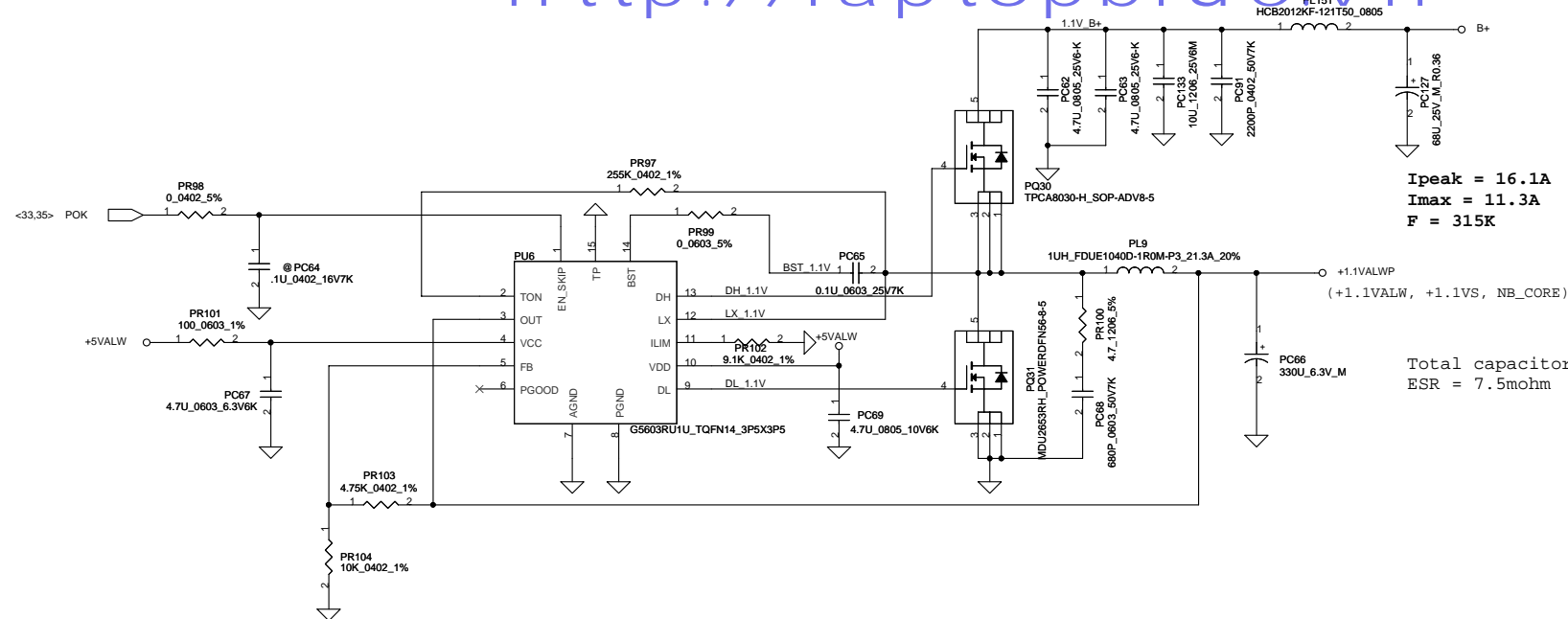
$$R_{tmh} \text{ at } 95C = 6.64K, R_{tml} \text{ at } 57C = 25.1K$$

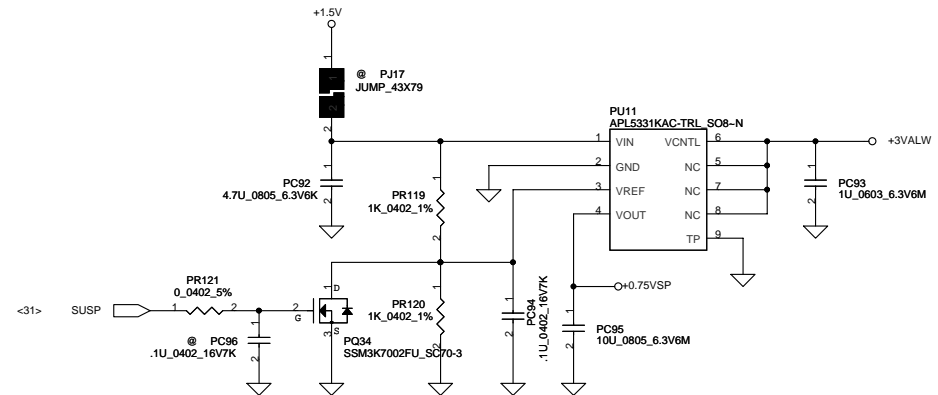
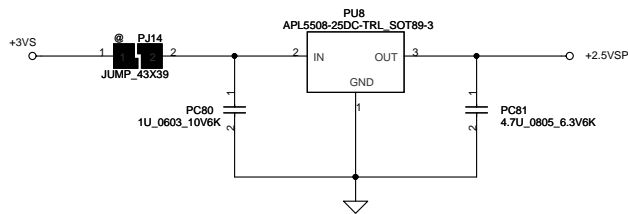
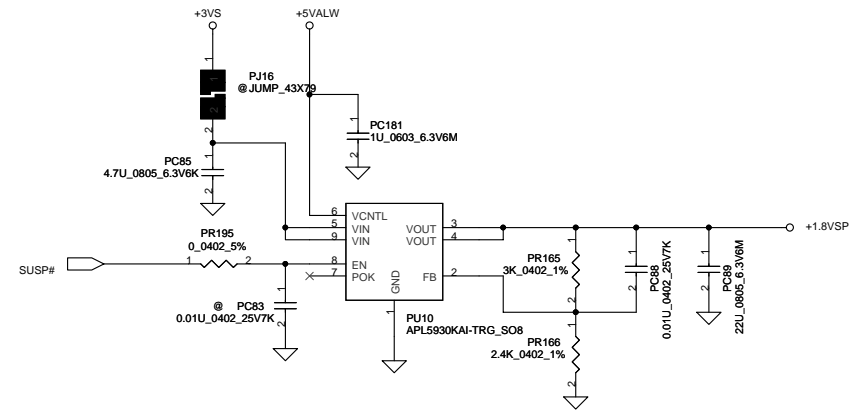
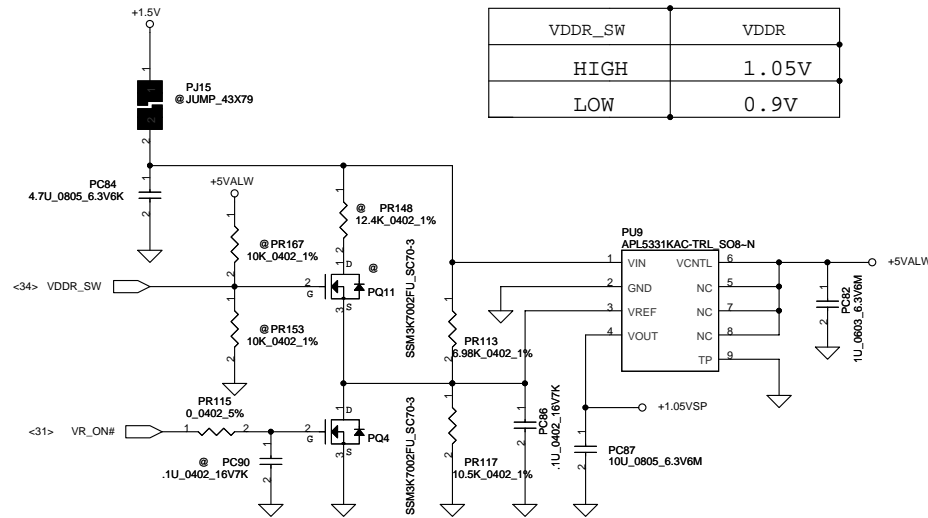
$$R_{set} = 3 * 6.64K = 19.92K \Rightarrow 20K$$

$$R_{hyst} = (20K * 25.1K) / (3 * 25.1K - 20K) = 9.078K \Rightarrow 9.09K$$









PIR (Product Improve Record)

PWWAE LA-6843P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/07/20	28	Reserve CL199,Y5,CL200	For design change
2	2010/07/20	28	Reserve R436 for only KB926E0	For design change
	2010/07/20	29	Del R875	For SERIRQ direct connect to H7.7
	2010/07/20	29	Del C588/C589/Y4/R368	For design change
3	2010/07/21	11-15	Change U8 R1 P/N from A12(SA000032WI40) to A13(SA000032WA0)	For SB820 A13 version
	2010/07/21	30	Change U8 R3 P/N from A12(SA000032WI50) to A13(SA000032WB0)	For SB820 A13 version
4	2010/07/23	18	Change D8 from DAN202U to CHN202UPT	For design change
5	2010/07/23	24	Chagne U4 from LF-H1201P-2 to LFE8456E-R for use 5mA type	For design change
6	2010/07/23	30	Change R768/R773 from 120 to 510 ohm for use 5mA type	For design change
			Change R768.1 pull up from +3VALW to +5VALW for use 5mA type	For design change
			Change R773.1 pull up from +3VALW to +5VALW for use 5mA type	For design change
7	2010/07/23	27	Change JLINE/JEXMIC to FOX_JA6331-B39S4-7F	For DFX request
8	2010/07/26	23	Reserve DM2	For +3V_WLAN is +3VS
9	2010/07/26		Add R50	For Intel Rainbow Peak module
	2010/07/26	24	Reserve CL39	For EMI request
10	2010/07/27	28	Change R867 pull up from +3VALW to +3VL	For design change

REVISION CHANGE: 0.2 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/08/06	29	Change U13 footprint to M25P10-AVNM6T-SOP	For design change
2	2010/08/06	25	Change Net name form V1_8 to +V1_8	For customer request
	2010/08/06	29	Add R774 link to BATT_CH0_LOW_LED#	For customer request
	2010/08/06	29	Change R773 link to BATT_FULL_LED#	For customer request
3	2010/08/06	30	Reserve SW6 Del SWS	For debug phase
	2010/08/09	30	Chagne U4 from NS681680 to NS681610	For design change
4	2010/08/09	08	Mount C26/C89,Reserve C24,C90	For design change
5	2010/08/16	18	Del R42/C94	For EMI request
	2010/08/16	18	Reserve CC9/RC7	For EMI request
6	2010/08/16	24	Add CL3/CL7 link to +3V_LAN	For EMI request
			Reserve CL38	For EMI request
			Change CL37 from 0.1uF to 120 pF	For EMI request
			Add D13 link to LANGND	For EMI request

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				401982	B
Date: Wednesday, September 01, 2010				Sheet	39 of 40

Version Change List (P. I. R. List) for Power Circuit

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	Rev.
2010 . 06 . 21 Release					
2010 . 07.25 modification list					
	P 33		PC16 change to SE070104Z80	Defore material EOL	PVT
	P 38		PU12 change to SA000022M80	Before material MP schedule will impact PWWAE MP schedule	PVT
	P 33		Remove PD6 , PD8 @	ESD test fail	PVT
	P 34		Add PC132 , remove PC130 , PC131 , PR69 , PC41 @	For EMI fail	PVT
	P 35		Add PC51 , remove PC49 , PC46 , PC57 , PC58 , PR89 , PR90 @	For EMI fail	PVT
	P 36		Add PC79 , PC91 , PC133 , remove PR100 , PR108 , PC68 , PC77 @	For EMI fail	PVT
	P 38		Remove PR125 , PR139 , PR151 , PC106 , PC111 , PC117 @	For EMI fail	PVT
2010 . 08.10 modification list					
	P 37		Change PU9 , PU11 to SA053310110	UP7711 stop using from now on	Pre-MP
	P 38		Add PC218 , PC219 , PC371	For VCORE Ripple	Pre-MP
	P 32		Add PR8	For Precharge rising current	Pre-MP
	P 32 , P 33		PQ1 , PQ2 , PQ6 change to SB900840003	SB906100210 material delivery had problem	Pre-MP
2010 . 08.16 modification list					
	P 35		Change PU5 to SA000020C80	UPI product stop using	Pre-MP
2010 . 08.17 modification list					
	P 34		Change PU4 to SA00001EP80	SA00003TK00 stop using	Pre-MP
	P 38		Remove PR127 @	To solve +1.1VALW noise	Pre-MP
2010 . 08.23 modification list					
	P 34		Remove PR193 , PQ39 @	For PWWAE MP use 25W CPU	Pre-MP