PWWAA

Delhi

LA-6847P REV 1.0 Schematic

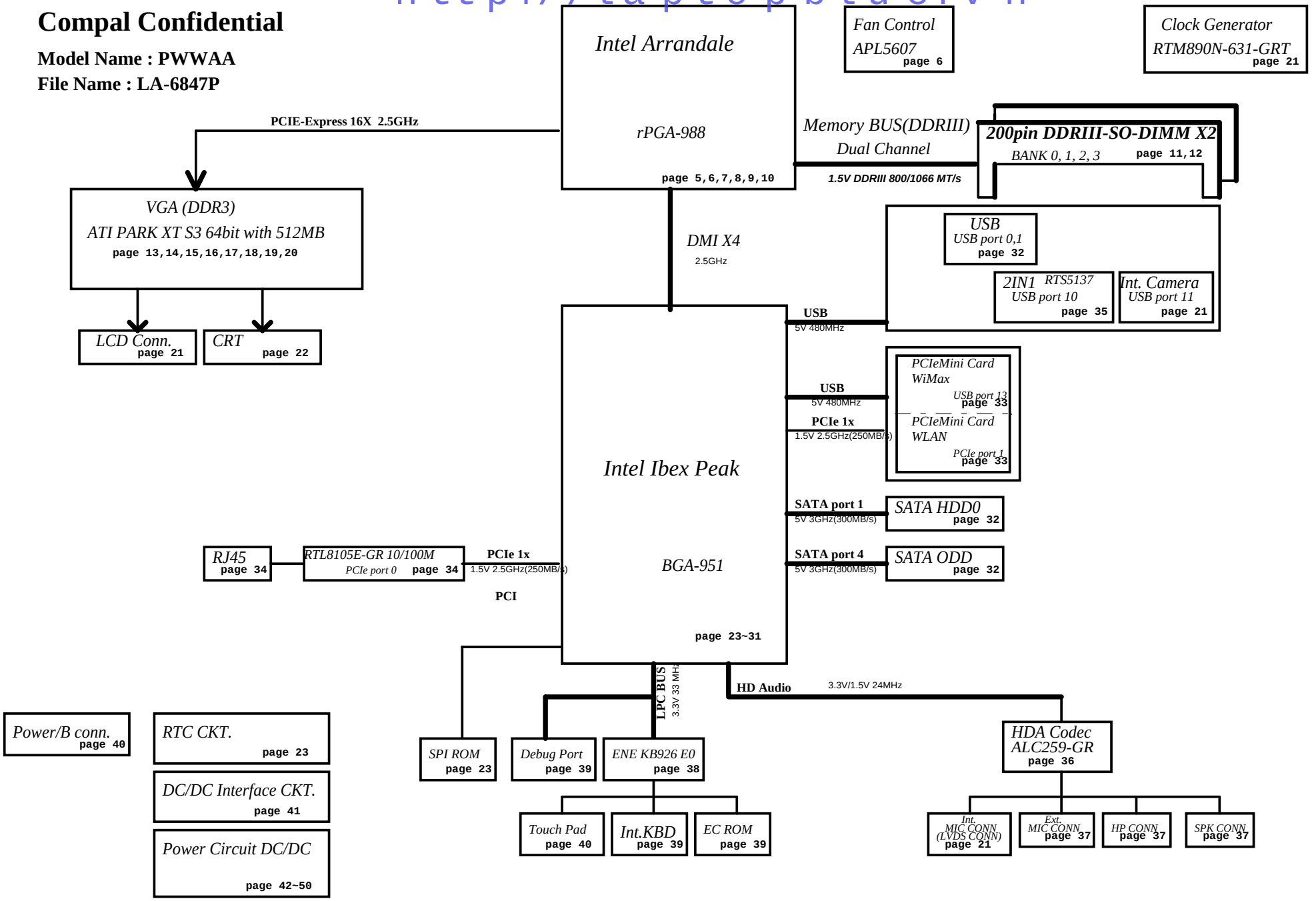
Intel Processor(ARD) /PCH(HM55)
2010-10-07 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/09/05	Deciphered Date	2011/09/05

Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6847		
Size: B	Document Number: 4019AP	Rev: B
Date: Tuesday, December 28, 2010	Sheet 1 of 52	

Compal Confidential

Model Name : PWWAA
File Name : LA-6847P



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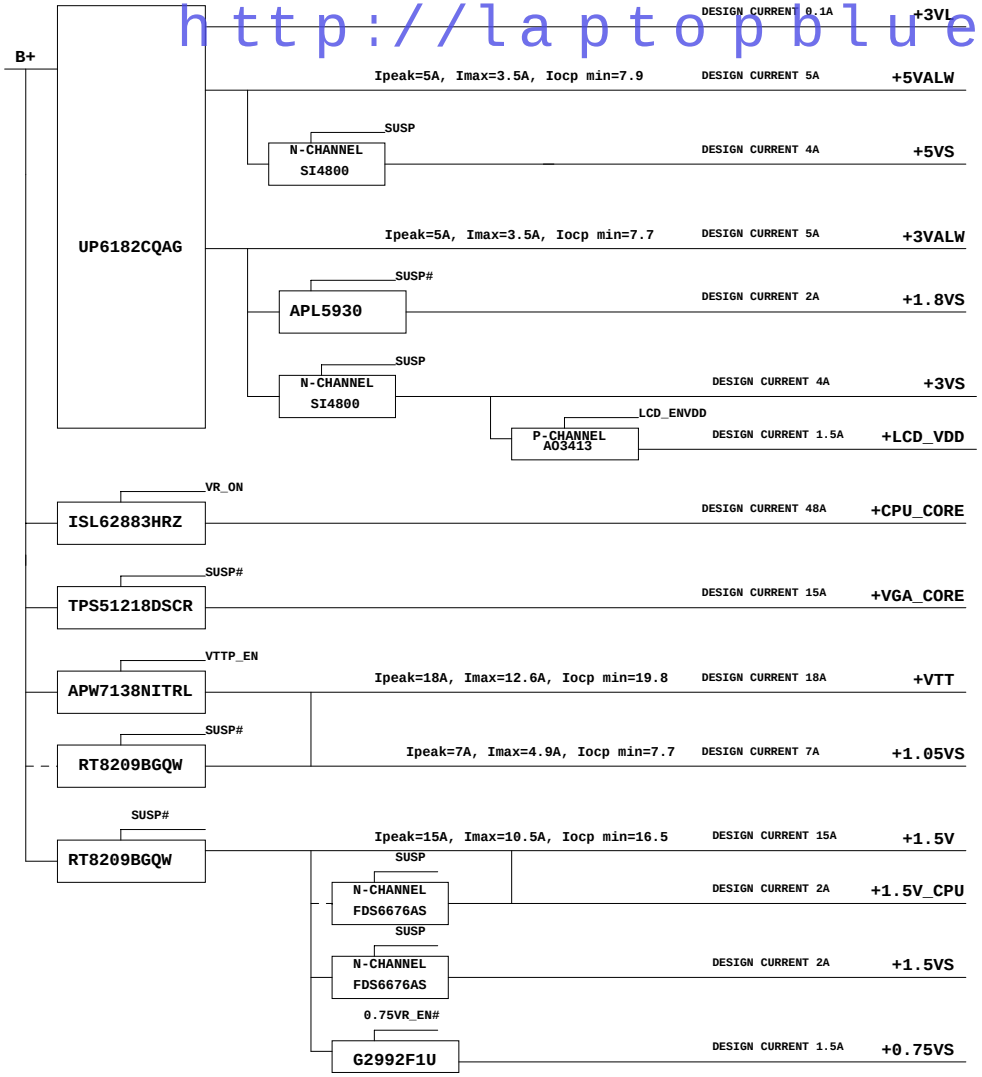

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	MINI PCI-E SLOT			LAN					
description			SLOT1	LAN					
explain			WLAN/BT	10/100M					
BTO									

Function				Camera & Mic			
description				Camera & Mic			
explain				Camera & Mic			
BTO				CAM@			

Function	S3 Power Saving		
description	S3 Power Saving		
explain		Power Saving	
BTO			

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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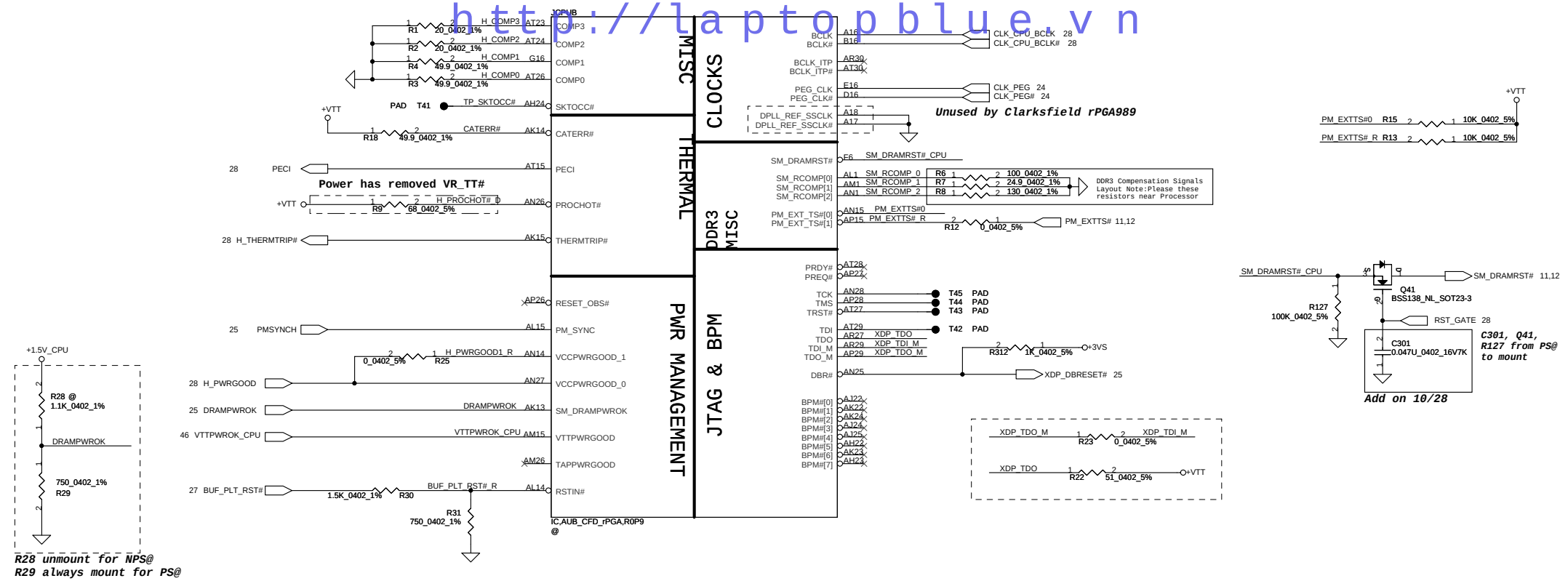
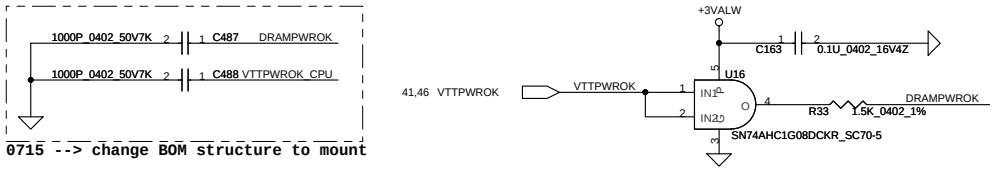


For S3 CPU Power Saving

place near JCPU



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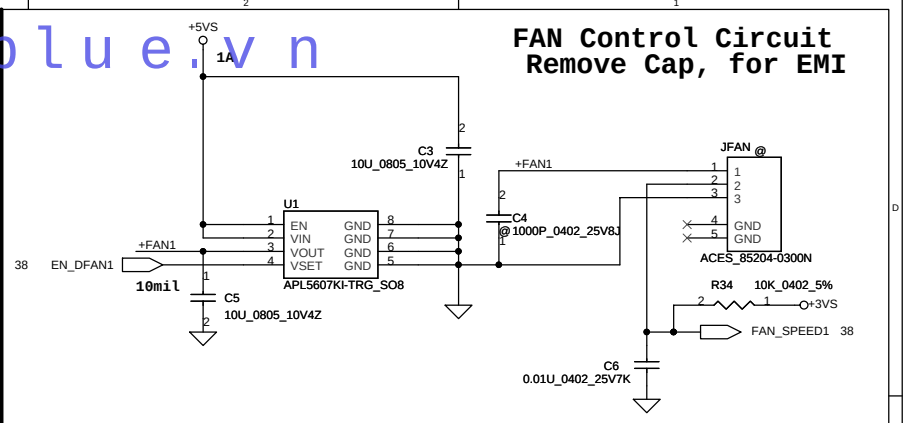

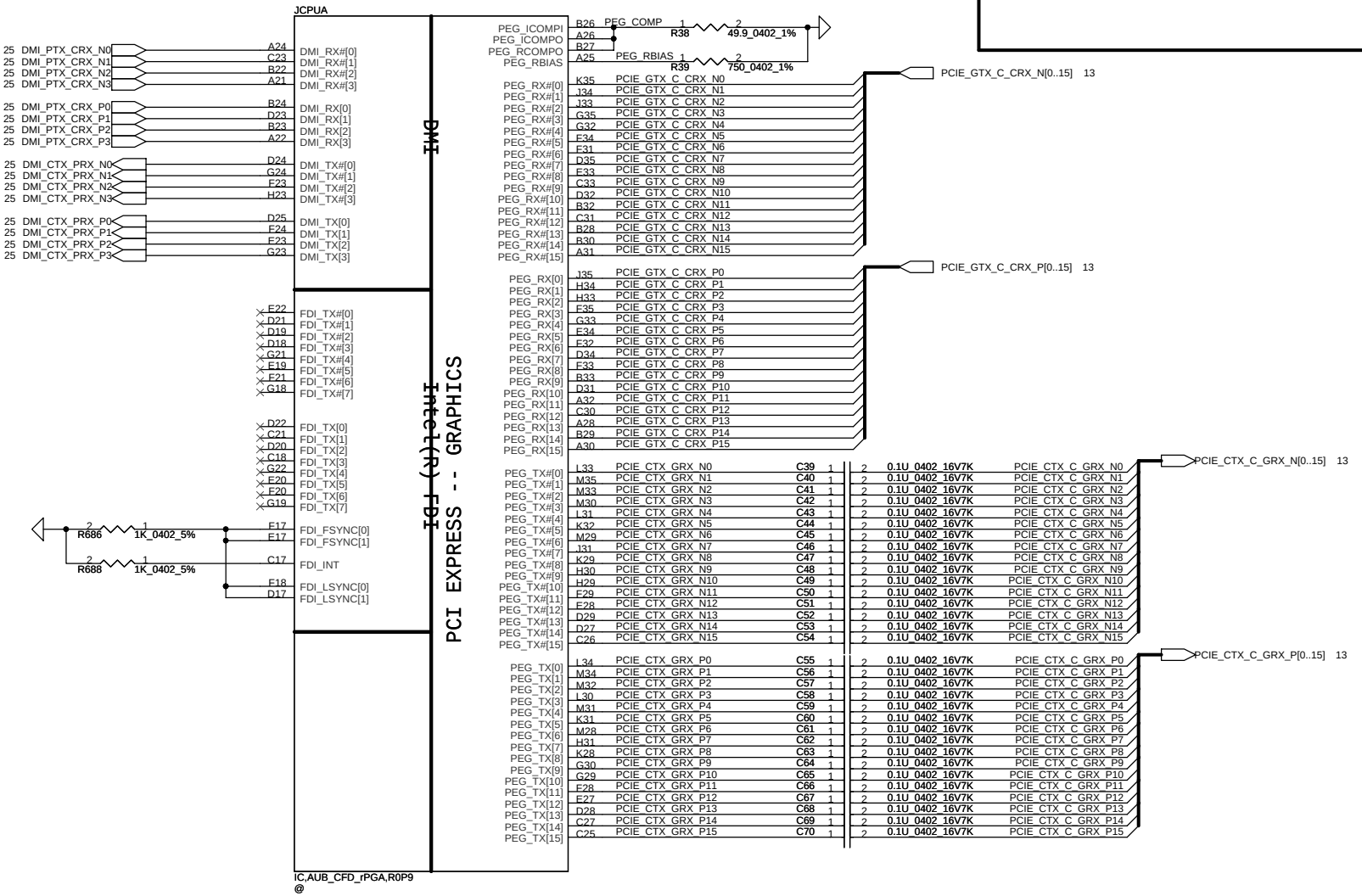

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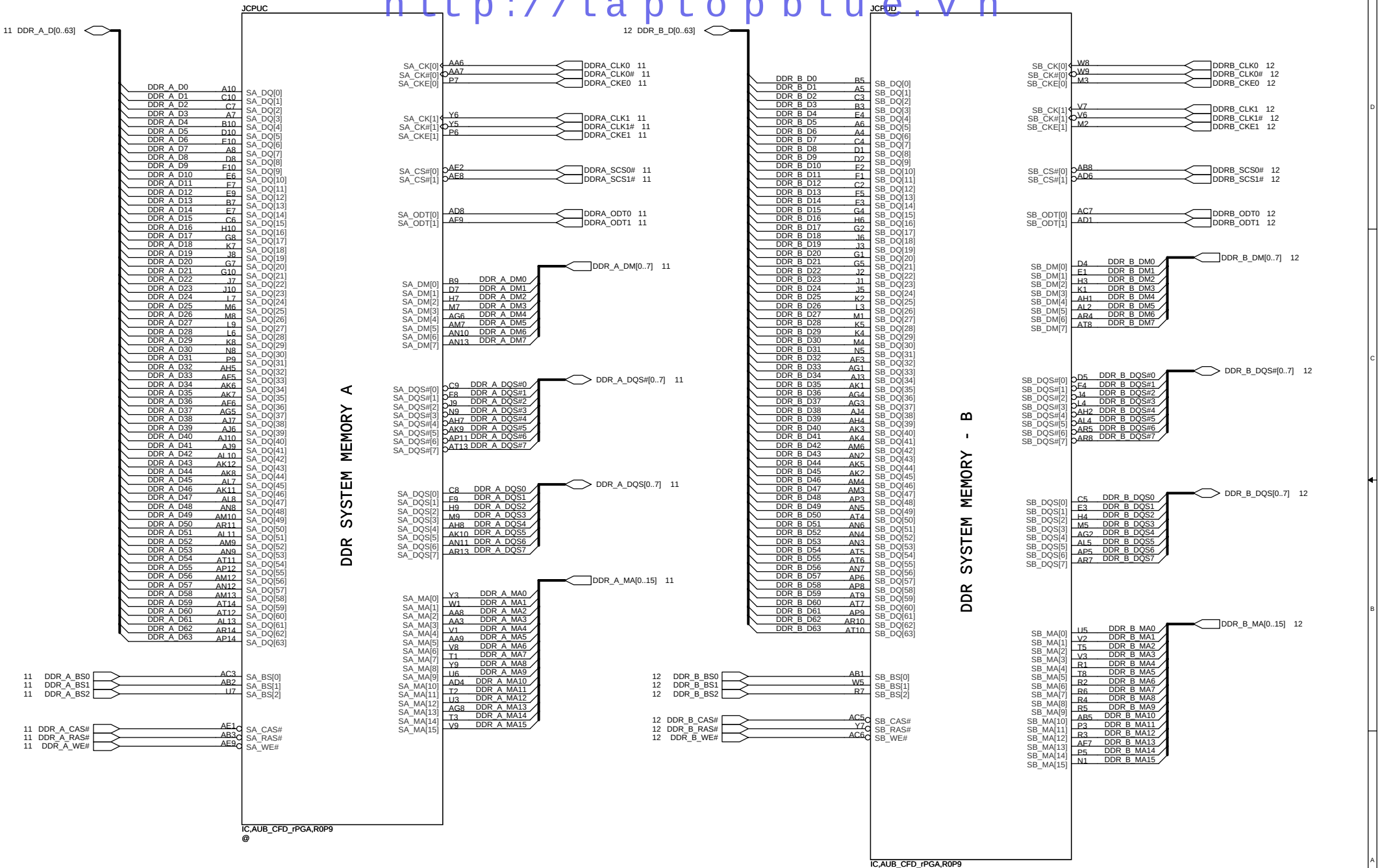

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Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

JCPUF

+CPU_CORE

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

(Place these capacitors under CPU socket Edge, top layer)

+VTT

C144 390U_2.5V_M_R10
C267 390U_2.5V_M_R10
C89 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 C83 C85 C87 C88 C90 C92 10U_0805_10V4K
C94 10U_0805_10V4K@

SF000002O00
ESR 10m-ohm
H6.3

Power team request for F-Din

+CPU_CORE
22U_0805_6.3V6M
C114 C179 C131 C116 C132 C129 C149

PSI# AN33 H_PSI# 49

VID[0] AK35 CPU_VID0 49
VID[1] AK33 CPU_VID1 49
VID[2] AK34 CPU_VID2 49
VID[3] AL35 CPU_VID3 49
VID[4] AL33 CPU_VID4 49
VID[5] AM33 CPU_VID5 49
VID[6] AM35 CPU_VID6 49

PROC_DPRSLPVR AM34 H_DPRSLPVR_R R62 0_0402_5% H_DPRSLPVR 49

VTT_SELECT G15

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

ISENSE AN35 IMVP_IMON 49

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5%

R64 100_0402_1% +CPU_CORE
VCCSENSE
VSSSENSE
VCCSENSE 49
VSSSENSE 49
R67 100_0402_1%
near CPU

VTT_SENSE B15 VTT_SENSE 46
VSS_SENSE_VTT A15 VSS_SENSE_VTT 46

IC,AUB_CFD_rPGA,R0P9
@

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE
10U_0805_10V4K
C71 C72 C73 C74 C75 C76 C77 C78 C79

(Place these capacitors under CPU socket, top layer)

+CPU_CORE
10U_0805_10V4K
C98 C99 C100 C101 C102 C103 C104

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE
22U_0805_6.3V6M
C105 C106 C107 C108 C109 C110
C111 C112 C113 C130 C115 C148

TOP side (under inductor)

+CPU_CORE
330U_D2_2.5VM_R9M
C121 C122 C123 C124

Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF

+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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+1.5V_CPU +1.5VS
PJ32 @
JUMP_43X79

7/22 modified for cost down.

3A
form PS@ to mount
+1.5V_CPU
R424 470_0805_5%
C273 10U_0805_10V4K
Q33 FDS6676AS_SO8
+1.5V
R418 220K_0402_5%
+VSB
Q46B 2N7002DW-T/R7_SOT363-6
SUSP
C472 0.1U_0402_25V6
R417 820K_0402_5%
Q46A 2N7002DW-T/R7_SOT363-6
SUSP
SUSP 41,48

JCPUG

R258 0_0402_5%

VAXG1 AT21
VAXG2 AT19
VAXG3 AT18
VAXG4 AT16
VAXG5 AR21
VAXG6 AR19
VAXG7 AR18
VAXG8 AR16
VAXG9 AP21
VAXG10 AP19
VAXG11 AP18
VAXG12 AP16
VAXG13 AN21
VAXG14 AN19
VAXG15 AN18
VAXG16 AN16
VAXG17 AM21
VAXG18 AM19
VAXG19 AM18
VAXG20 AM16
VAXG21 AL21
VAXG22 AL19
VAXG23 AL18
VAXG24 AL16
VAXG25 AK21
VAXG26 AK19
VAXG27 AK18
VAXG28 AK16
VAXG29 AJ21
VAXG30 AJ19
VAXG31 AJ18
VAXG32 AJ16
VAXG33 AH21
VAXG34 AH19
VAXG35 AH18
VAXG36 AH16

Auburndale:22A

GRAPHICS

SENSE LINES
VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDS
GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

GFXVR_IMON R687 1K_0402_5%

C230 0.1U_0402_16V4Z
C314 0.1U_0402_16V4Z
C205 0.1U_0402_16V4Z
C186 0.1U_0402_16V4Z

remove PJ30

PJ31 @
JUMP_43X79
+1.5V

PJ31 need to open for S3 CPU Power Saving

POWER

DDR3 - 1.5V RAILS

VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

Clarksfield: 5A
Auburndale:3A

+1.5V_CPU
1U_0402_6.3V4Z 1U_0402_6.3V4Z 22U_0805_6.3V6M
C133 C134 C135 C136 C137 C138 C139
C216 390U_2.5V_M_R10
1U_0402_6.3V4Z 1U_0402_6.3V4Z 1U_0402_6.3V4Z 22U_0805_6.3V6M

FDI

VTT1_45 J24
VTT1_46 J23
VTT1_47 H25

+VTT
C141 22U_0805_6.3V6M
C142 22U_0805_6.3V6M

1.1V

VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

Clarksfield: 21A
Auburndale:18A

+VTT
C143 10U_0805_10V4K
(Place these capacitors under CPU socket Edge, top layer)

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

+VTT
C145 22U_0805_6.3V6M
(Place these capacitors under CPU socket, top layer)

PEG & DMI

VTT1_48 K26
VTT1_49 J27
VTT1_50 J26
VTT1_51 J25
VTT1_52 H27
VTT1_53 G28
VTT1_54 G27
VTT1_55 G26
VTT1_56 F26
VTT1_57 F26
VTT1_58 E25

+VTT
C146 22U_0805_6.3V6M
C147 22U_0805_6.3V6M
(Place these capacitors under CPU socket, top layer)

1.8V

VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26

+1.8VS_H_PLL 1U_0402_6.3V4Z 4.7U_0603_6.3V6K
+1.8VS
R71 0_0805_5%
C151 1U_0402_6.3V4Z
C152 C153 C154 C155 22U_0805_6.3V6M
2.2U_0603_6.3V4Z

Clarksfield: 0.6A
Auburndale:1.35A

IC,AUB_CFD_rPGA,R0P9
@

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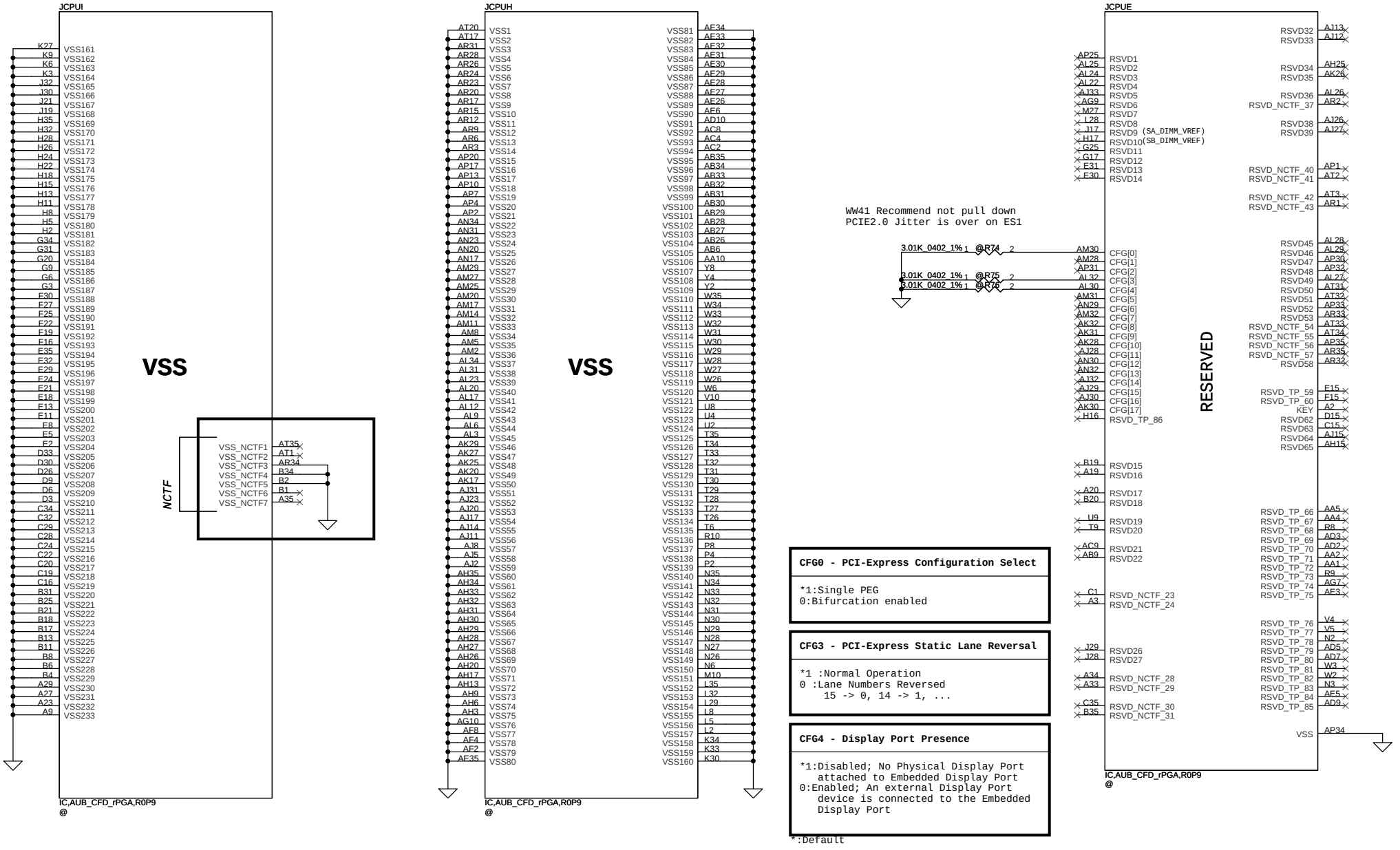

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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DDR3 SO-DIMM A
Standard Type

JDDRL

+VREF_DQA

+1.5V

C156 0.1U_0402_16V4Z
C157 2.2U_0603_6.3V4Z

close to JDDRL.1

		1	VREF_DQ	VSS	2	
DDR_A_D0		3	VSS	DQ4	4	DDR_A_D4
DDR_A_D1		5	DQ0	DQ5	6	DDR_A_D5
		7	DQ1	VSS	8	
DDR_A_DM0		9	VSS	DQS0#	10	DDR_A_DQS#0
		11	DM0	DQS0	12	DDR_A_DQS0
DDR_A_D2		13	VSS	VSS	14	
DDR_A_D3		15	DQ2	DQ6	16	DDR_A_D6
		17	DQ3	DQ7	18	DDR_A_D7
DDR_A_D8		19	VSS	VSS	20	
DDR_A_D9		21	DQ8	DQ12	22	DDR_A_D12
		23	DQ9	DQ13	24	DDR_A_D13
DDR_A_DQS#1		25	VSS	VSS	26	
DDR_A_DQS1		27	DQS1#	DM1	28	DDR_A_DM1
		29	DQS1	RESET#	30	
DDR_A_D10		31	VSS	VSS	32	
DDR_A_D11		33	DQ10	DQ14	34	DDR_A_D14
		35	DQ11	DQ15	36	DDR_A_D15
DDR_A_D16		37	VSS	VSS	38	
DDR_A_D17		39	DQ16	DQ20	40	DDR_A_D20
		41	DQ17	DQ21	42	DDR_A_D21
DDR_A_DQS#2		43	VSS	VSS	44	
DDR_A_DQS2		45	DQS2#	DM2	46	DDR_A_DM2
		47	DQS2	VSS	48	
DDR_A_D18		49	VSS	DQ22	50	DDR_A_D22
DDR_A_D19		51	DQ18	DQ23	52	DDR_A_D23
		53	DQ19	VSS	54	
DDR_A_D24		55	VSS	DQ28	56	DDR_A_D28
DDR_A_D25		57	DQ24	DQ29	58	DDR_A_D29
		59	DQ25	VSS	60	
DDR_A_DM3		61	VSS	DQS3#	62	DDR_A_DQS#3
		63	DM3	DQS3	64	DDR_A_DQS3
DDR_A_D26		65	VSS	VSS	66	
DDR_A_D27		67	DQ26	DQ30	68	DDR_A_D30
		69	DQ27	DQ31	70	DDR_A_D31
		71	VSS	VSS	72	
7 DDRA_CKE0		73	CKE0	CKE1	74	DDRA_CKE1 7
		75	VDD	VDD	76	
7 DDR_A_BS2		77	NC	A15	78	DDR_A_MA15
		79	BA2	A14	80	DDR_A_MA14
DDR_A_MA12		81	VDD	VDD	82	
DDR_A_MA9		83	A12/BC#	A11	84	DDR_A_MA11
		85	A9	A7	86	DDR_A_MA7
DDR_A_MA8		87	VDD	VDD	88	
DDR_A_MA5		89	A8	A6	90	DDR_A_MA6
		91	A5	A4	92	DDR_A_MA4
DDR_A_MA3		93	VDD	VDD	94	
DDR_A_MA1		95	A3	A2	96	DDR_A_MA2
		97	A1	A0	98	DDR_A_MA0
		99	VDD	VDD	100	
7 DDRA_CLK0		101	CK0	CK1	102	DDRA_CLK1 7
7 DDRA_CLK0#		103	CK0#	CK1#	104	DDRA_CLK1# 7
		105	VDD	VDD	106	
DDR_A_MA10		107	A10/AP	BA1	108	DDR_A_BS1 7
7 DDR_A_BS0		109	BA0	RAS#	110	DDR_A_RAS# 7
		111	VDD	VDD	112	
7 DDR_A_WE#		113	WE#	S0#	114	DDRA_SCS0# 7
7 DDR_A_CAS#		115	CAS#	ODT0	116	DDRA_ODT0 7
		117	VDD	VDD	118	
DDR_A_MA13		119	A13	ODT1	120	DDRA_ODT1 7
7 DDRA_SCS1#		121	S1#	NC	122	
		123	VDD	VDD	124	
		125	TEST	VREF_CA	126	+DDR_VREF_CA_DIMMA
		127	VSS	VSS	128	
DDR_A_D32		129	DQ32	DQ36	130	DDR_A_D36
DDR_A_D33		131	DQ33	DQ37	132	DDR_A_D37
		133	VSS	VSS	134	
DDR_A_DQS#4		135	DQS4#	DM4	136	DDR_A_DM4
DDR_A_DQS4		137	DQS4	VSS	138	
		139	VSS	DQ38	140	DDR_A_D38
DDR_A_D34		141	DQ34	DQ39	142	DDR_A_D39
DDR_A_D35		143	DQ35	VSS	144	
		145	VSS	DQ44	146	DDR_A_D44
DDR_A_D40		147	DQ40	DQ45	148	DDR_A_D45
DDR_A_D41		149	DQ41	VSS	150	
		151	VSS	DQS5#	152	DDR_A_DQS#5
DDR_A_DM5		153	DM5	DQS5	154	DDR_A_DQS5
		155	VSS	VSS	156	
DDR_A_D42		157	DQ42	DQ46	158	DDR_A_D46
DDR_A_D43		159	DQ43	DQ47	160	DDR_A_D47
		161	VSS	VSS	162	
DDR_A_D48		163	DQ48	DQ52	164	DDR_A_D52
DDR_A_D49		165	DQ49	DQ53	166	DDR_A_D53
		167	VSS	VSS	168	
DDR_A_DQS#6		169	DQS6#	DM6	170	DDR_A_DM6
DDR_A_DQS6		171	DQS6	VSS	172	
		173	VSS	DQ54	174	DDR_A_D54
DDR_A_D50		175	DQ50	DQ55	176	DDR_A_D55
DDR_A_D51		177	DQ51	VSS	178	
		179	VSS	DQ60	180	DDR_A_D60
DDR_A_D56		181	DQ56	DQ61	182	DDR_A_D61
DDR_A_D57		183	DQ57	VSS	184	
		185	VSS	DQS7#	186	DDR_A_DQS#7
DDR_A_DM7		187	DM7	DQS7	188	DDR_A_DQS7
		189	VSS	VSS	190	
DDR_A_D58		191	DQ58	DQ62	192	DDR_A_D62
DDR_A_D59		193	DQ59	DQ63	194	DDR_A_D63
		195	VSS	VSS	196	
		197	SA0	EVENT#	198	PM_EXTTS# 5,12
		199	VDDSPD	SDA	200	PM_SMBDATA 12,21,24,33
		201	SA1	SCL	202	PM_SMBCLK 12,21,24,33
		203	VTT	VTT	204	+0.75VS
		205	GND1	BOSS1	206	
		207	GND2	BOSS2	208	

FOX_AS0A626-U2SN-7F_204P
@

R83 1K_0402_1%
R83 from PS@ to mount
SM_DRAMRST# 5,12

7 DDR_A_DQS[0..7]
7 DDR_A_DQS#[0..7]
7 DDR_A_D[0..63]
7 DDR_A_DM[0..7]
7 DDR_A_MA[0..15]

M1 Circuit
+1.5V
R79 1K_0402_1%
R81 1K_0402_1%
+V_DDR3_DIMM_REF
R78 0_0402_5%
R80 0_0402_5%
+VREF_DQB
+VREF_DQA

+V_DDR3_DIMM_REF
R89 0_0402_5%
+DDR_VREF_CA_DIMMA
C161 2.2U_0603_6.3V4Z
C162 0.1U_0402_16V4Z
close to JDDRL.126

R90 10K_0402_5%
+3VSO
C181 2.2U_0603_6.3V4Z
C182 0.1U_0402_16V4Z
R91 10K_0402_5%
+0.75VS

Layout Note:
Place near JDDRL

C218 390U_2.5V_M_R10
C166 10U_0805_6.3V6M
C168 10U_0805_6.3V6M
C171 10U_0805_6.3V6M
C174 10U_0805_6.3V6M
C176 10U_0805_6.3V6M
C178 10U_0805_6.3V6M

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

C164 0.1U_0402_16V4Z
C167 0.1U_0402_16V4Z
C170 0.1U_0402_16V4Z
C173 0.1U_0402_16V4Z

Layout Note:
Place near JDDRL1.203 and 204

C165 10U_0805_6.3V6M
C169 1U_0402_6.3V4Z
C172 1U_0402_6.3V4Z
C175 1U_0402_6.3V4Z
C177 1U_0402_6.3V4Z

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Standard Type
DDR3 SO-DIMM B

7 DDR_B_DQS#[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_MA[0..15]

JDDRH

+VREF_DQB

close to JDDRH.1

C183 2.2U_0603_6.3V4Z
C184 0.1U_0402_16V4Z

	DDR_B_D0	3	VREF_DQ	VSS	2		
	DDR_B_D1	5	VSS	DQ4	4	DDR_B_D4	
		7	DQ0	DQ5	6	DDR_B_D5	
		9	DQ1	VSS	8		
	DDR_B_DM0	11	VSS	DQS0#	10	DDR_B_DQS#0	
		13	DM0	DQS0	12	DDR_B_DQS0	
	DDR_B_D2	15	VSS	VSS	14		
	DDR_B_D3	17	DQ2	DQ6	16	DDR_B_D6	
		19	DQ3	DQ7	18	DDR_B_D7	
	DDR_B_D8	21	VSS	VSS	20		
	DDR_B_D9	23	DQ8	DQ12	22	DDR_B_D12	
		25	DQ9	DQ13	24	DDR_B_D13	
	DDR_B_DQS#1	27	VSS	VSS	26		
	DDR_B_DQS1	29	DQS1#	DM1	28	DDR_B_DM1	
		31	DQS1	RESET#	30	SM_DRAMRST# 5,11	
	DDR_B_D10	33	VSS	VSS	32		
	DDR_B_D11	35	DQ10	DQ14	34	DDR_B_D14	
		37	DQ11	DQ15	36	DDR_B_D15	
	DDR_B_D16	39	VSS	VSS	38		
	DDR_B_D17	41	DQ16	DQ20	40	DDR_B_D20	
		43	DQ17	DQ21	42	DDR_B_D21	
	DDR_B_DQS#2	45	VSS	VSS	44		
	DDR_B_DQS2	47	DQS2#	DM2	46	DDR_B_DM2	
		49	DQS2	VSS	48		
	DDR_B_D18	51	VSS	DQ22	50	DDR_B_D22	
	DDR_B_D19	53	DQ18	DQ23	52	DDR_B_D23	
		55	DQ19	VSS	54		
	DDR_B_D24	57	VSS	DQ28	56	DDR_B_D28	
	DDR_B_D25	59	DQ24	DQ29	58	DDR_B_D29	
		61	DQ25	VSS	60		
	DDR_B_DM3	63	VSS	DQS3#	62	DDR_B_DQS#3	
		65	DM3	DQS3	64	DDR_B_DQS3	
	DDR_B_D26	67	VSS	VSS	66		
	DDR_B_D27	69	DQ26	DQ30	68	DDR_B_D30	
		71	DQ27	DQ31	70	DDR_B_D31	
			VSS	VSS	72		
7 DDRB_CKE0		73	CKE0	CKE1	74	DDRB_CKE1 7	
		75	VDD	VDD	76		
		77	NC	A15	78	DDR_B_MA15	
7 DDR_B_BS2		79	BA2	A14	80	DDR_B_MA14	
		81	VDD	VDD	82		
	DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11	
	DDR_B_MA9	85	A9	A7	86	DDR_B_MA7	
		87	VDD	VDD	88		
	DDR_B_MA8	89	A8	A6	90	DDR_B_MA6	
	DDR_B_MA5	91	A5	A4	92	DDR_B_MA4	
		93	VDD	VDD	94		
	DDR_B_MA3	95	A3	A2	96	DDR_B_MA2	
	DDR_B_MA1	97	A1	A0	98	DDR_B_MA0	
		99	VDD	VDD	100		
7 DDRB_CLK0		101	CK0	CK1	102	DDRB_CLK1 7	
7 DDRB_CLK0#		103	CK0#	CK1#	104	DDRB_CLK1# 7	
	DDR_B_MA10	105	VDD	VDD	106		
		107	A10/AP	BA1	108	DDR_B_BS1 7	
7 DDR_B_BS0		109	BA0	RAS#	110	DDR_B_RAS# 7	
		111	VDD	VDD	112		
7 DDR_B_WE#		113	WE#	S0#	114	DDRB_SCS0# 7	
7 DDR_B_CAS#		115	CAS#	ODT0	116	DDRB_ODT0 7	
		117	VDD	VDD	118		
	DDR_B_MA13	119	A13	ODT1	120	DDRB_ODT1 7	
7 DDRB_SCS1#		121	S1#	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREF_CA	126	+DDR_VREF_CA_DIMMB	
		127	VSS	VSS	128		
	DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D36	
	DDR_B_D33	131	DQ33	DQ37	132	DDR_B_D37	
		133	VSS	VSS	134		
	DDR_B_DQS#4	135	DQS4#	DM4	136	DDR_B_DM4	
	DDR_B_DQS4	137	DQS4	VSS	138		
		139	VSS	DQ38	140	DDR_B_D38	
	DDR_B_D34	141	DQ34	DQ39	142	DDR_B_D39	
	DDR_B_D35	143	DQ35	VSS	144		
		145	VSS	DQ44	146	DDR_B_D44	
	DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D45	
	DDR_B_D41	149	DQ41	VSS	150		
		151	VSS	DQS5#	152	DDR_B_DQS#5	
	DDR_B_DM5	153	DM5	DQS5	154	DDR_B_DQS5	
		155	VSS	VSS	156		
	DDR_B_D42	157	DQ42	DQ46	158	DDR_B_D46	
	DDR_B_D43	159	DQ43	DQ47	160	DDR_B_D47	
		161	VSS	VSS	162		
	DDR_B_D48	163	DQ48	DQ52	164	DDR_B_D52	
	DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D53	
		167	VSS	VSS	168		
	DDR_B_DQS#6	169	DQS6#	DM6	170	DDR_B_DM6	
	DDR_B_DQS6	171	DQS6	VSS	172		
		173	VSS	DQ54	174	DDR_B_D54	
	DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D55	
	DDR_B_D51	177	DQ51	VSS	178		
		179	VSS	DQ60	180	DDR_B_D60	
	DDR_B_D56	181	DQ56	DQ61	182	DDR_B_D61	
	DDR_B_D57	183	DQ57	VSS	184		
		185	VSS	DQS7#	186	DDR_B_DQS#7	
	DDR_B_DM7	187	DM7	DQS7	188	DDR_B_DQS7	
		189	VSS	VSS	190		
	DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D62	
	DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D63	
		195	VSS	VSS	196		
		197	SA0	EVENT#	198	PM_EXTTS# 5,11	
		199	VDDSPD	SDA	200	PM_SMBDATA 11,21,24,33	
		201	SA1	SCL	202	PM_SMBCLK 11,21,24,33	
		203	VTT	VTT	204	+0.75VS	
		205	GND1	BOSS1	206		
		207	GND2	BOSS2	208		

FOX_AS0A626-UASN-7F_204P
@

R97 1 2 0_0402_5%
+V_DDR3_DIMM_REF

close to JDDRH.126

C187 2.2U_0603_6.3V4Z
C188 0.1U_0402_16V4Z

R98 1 2 10K_0402_5%
R99 1 2 10K_0402_5%
+3VS
+0.75VS
C207 2.2U_0603_6.3V4Z
C208 0.1U_0402_16V4Z

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

+1.5V
C189 330U_B2_2.5VM_R15M
C192 10U_0805_6.3V6M
C194 10U_0805_6.3V6M
C197 10U_0805_6.3V6M
C200 10U_0805_6.3V6M
C202 10U_0805_6.3V6M
C204 10U_0805_6.3V6M

+1.5V
C190 0.1U_0402_16V4Z
C193 0.1U_0402_16V4Z
C196 0.1U_0402_16V4Z
C199 0.1U_0402_16V4Z

Layout Note:
Place near JDDRH.203 and 204

+0.75VS
C191 10U_0805_6.3V6M
C195 1U_0402_6.3V4Z
C198 1U_0402_6.3V4Z
C201 1U_0402_6.3V4Z
C203 1U_0402_6.3V4Z

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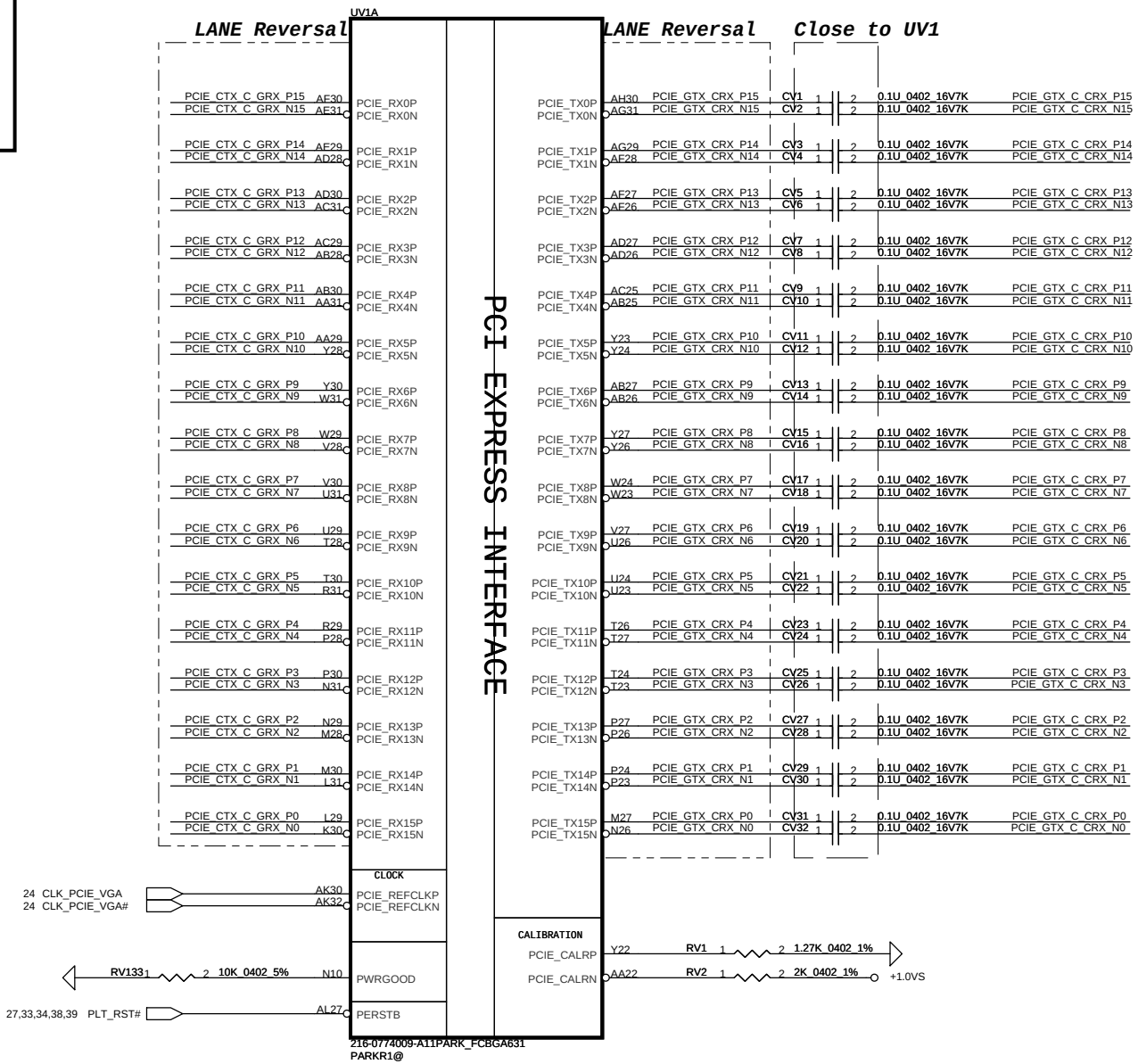
6 PCIE_GTX_C_CRX_P[0..15] → PCIE_GTX_C_CRX_P[0..15]
6 PCIE_GTX_C_CRX_N[0..15] → PCIE_GTX_C_CRX_N[0..15]
6 PCIE_CTX_C_GRX_P[0..15] → PCIE_CTX_C_GRX_P[0..15]
6 PCIE_CTX_C_GRX_N[0..15] → PCIE_CTX_C_GRX_N[0..15]



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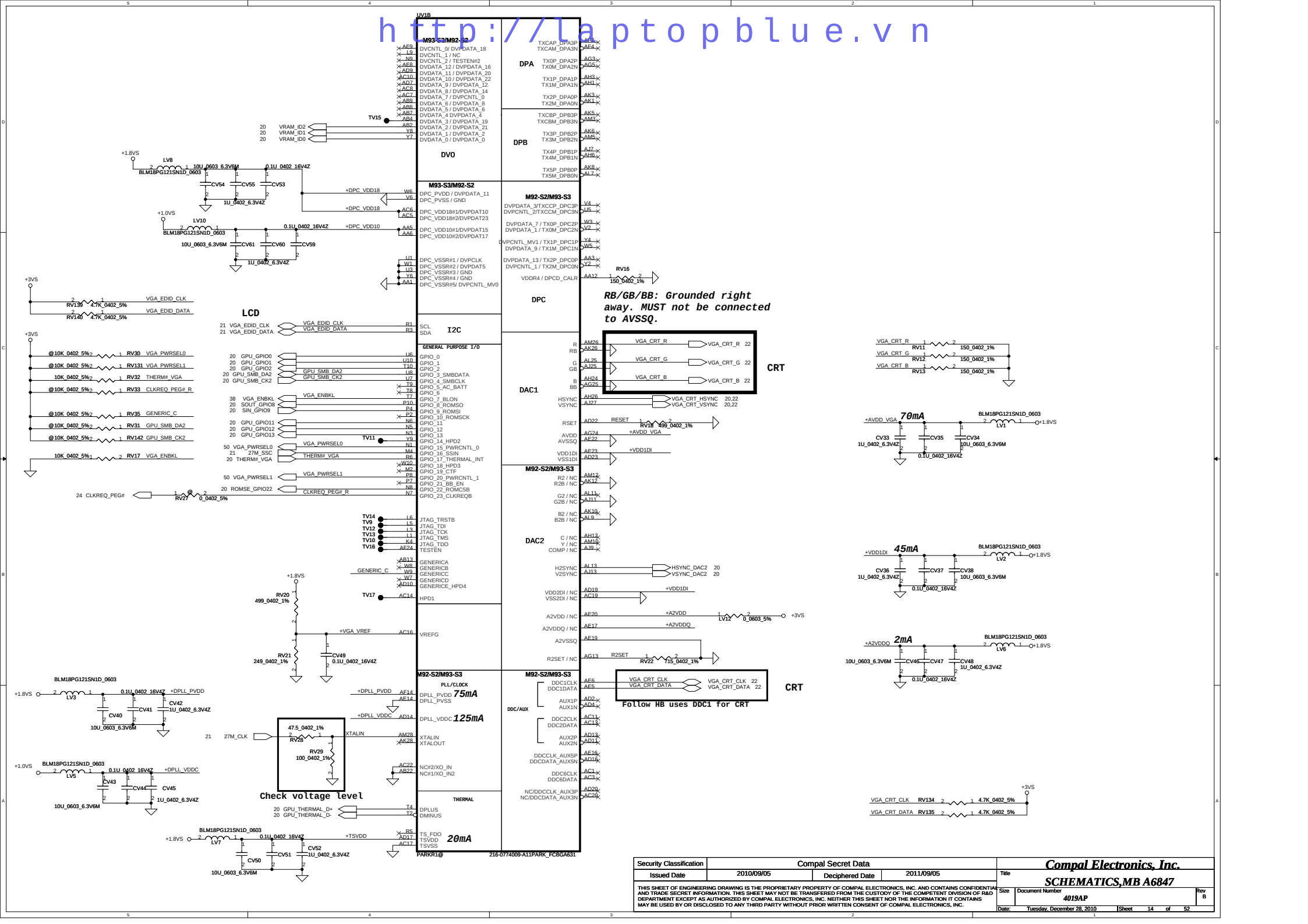

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Title	SCHEMATICS,MB A6847
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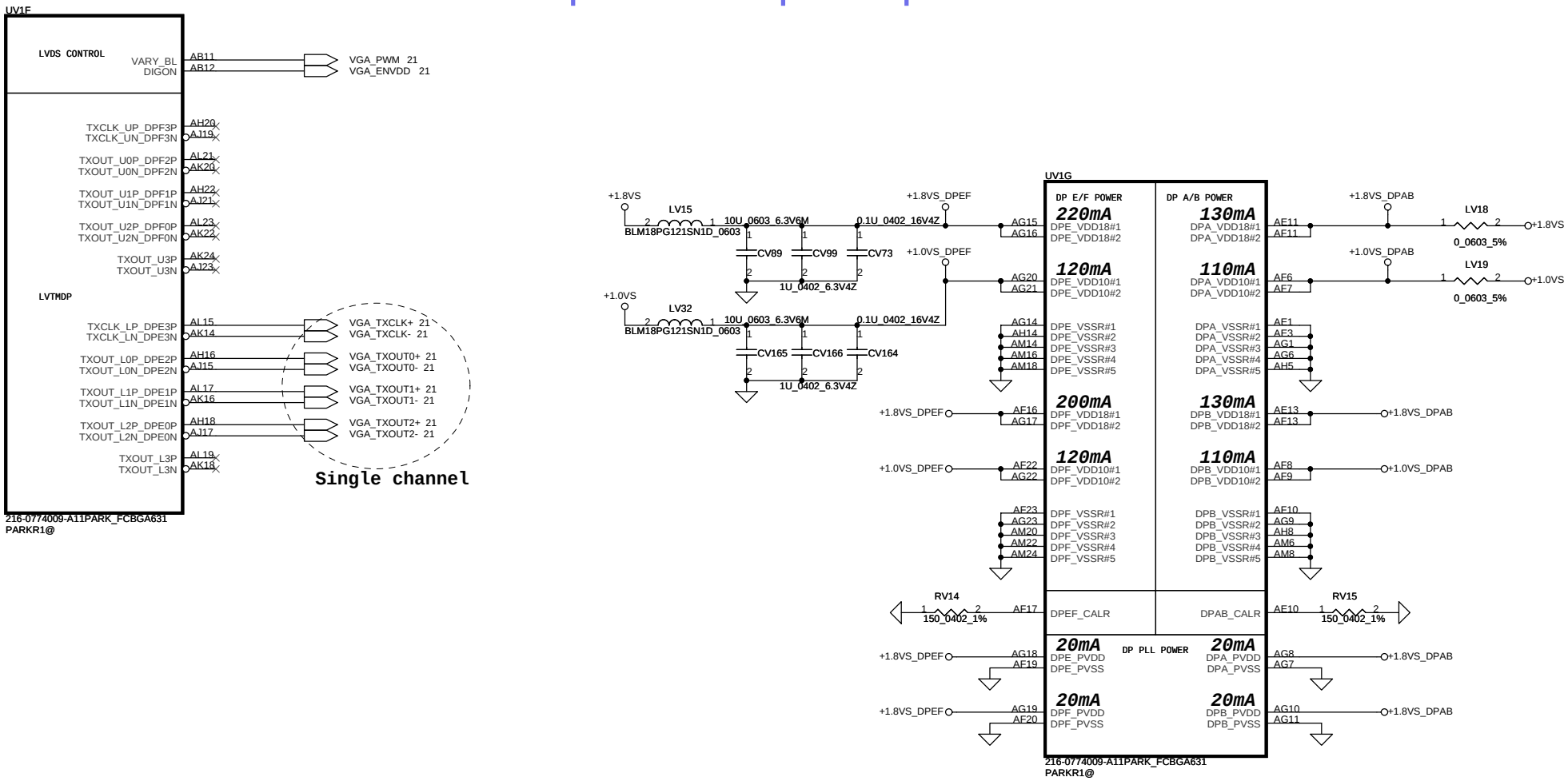

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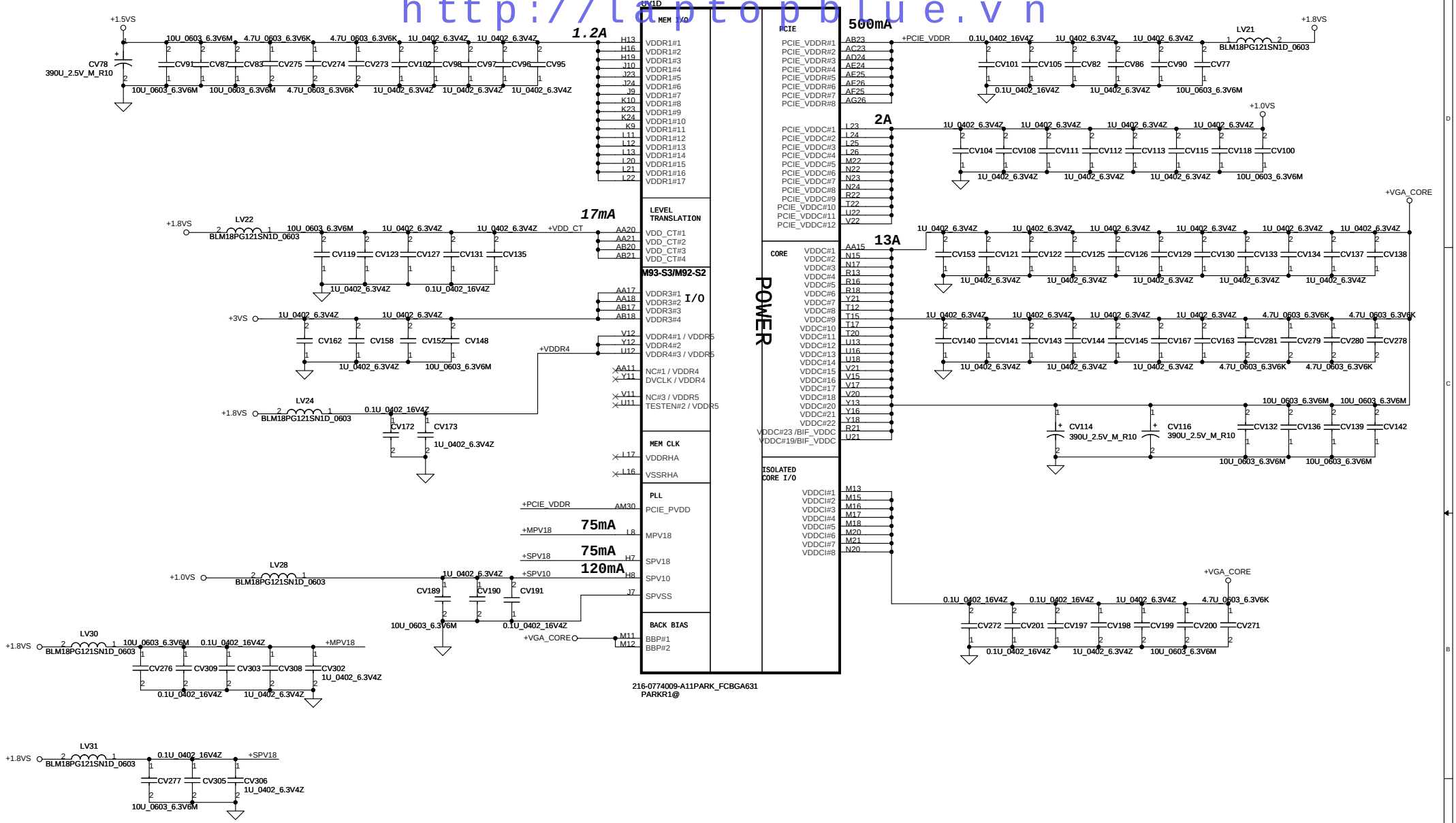

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Compal Electronics, Inc.			
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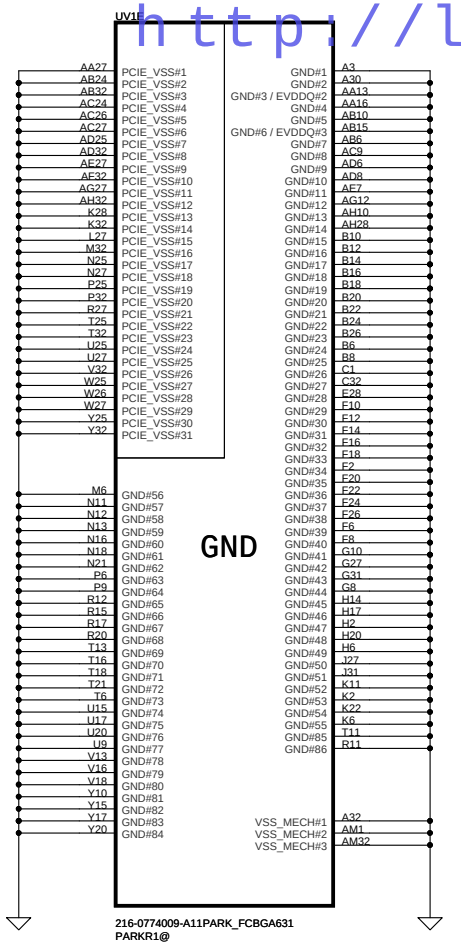

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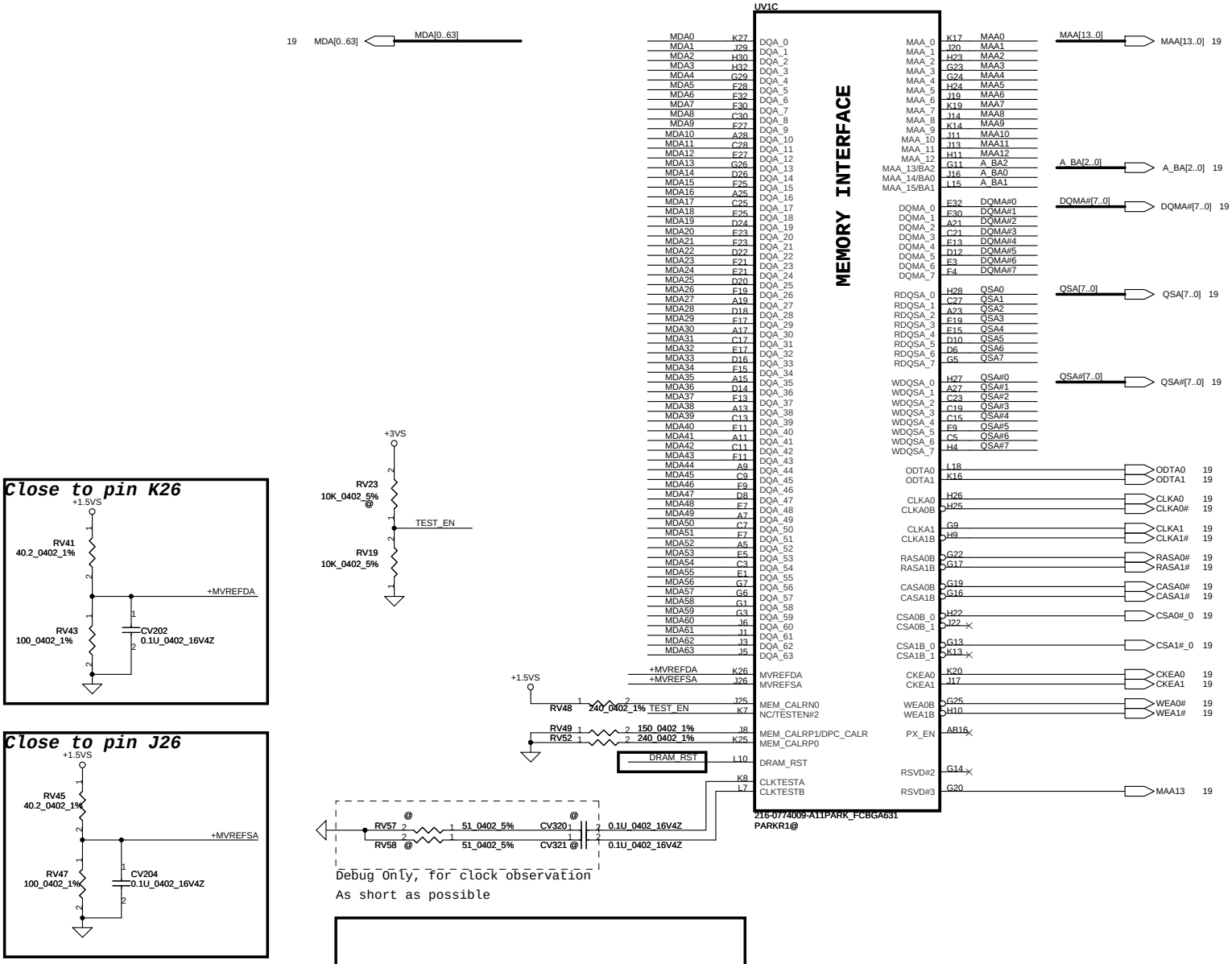

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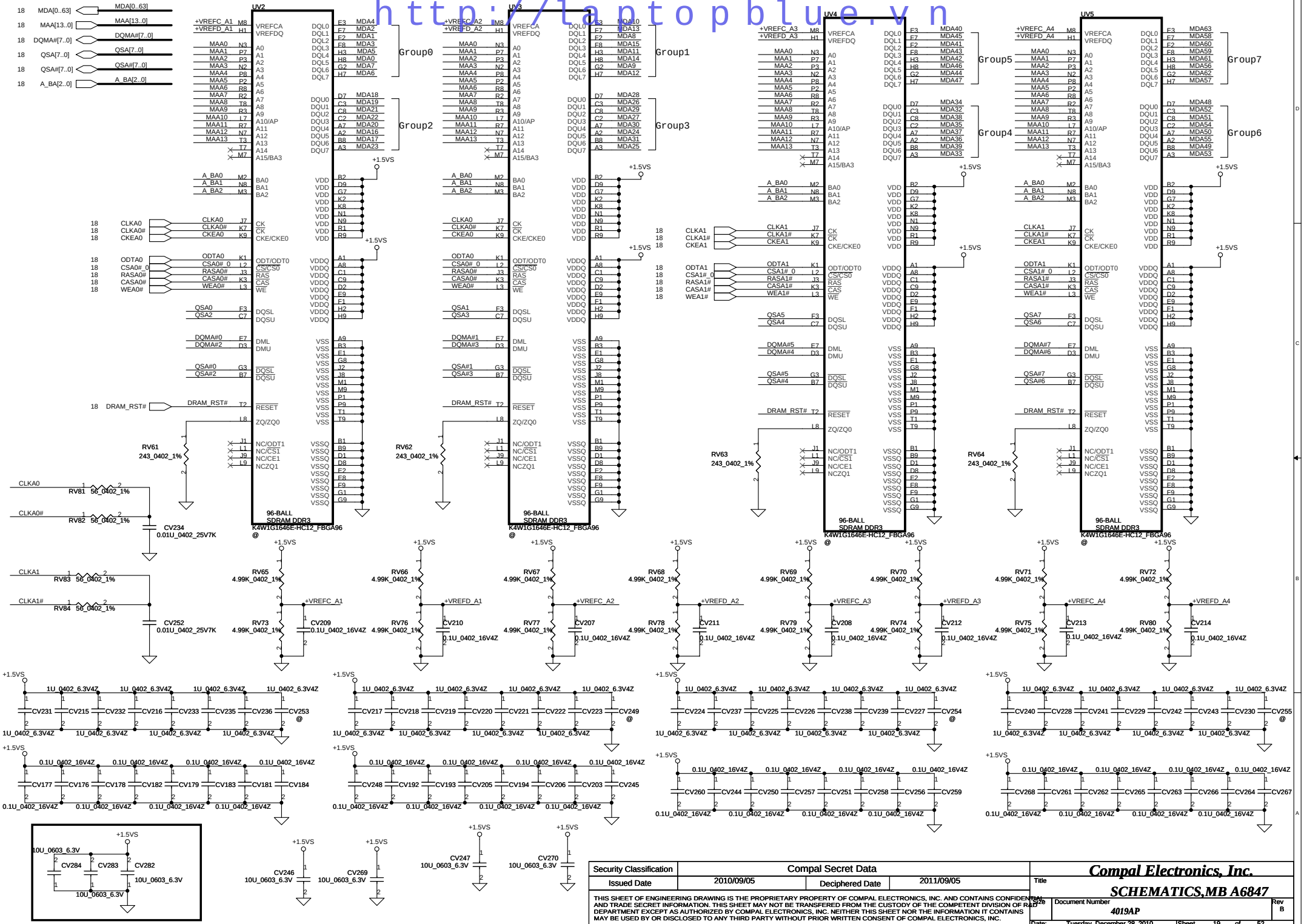

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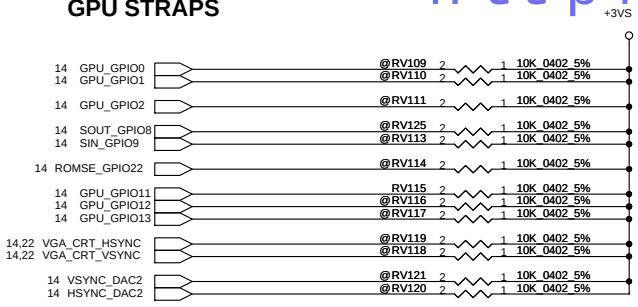
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0		GPIO22 = 1 (BIOS_ROM_EN = 1
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	

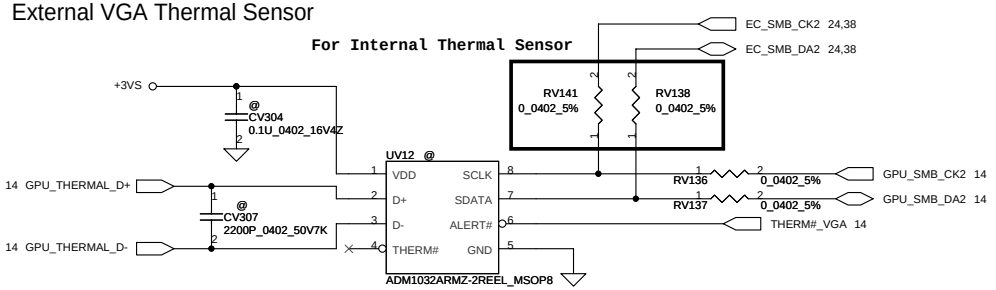
CONFIGURATION STRAPS

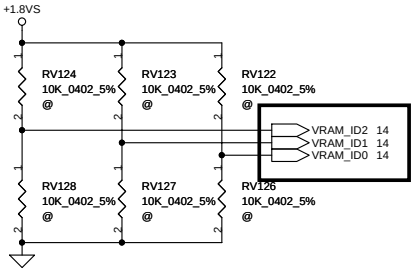
ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
VIP_DEVICE_STRAP_DIS	V2SYNC	VSYNC_DAC2	VIP Device Strap Enable indicates to the software driver 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device is connected	0
RESERVED	H2SYNC	HSYNC_DAC2	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

External VGA Thermal Sensor

For Internal Thermal Sensor





Need to check the VBIOS setting

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVDATA (2,1,0)	Park XT S3	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C	SA00003VS00	0 1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC12	SA00003MQ40	0 1 1
				Design Ready		
		Robson LP S3	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	1 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C	SA00003VS00	1 1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC12	SA00003MQ40	1 1 1
				Design Ready		

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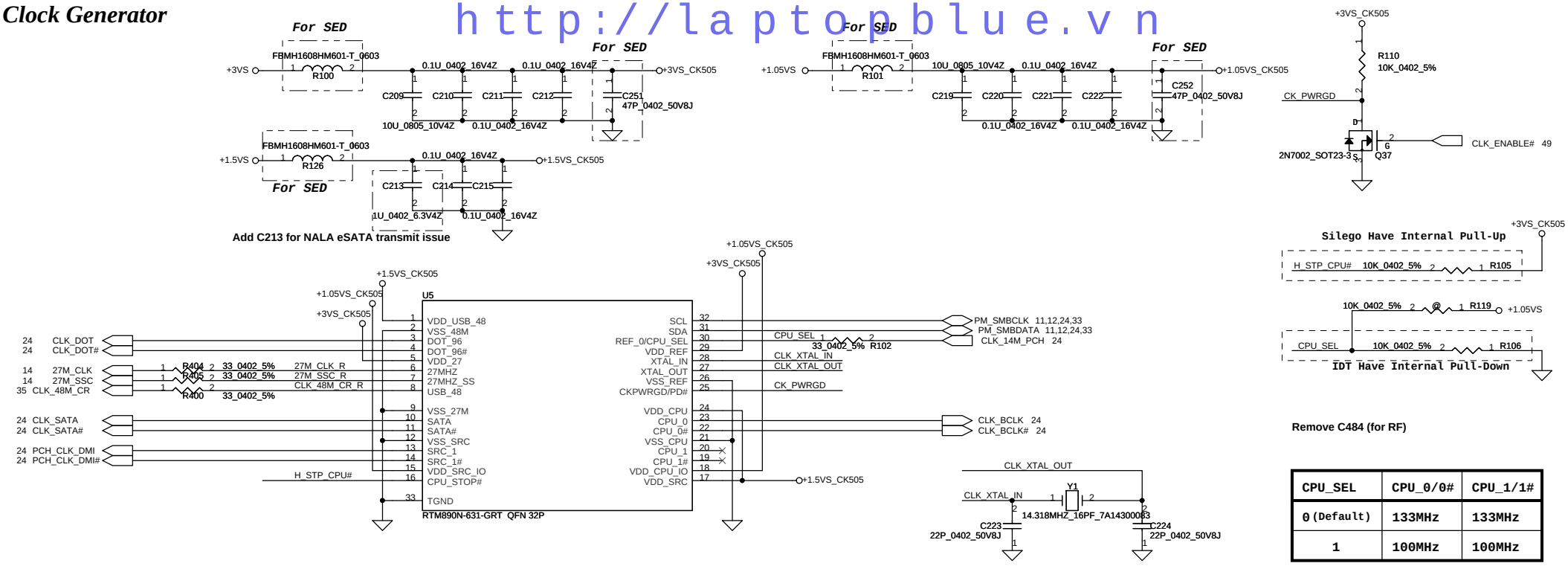
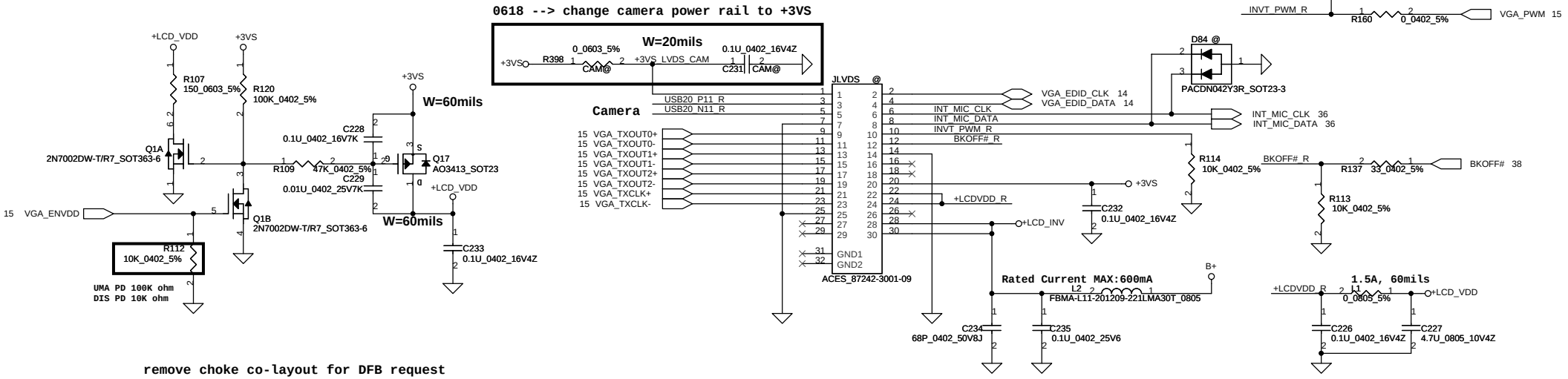
Clock Generator



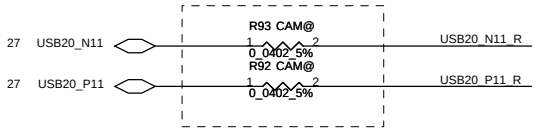
Remove C484 (for RF)

CPU_SEL	CPU_0/0#	CPU_1/1#
0(Default)	133MHz	133MHz
1	100MHz	100MHz

LVDS / Int.Camera / Int.MIC Conn



remove choke co-layout for DFB request



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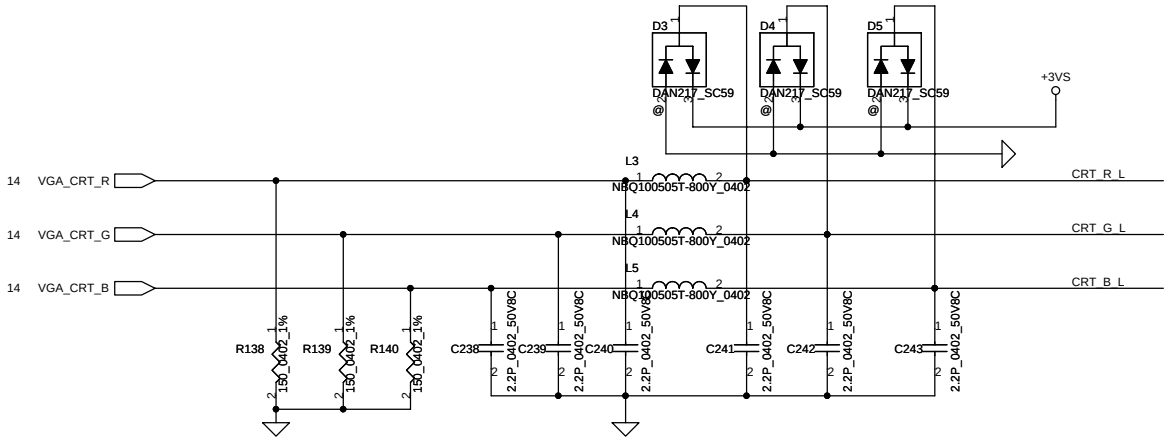
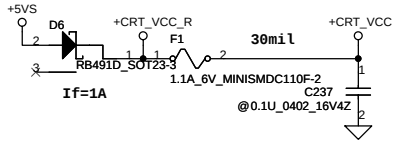
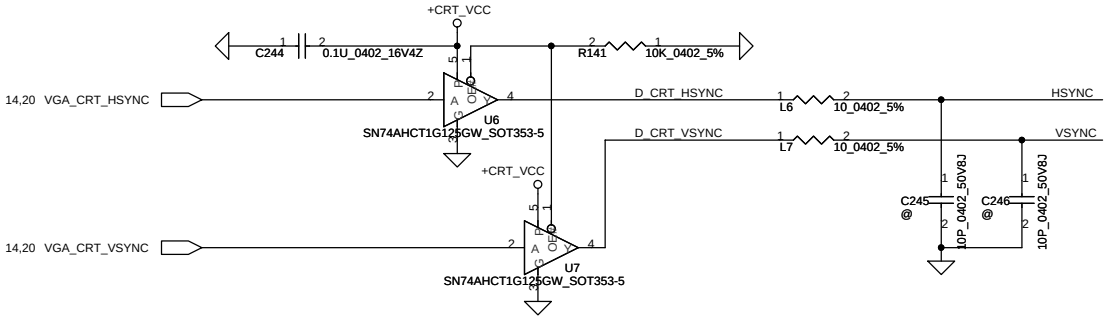
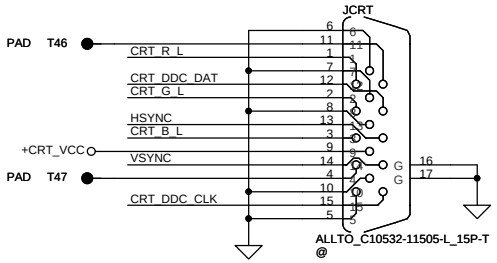
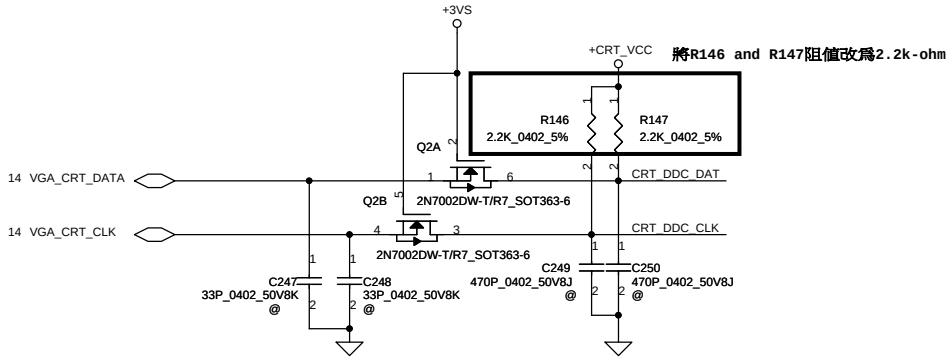
CRT CONNECTOR











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CMOS Setting, near DDR Door

+RTCVCC — R282 20K_0402_1% — PCH_RTCRST# — JCMOS — C288 1U_0402_6.3V4Z

iME Setting.

+RTCVCC — R284 20K_0402_1% — PCH_SRTCRST# — J2 — C289 1U_0402_6.3V4Z

C287 15P_0402_50V8J — Y3 32.768KHZ_12.5PF_Q13MC14610002 — C290 15P_0402_50V8J — R283 10M_0402_5%

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Overide

HDA_DOCK_EN#	Low = Enabled High = Disabled *

ITPM Enabled — Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)

U11A

RTC: PCH_RTCX1 B13 — RTCX1; PCH_RTCX2 D13 — RTCX2; PCH_RTCRST# C14 — RTCRST#; PCH_SRTCRST# D17 — SRTCRST#; SM_INTRUDER# A16 — INTRUDER#; PCH_INTVRMEN A14 — INTVRMEN

LPC: FWH0 / LAD0 D33; FWH1 / LAD1 B33; FWH2 / LAD2 C32; FWH3 / LAD3 A32 — LPC_AD0 38,39; LPC_AD1 38,39; LPC_AD2 38,39; LPC_AD3 38,39; FWH4 / LFRAME# C34 — LPC_FRAME# 38,39; LDRQ0# A34; LDRQ1# / GPIO23 F34 — remove FELICA_PWR#; SERIRQ AB9 — SERIRQ 38,39

IHDA: AZ_BITCLK A30 — HDA_BCLK; AZ_SYNC D29 — HDA_SYNC; 26,36 PCH_SPKR — PCH_SPKR P1 — SPKR; AZ_RST# C30 — HDA_RST#; 36 AZ_SDIN0_HD — G30 — HDA_SDIN0; remove SDN1 for MDC; E30 — HDA_SDIN1; F32 — HDA_SDIN2; F32 — HDA_SDIN3; @R118 1K_0402_5% AZ_SDOUT — B29 — HDA_SDO; 38 PWRME_CTRL# — H32 — HDA_DOCK_EN# / GPIO33; remove CR_CPPE# for JM385; J30 — HDA_DOCK_RST# / GPIO13

SATA: SATA0RXN AK7; SATA0RXP AK6; SATA0TXN AK11; SATA0TXP AK9 — SATA_PRX_C_DTX_N1 32; SATA_PRX_C_DTX_P1 32; SATA_PTX_DRX_N1 32; SATA_PTX_DRX_P1 32 — 1ST HDD

SATA1RXN AH6; SATA1RXP AH5; SATA1TXN AH9; SATA1TXP AH8

SATA2RXN AE11; SATA2RXP AE9; SATA2TXN AE7; SATA2TXP AE6; SATA3RXN AH3; SATA3RXP AH1; SATA3TXN AF3; SATA3TXP AF1 — Desktop Only

SATA4RXN AD9; SATA4RXP AD8; SATA4TXN AD6; SATA4TXP AD5 — SATA_PRX_C_DTX_N4 32; SATA_PRX_C_DTX_P4 32; SATA_PTX_DRX_N4 32; SATA_PTX_DRX_P4 32 — SATA ODD

SATA5RXN AD3; SATA5RXP AD1; SATA5TXN AB3; SATA5TXP AB1 — remove eSATA SATA

JTAG: PCH_JTAG_TCK M3 — JTAG_TCK; PCH_JTAG_TMS K3 — JTAG_TMS; PCH_JTAG_TDI K1 — JTAG_TDI; PCH_JTAG_TDO J2 — JTAG_TDO; PCH_JTAG_RST# J4 — TRST#

SATAICOMPO AF16; SATAICOMPI AF15 — SATAICOMP — R295 37.4_0402_1% — +1.05VS

SPI: PCH_SPI_CLK BA2 — SPI_CLK; PCH_SPI_CS0# AV3 — SPI_CS0#; AY3 — SPI_CS1#; +3VS — R273 1K_0402_5% — PCH_SPI_MOSI AY1 — SPI_MOSI; PCH_SPI_MISO AV1 — SPI_MISO

SATALED# T3 — SATA_LED#

SATA0GP / GPIO21 Y9 — PCH_GPIO21

SATA1GP / GPIO19 V1 — PCH_GPIO19

IBEXPEAK-M QV20 A0_FCBGA1071 — HM55R1@

RTC schematic for non-chargeable

+RTCVCC — D10 CHN202UPT SC-70 — +3VL — +RTCBATT — R277 1K_0402_5% — C291 0.1U_0402_16V4Z

@ JRTC LOTES_AAA-BAT-054-K01

36 AZ_BITCLK_HD — R288 33_0402_5% — AZ_BITCLK

36 AZ_SYNC_HD — R290 33_0402_5% — AZ_SYNC

36 AZ_RST_HD# — R292 33_0402_5% — AZ_RST#

36 AZ_SDOUT_HD — R294 33_0402_5% — AZ_SDOUT

+3VS — PCH_GPIO21 R302 10K_0402_5%; SATA_LED# R301 10K_0402_5%; PCH_GPIO19 R306 10K_0402_5%

+3VALW — @R386 200_0402_5% — PCH_JTAG_TMS — @R355 100_0402_5%

+3VALW — @R363 200_0402_5% — PCH_JTAG_TDO — @R535 100_0402_5%

+3VALW — @R536 200_0402_5% — PCH_JTAG_TDI — @R537 100_0402_5%

+3VALW — @R643 20K_0402_5% — PCH_JTAG_RST# — @R364 10K_0402_5%

R156 51_0402_5% — PCH_JTAG_TCK

06/01 change R125 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

For EMI Place near U13

PCH_SPI_CLK — R385 @ 10_0402_5% — @ C16 10P_0402_50V8J

4MB

+3VS — C293 0.1U_0402_16V4Z — U13 MX25L3205DM2I-12G SO8

PCH_SPI_CS0# — PCH_SPI_CLK — PCH_SPI_MOSI — PCH_SPI_MISO

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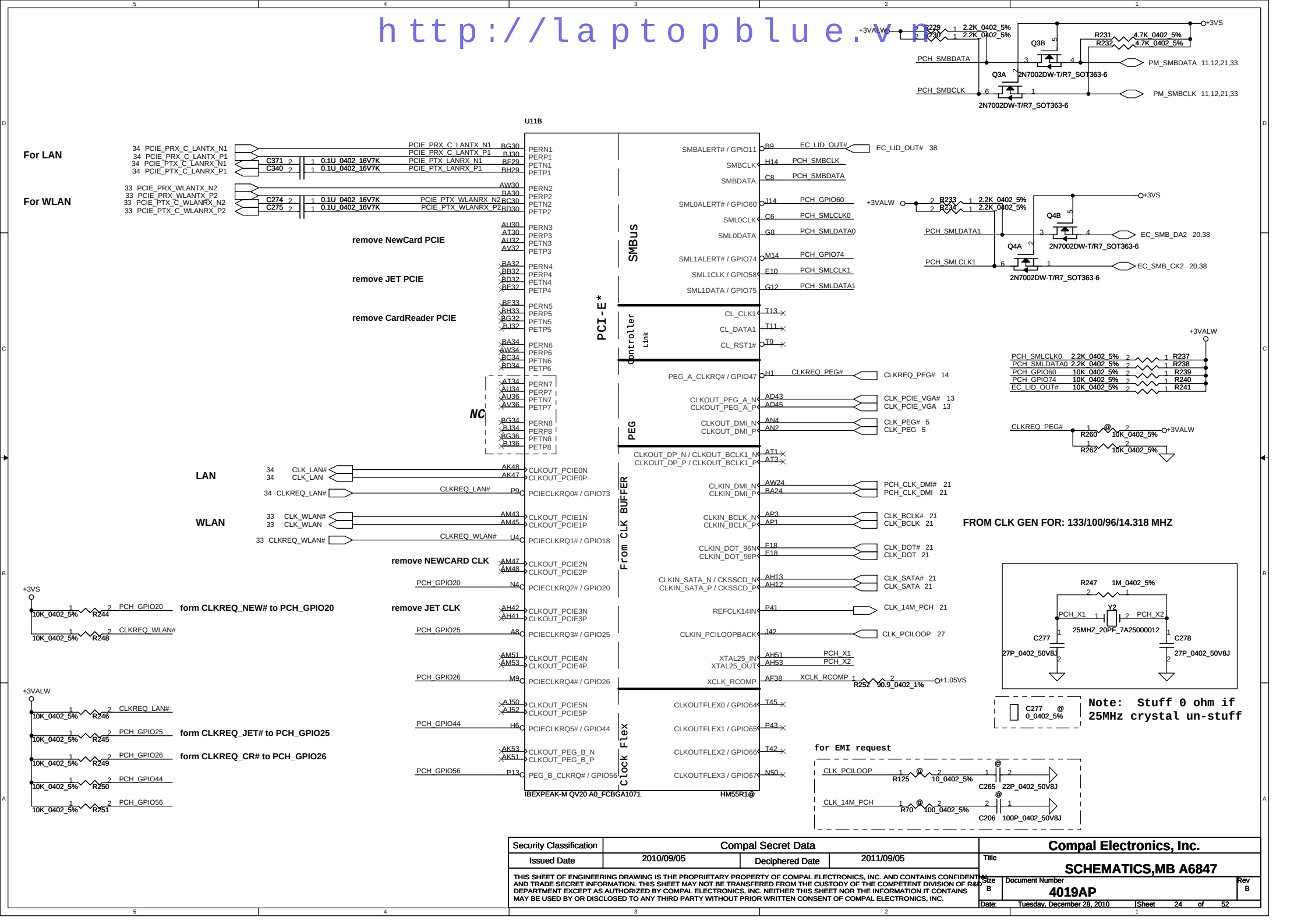

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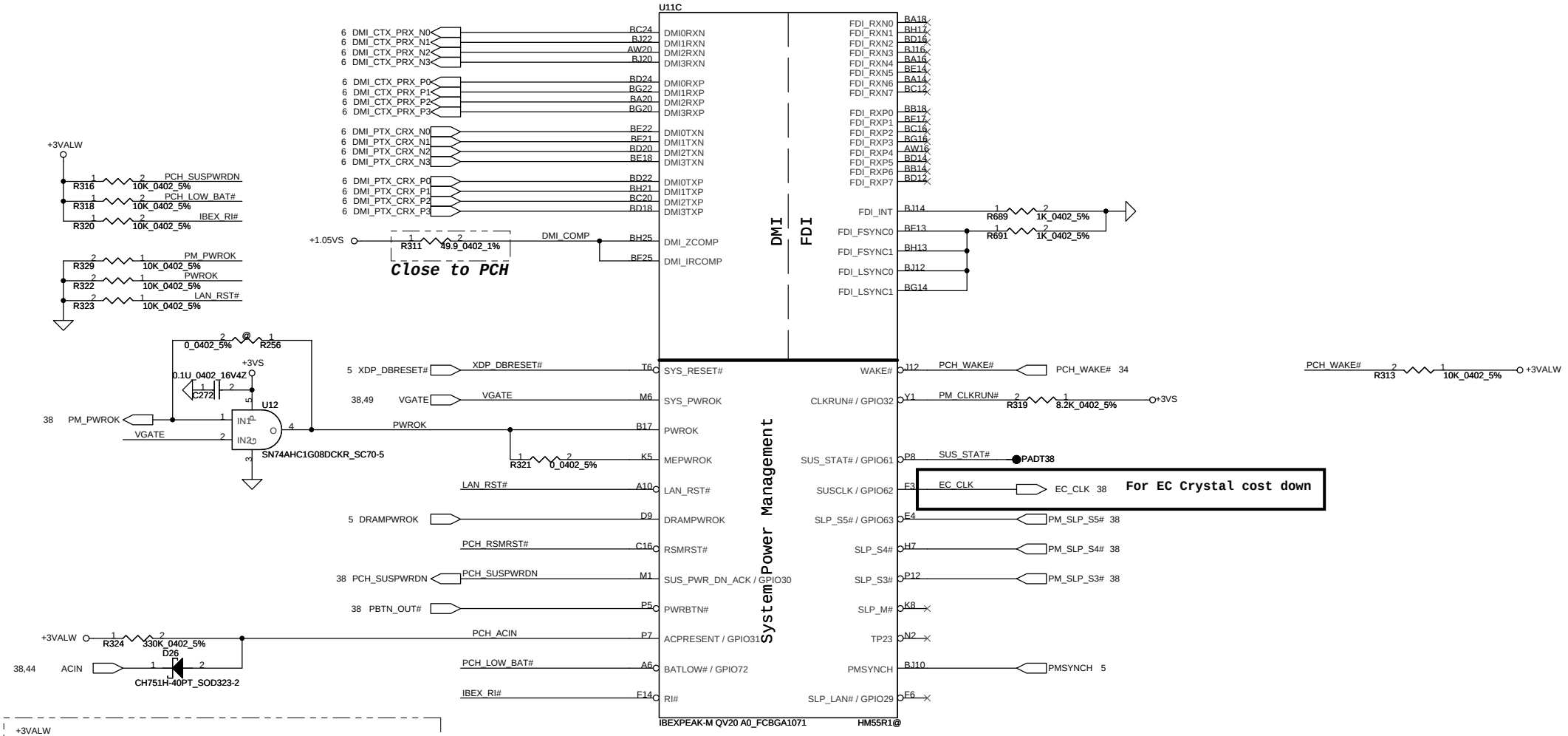

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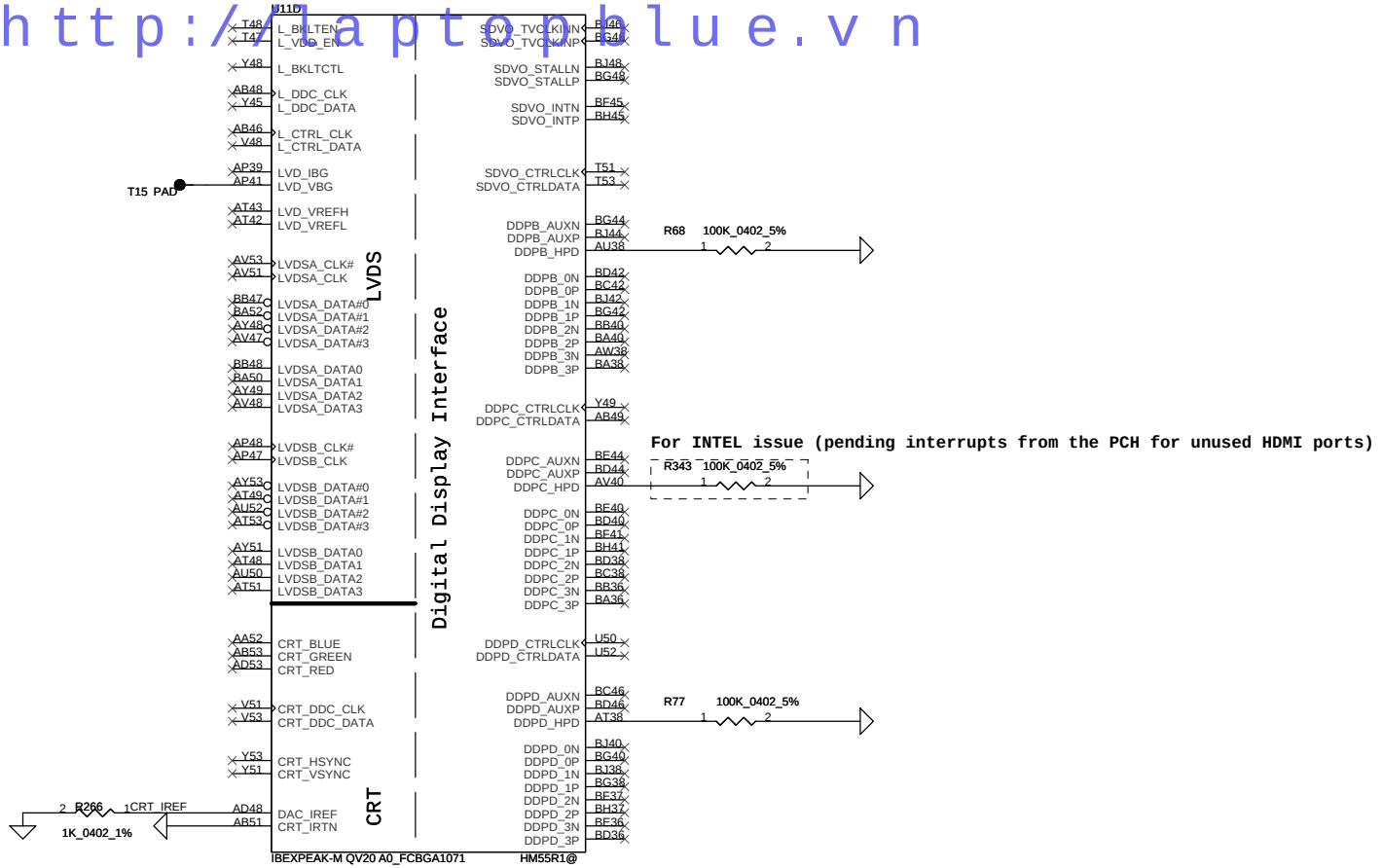
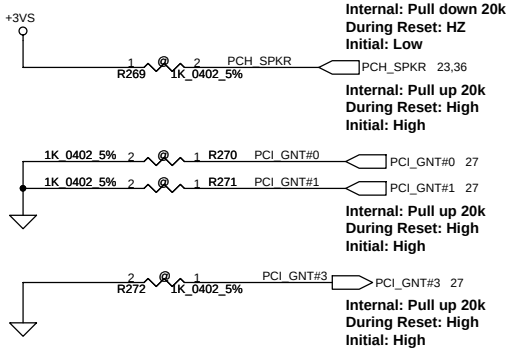


PCH Strap Pin



Internal: Pull down 20k
During Reset: HZ
Initial: Low

Internal: Pull up 20k
During Reset: High
Initial: High

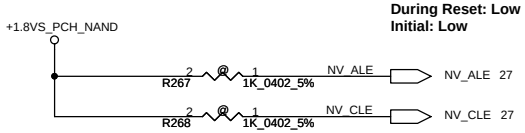
Internal: Pull up 20k
During Reset: High
Initial: High

Internal: Pull up 20k
During Reset: High
Initial: High

NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Internal: Pull down 20k
During Reset: Low
Initial: Low

Internal: Pull down 20k
During Reset: Low
Initial: Low

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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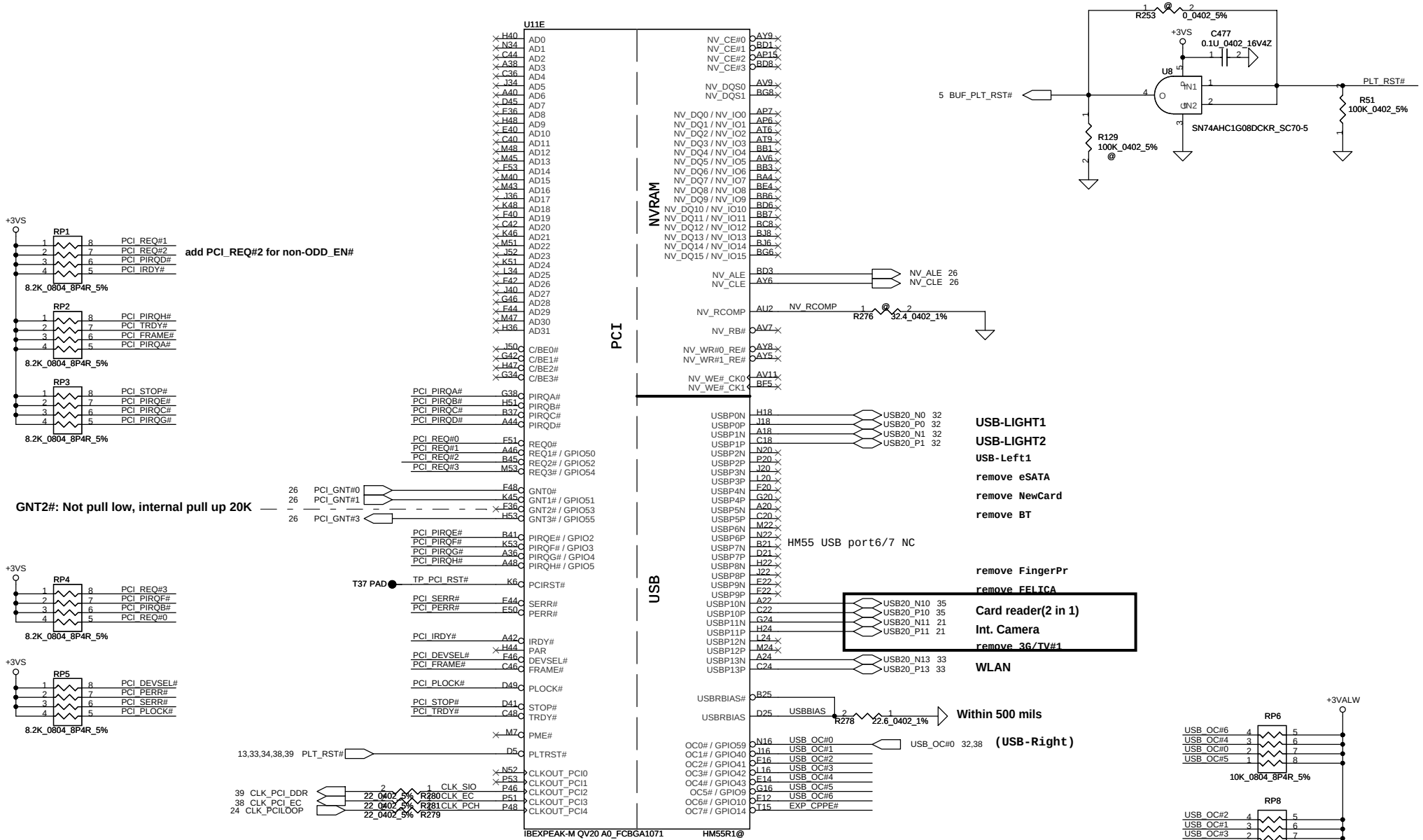

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pull down 100k to GND

R189 100K_0402_5%

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR	
PCH_GPIO27	High = Enabled (Default) Low = Disabled

PROJECT_ID		
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NWQAA 16"	H	L
NALAA 17.3"	H	H

U11F

PCH_HDMI_HPD	Y3	BMBUSY# / GPIO0	MISC	CLKOUT_PCIE6N	AH45
PCH_GPIO1	C38	TACH1 / GPIO1		CLKOUT_PCIE6P	AH46
PCH_GPIO6	D37	TACH2 / GPIO6			
38 EC_SCI# / EC_SCI#	J32	TACH3 / GPIO7		CLKOUT_PCIE7N	AF48
38 EC_SMI# / EC_SMI#	F10	GPIO8		CLKOUT_PCIE7P	AF47
PCH_GPIO12	K9	LAN_PHY_PWR_CTRL / GPIO12		A20GATE	U2 GATEA20 → GATEA20 38
PCH_GPIO15	T7	GPIO15			
PCH_GPIO16	AA2	SATA4GP / GPIO16		CLKOUT_BCLK0_N / CLKOUT_PCIE8N	AM3 → CLK_CPU_BCLK# 5
PCH_GPIO17	F38	TACH0 / GPIO17		CLKOUT_BCLK0_P / CLKOUT_PCIE8P	AM1 → CLK_CPU_BCLK 5
BT_DET#	Y7	SCLOCK / GPIO22		PECI	BG10 → PECI 5
	H10	GPIO24	GPIO	RCIN#	T1 KB_RST# → KB_RST# 38
R274 2 @ 1 1K_0402_5% / PCH_GPIO27	AB12	GPIO27		PROCPWRGD	BE10 → H_PWRGOOD 5
PCH_GPIO28	V13	GPIO28	CPU	THRMTRIP#	BD10 THRMTRIP_PCH# → R212 1 2 56_0402_1% → H_THERMTRIP# 5
33 BT_PWR#	M11	STP_PCI# / GPIO34			
remove BT_RST#	V6	SATACLKREQ# / GPIO35			R210 1 2 56_0402_1% → +VTT
PROJECT_ID0	AB7	SATA2GP / GPIO36		TP1	BA23
PROJECT_ID1	AB13	SATA3GP / GPIO37		TP2	AW22
PCH_GPIO38	V3	SLOAD / GPIO38		TP3	BB22
PCH_GPIO39	P3	SDATAOUT0 / GPIO39		TP4	AY45
LVDS_SEL	H3	PCIECLKRQ6# / GPIO45		TP5	AY46
5 RST_GATE / RST_GATE	F1	PCIECLKRQ7# / GPIO46		TP6	AV43
PCH_GPIO48	AB6	SDATAOUT1 / GPIO48		TP7	AV45
38 THM_ALT# / THM_ALT#	AA4	SATA5GP / GPIO49		TP8	AF13
PCH_GPIO57	F8	GPIO57		TP9	M18
				TP10	N18
				TP11	AJ24
				TP12	AK41
				TP13	AK42
				TP14	M32
				TP15	N32
				TP16	M30
				TP17	N30
				TP18	H12
				TP19	AA23
				NC_1	AB45
				NC_2	AB38
				NC_3	AB42
				NC_4	AB41
				NC_5	T39
				INIT3_3V#	P6
				TP24	C10

A4, A49, A5, A50, A52, A53, B2, B4, B52, B53, BE1, BE53, BE1, BF53, BH1, BH2, BH52, BH53, BJ1, BJ2, BJ4, BJ49, BJ5, BJ50, BJ52, BJ53, D1, D2, D53, E1, E53 — VSS_NCTF_1 … VSS_NCTF_31 (NCTF / RSVD)

IBEXPEAK-M QV20 A0_FCBGA1071 — HM55R1@

Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

+3VS

PCH_GPIO1	R214 10K_0402_5%
PCH_GPIO6	R218 10K_0402_5%
EC_SCI#	R224 10K_0402_5%
PCH_GPIO16	R221 10K_0402_5%
PCH_GPIO17	R220 10K_0402_5% — change Netname from RF_OFF# to PCH_GPIO17
BT_DET#	R215 8.2K_0402_5%
PCH_GPIO38	R217 10K_0402_5%
PCH_GPIO39	R254 10K_0402_5% — change R254 to 10k and Netname from CIR_EN# to PCH_GPIO39
PROJECT_ID0	R255 10K_0402_5%
PROJECT_ID1	R216 10K_0402_5%
PCH_GPIO48	R257 10K_0402_5% — change Netname from ISDBT_DET to PCH_GPIO39
THM_ALT#	R259 10K_0402_5%
BT_PWR#	R261 10K_0402_5% — add R261 10k for BT fun

+3VALW

EC_SMI#	R225 10K_0402_5%
PCH_GPIO57	R226 10K_0402_5%
PCH_GPIO15	R227 1K_0402_5%
PCH_GPIO28	R242 10K_0402_5%
LVDS_SEL	R222 10K_0402_5%
RST_GATE	R223 10K_0402_5%
PCH_GPIO12	R219 10K_0402_5%

LVDS_SEL=H
for Single Channel LVDS

PROJECT_ID0	R416 @ 10K_0402_5%
PROJECT_ID1	R415 @ 10K_0402_5%

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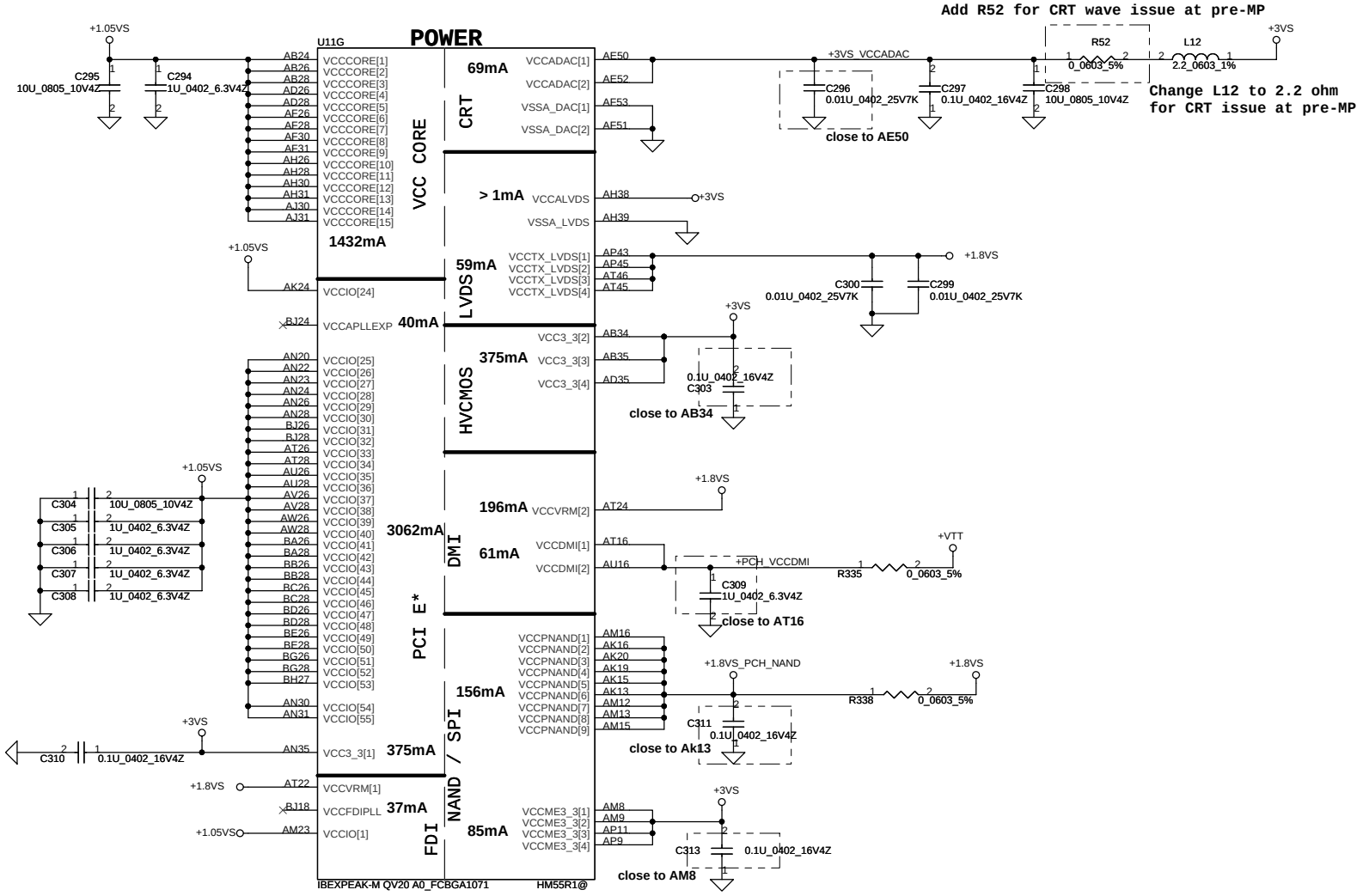

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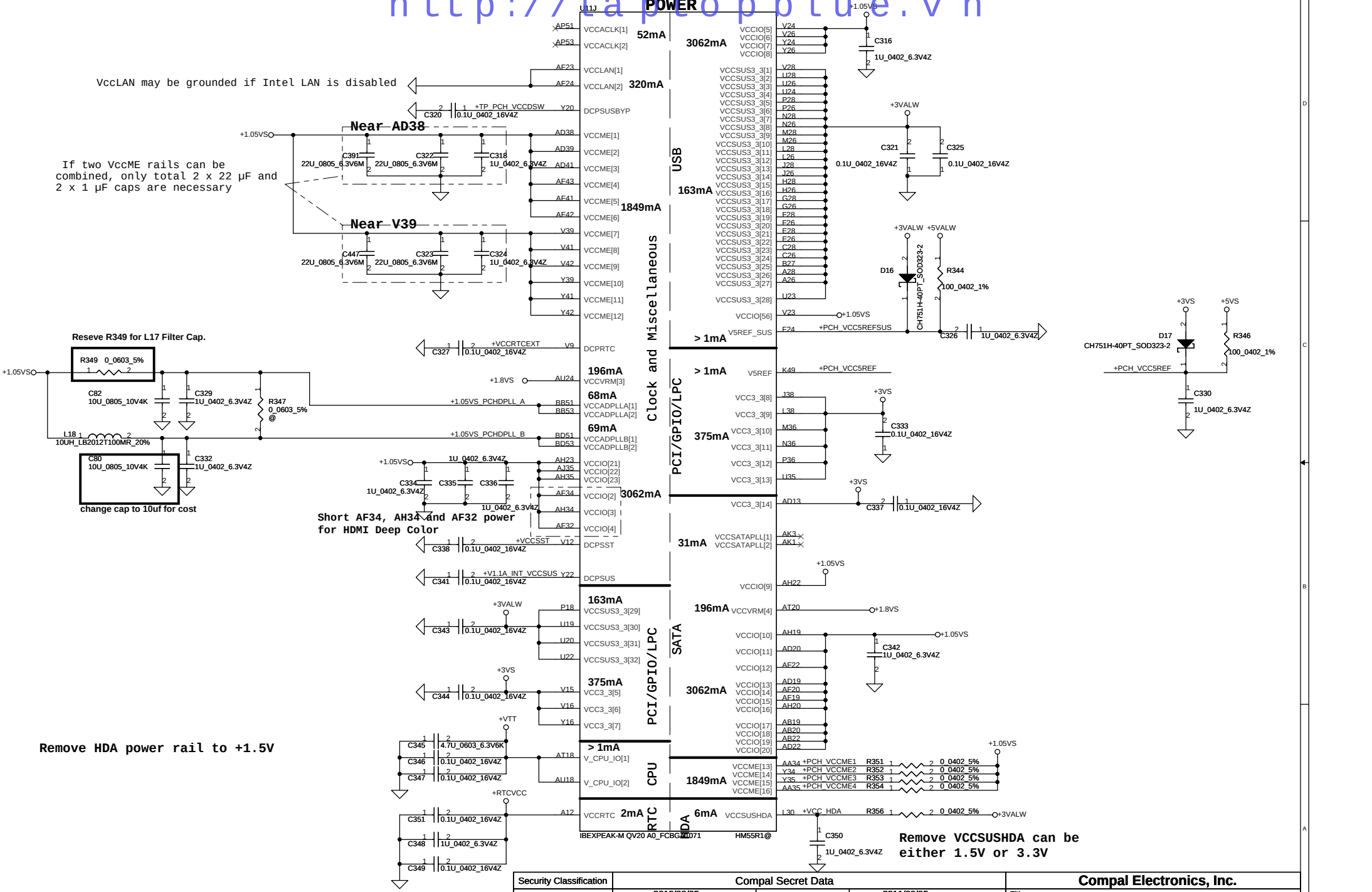

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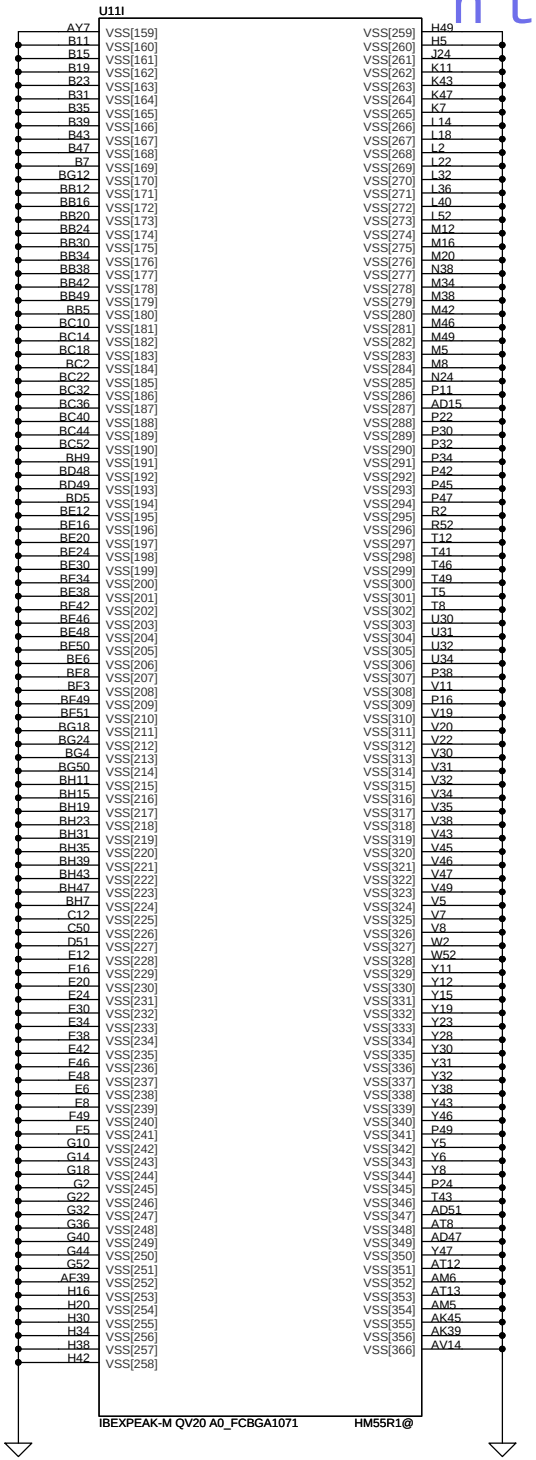

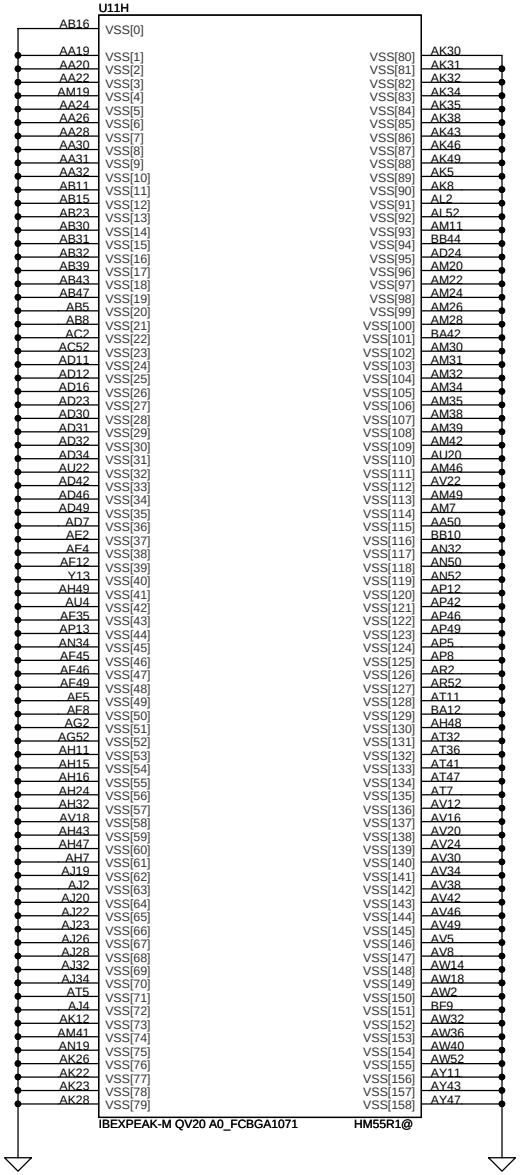

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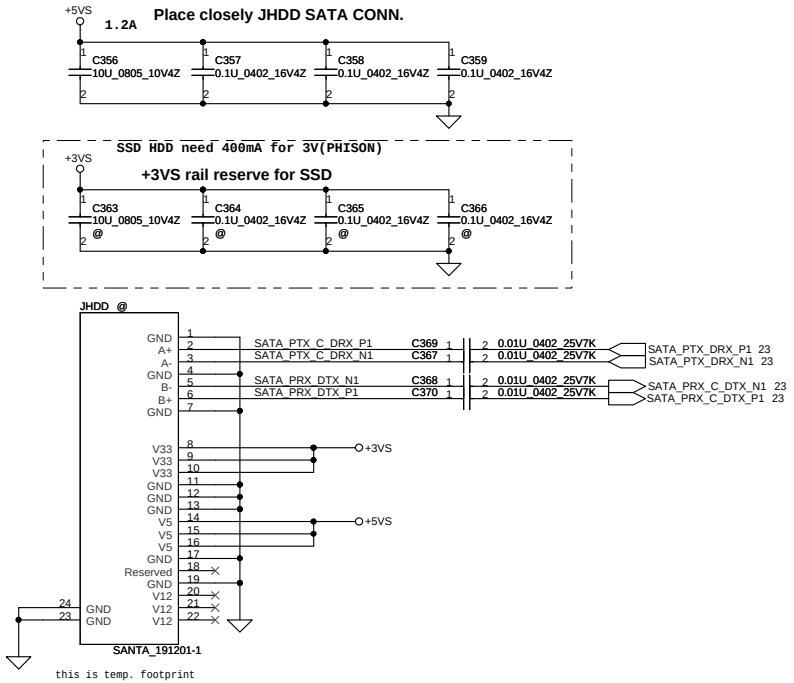
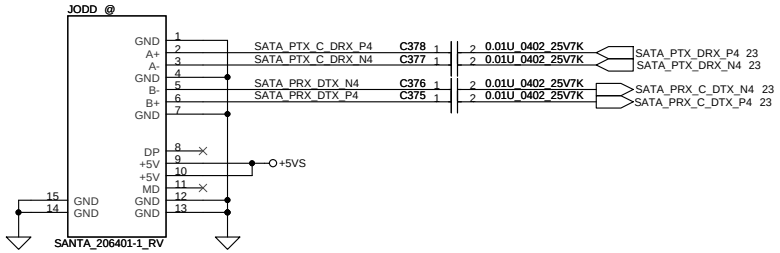
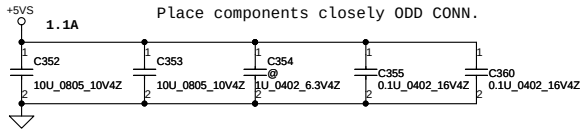
SATA HDD Conn.

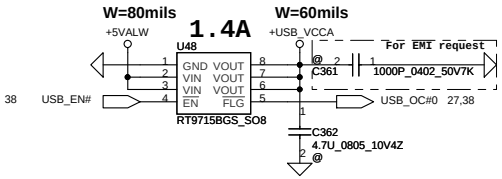


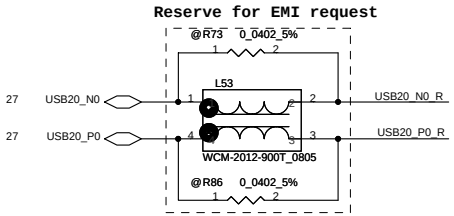
SATA ODD Conn

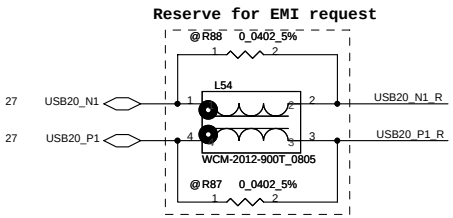


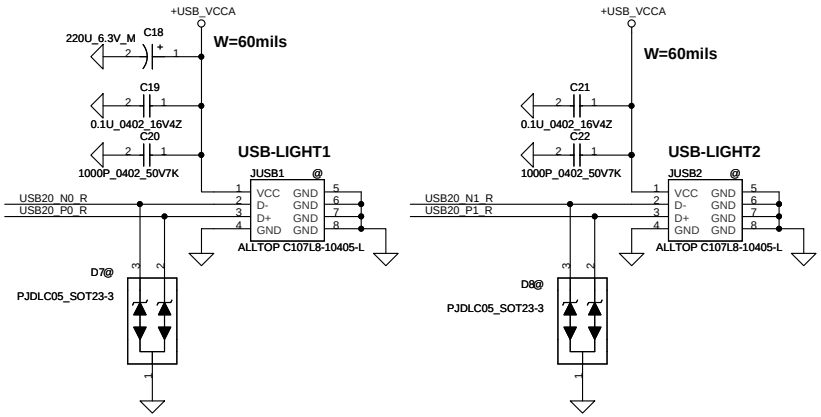


USB Conn. (2 Port)









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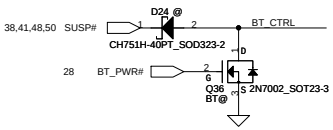
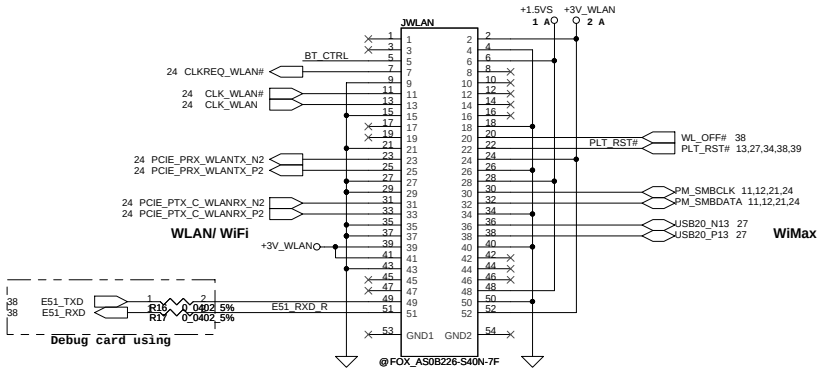
PCIe Mini Card-WLAN/WiMax

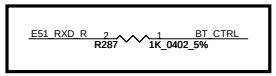
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

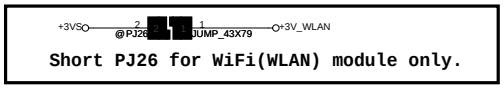
**If +3V_WLAN is +3VS, please remove D24.

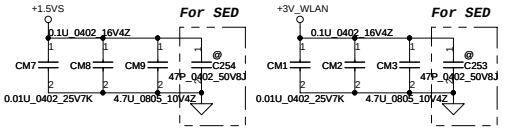






Slot#1 Half PCIe Mini Card-WLAN/WiMax





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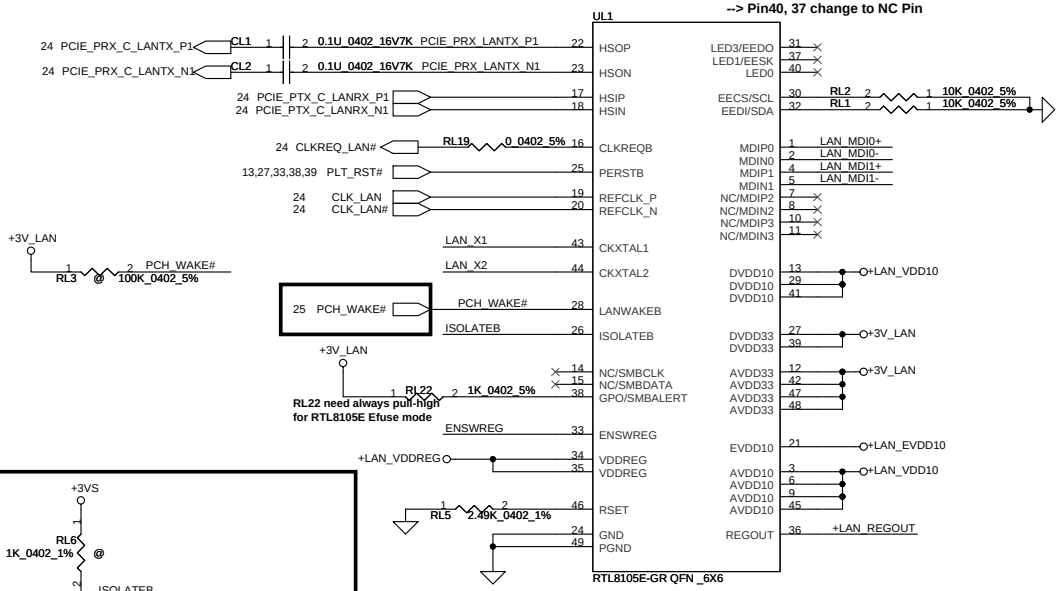
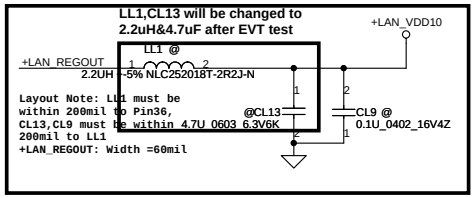
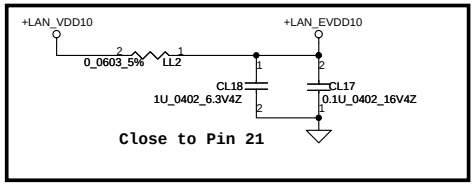
3/19 --> Change JLAN for don't support LAN LED fuction
--> Pin40, 37 change to NC Pin

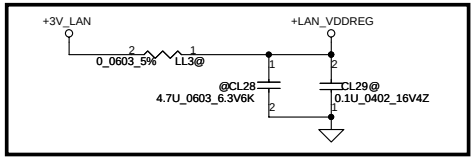


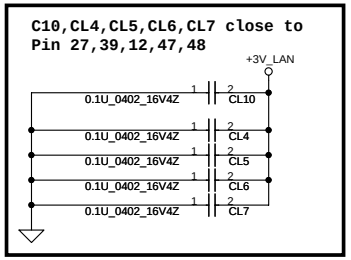
0715 --> change P/N to SA00003PO20 (RTL8105E-VC)

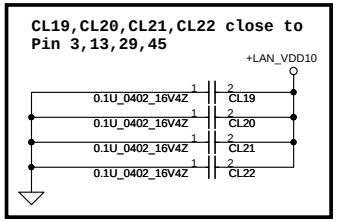
0715 --> LL1, CL13, CL9, LL3, CL28,
CL29 are unmount for RTL8105E-VC

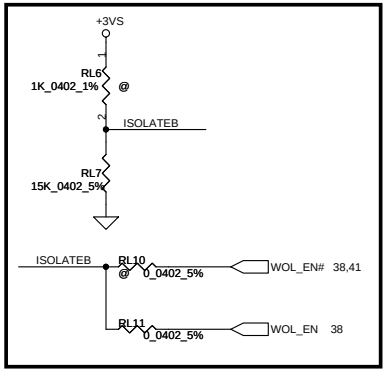




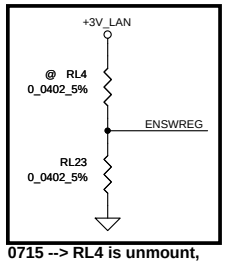






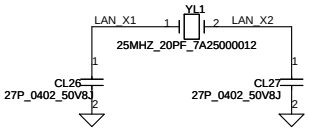


Add RL10 for +3V_LAN power enable signal
Add RL11 for wake on LAN function enable signal

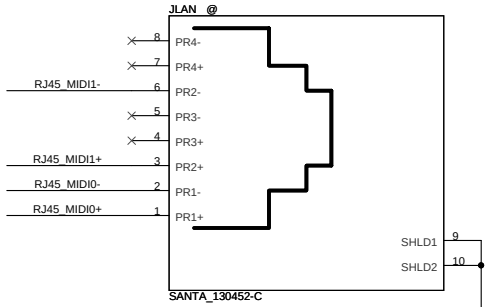


0715 --> RL4 is unmount,
RL23 mount for
RTL8105E-VC

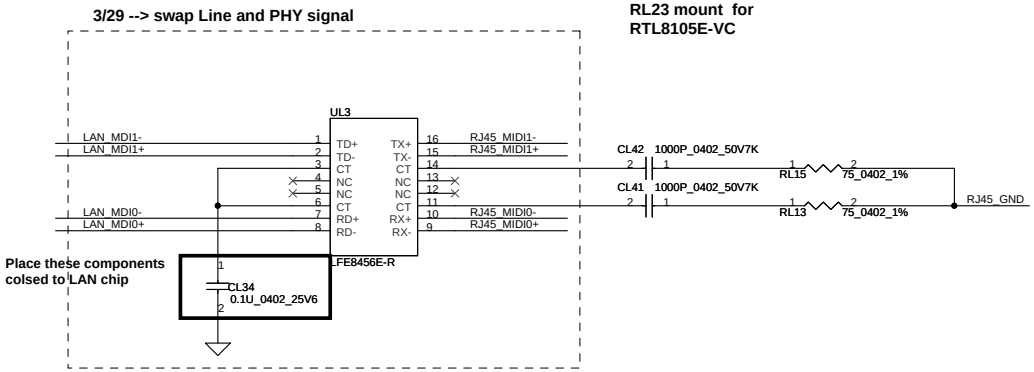
4/2->remove RL8, RL9, CL11



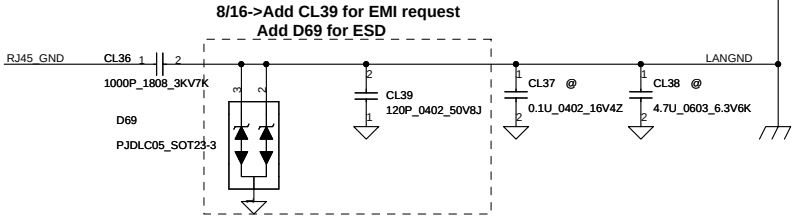
LAN Conn.



3/29 --> swap Line and PHY signal



8/16->Add CL39 for EMI request
Add D69 for ESD



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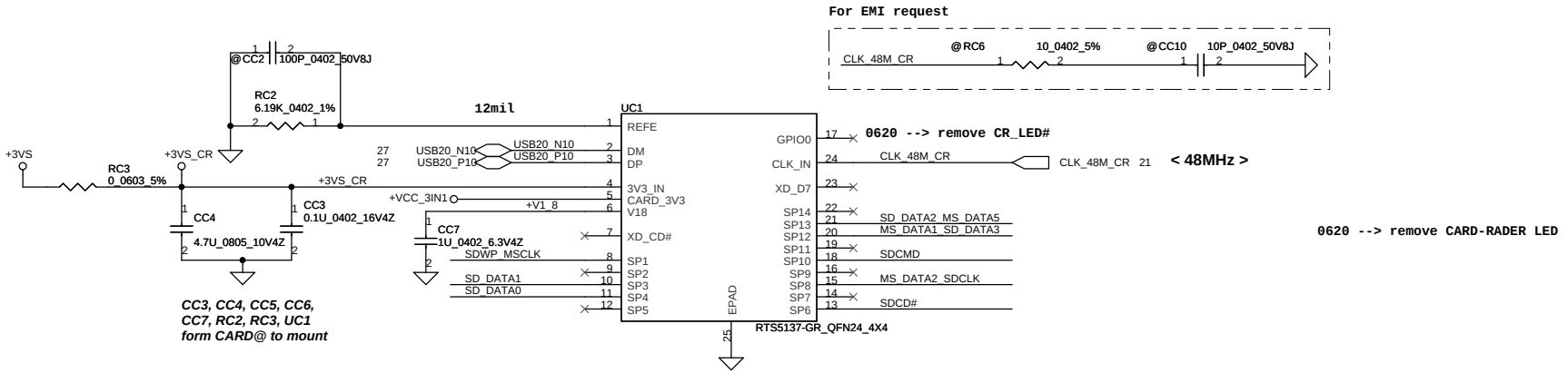
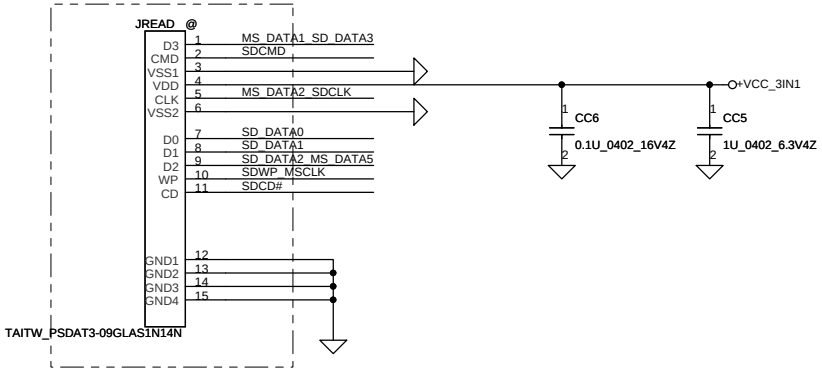


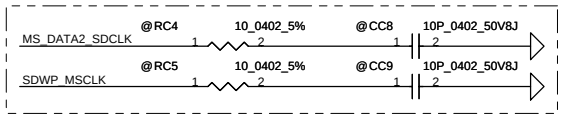
0715 --> change P/N to RTS5137 (SA000043500)

< 2 in 1 Card Reader >

0624 --> change CARDREADER conn.



For EMI request



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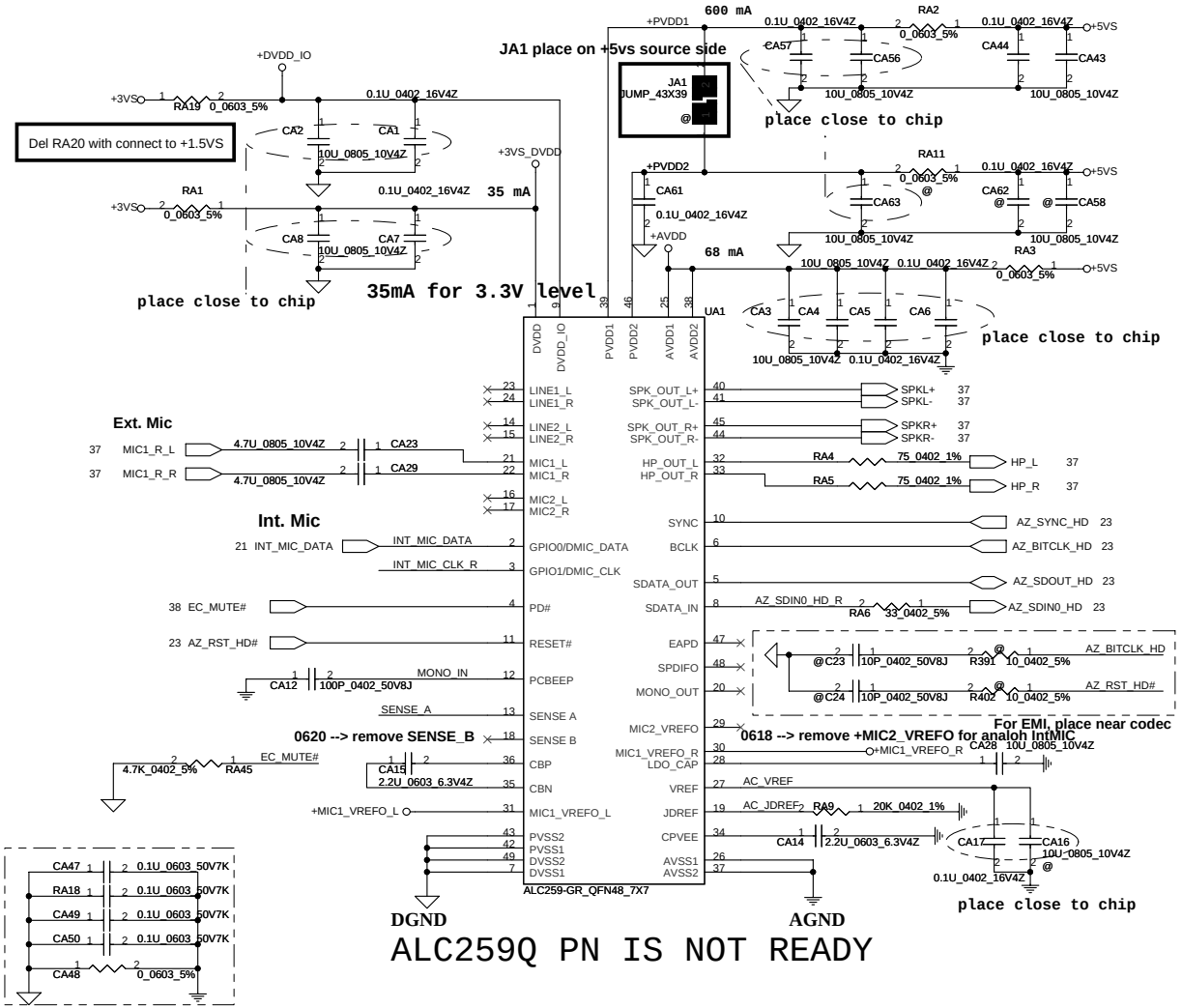
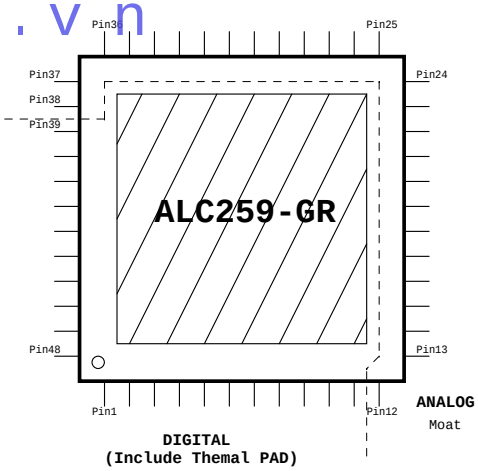
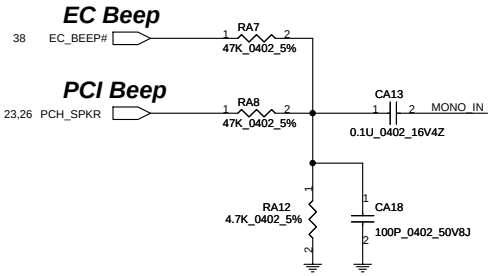
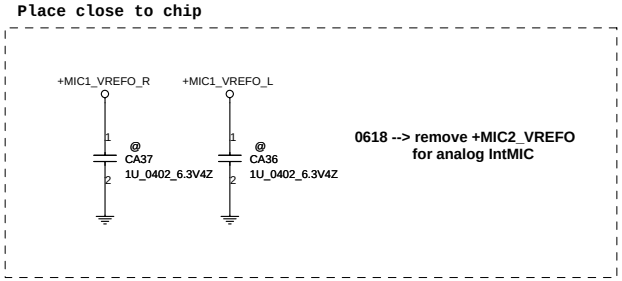
Codec

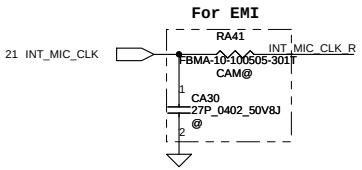




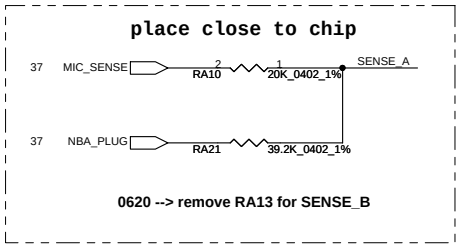
Beep sound







Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



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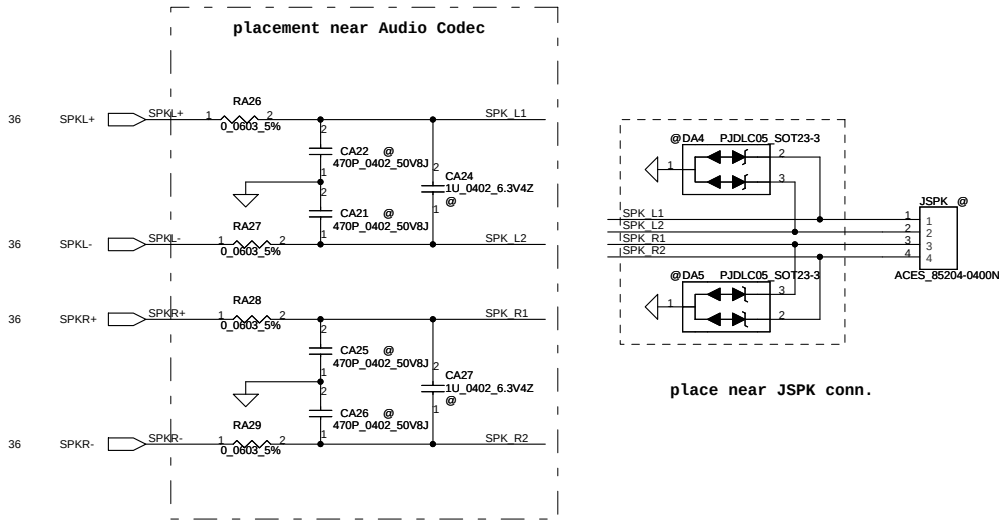
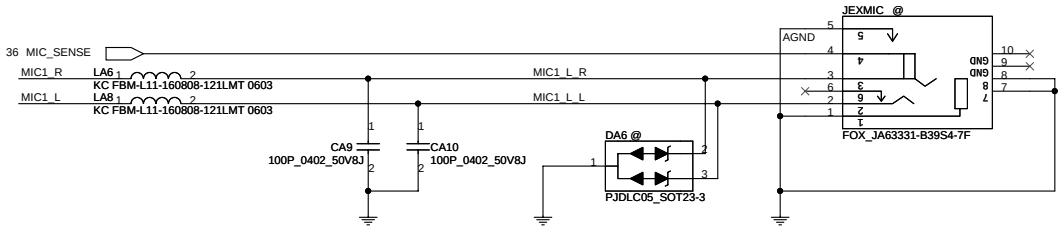
Speaker Connector

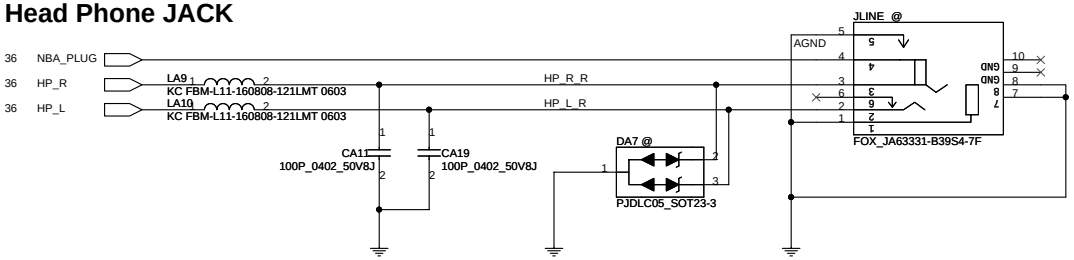


place near JSPK conn.

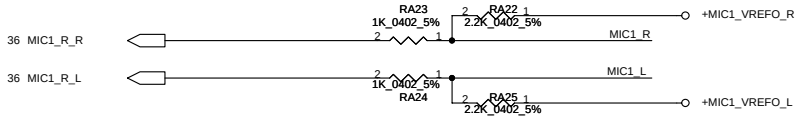
Ex.MIC JACK



Head Phone JACK



Ext.MIC/LINE IN



Int. Mic

0618 --> remove Analog IntMIC, and change to DIGITAL MIC

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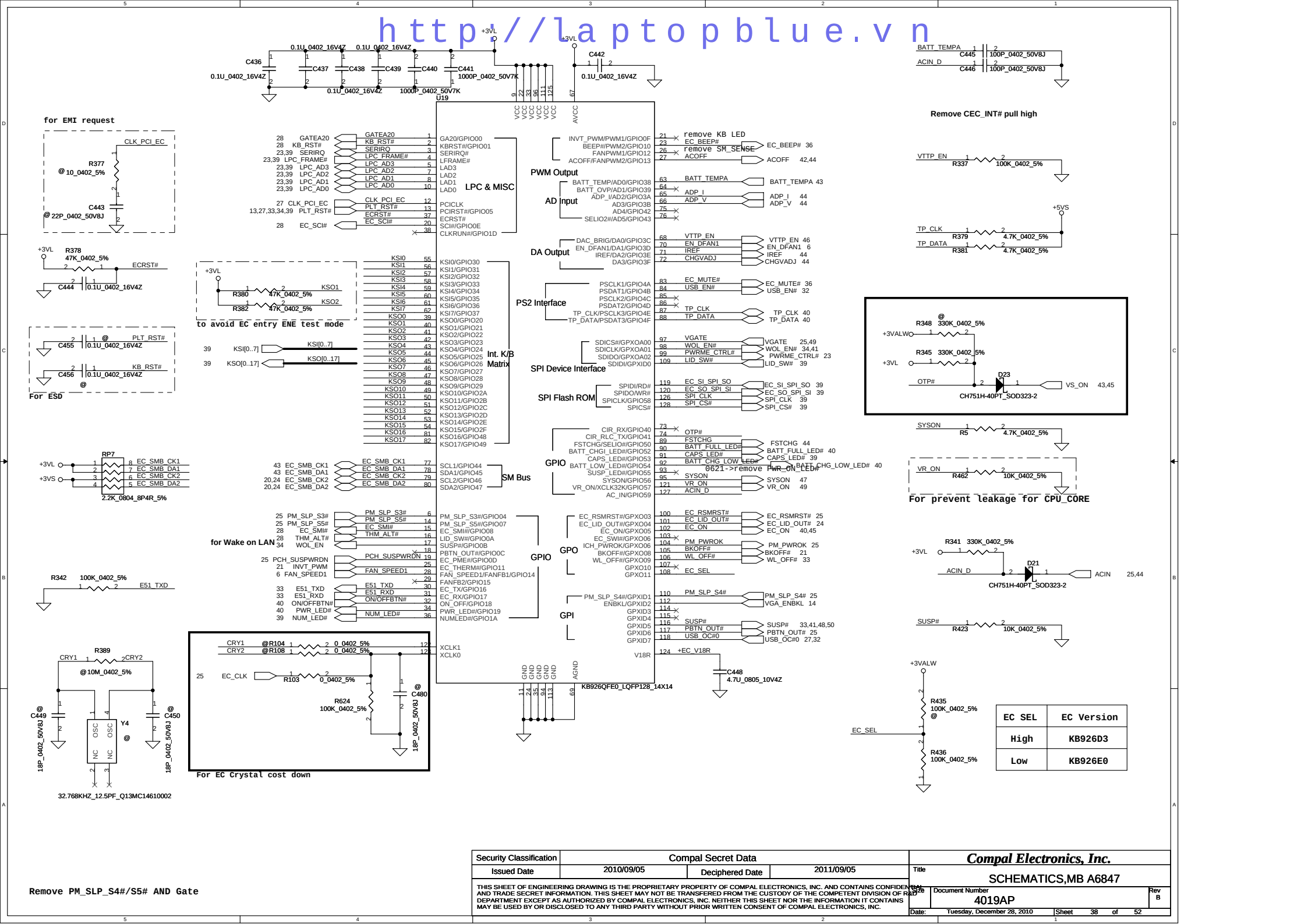

EC SEL	EC Version
High	KB926D3
Low	KB926E0

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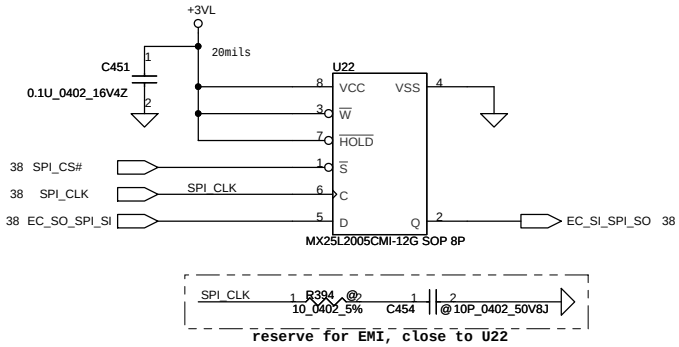
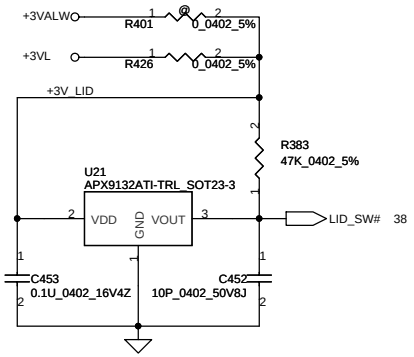
SPI Flash (256KB)

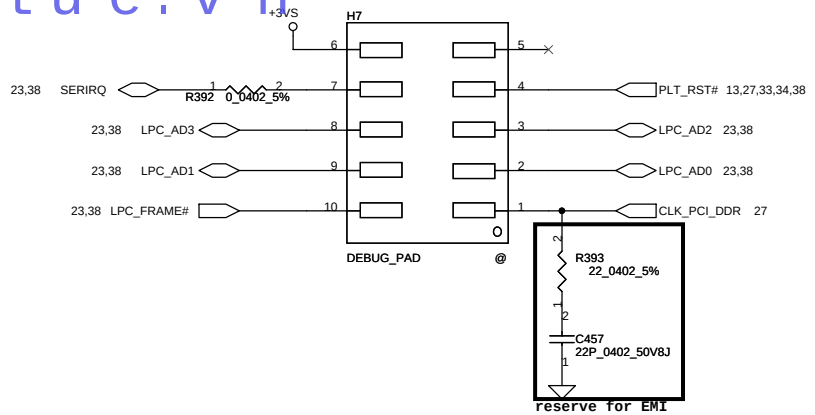


Lid SW



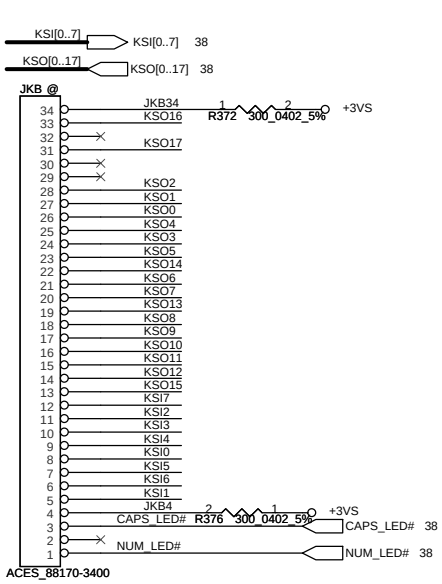
LPC Debug Port

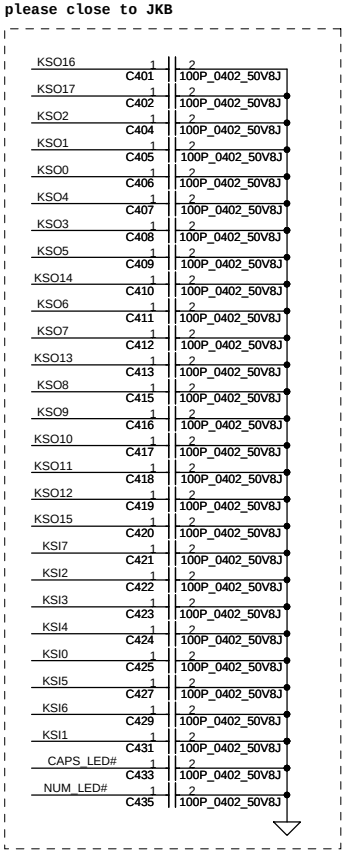
Please place the PAD under DDR DIMM.



KEYBOARD CONN.

Noticed: KB Connector Pin Definition Reversed with KB Membrane Pin Definition





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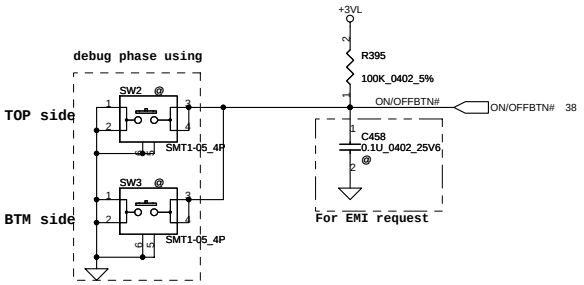
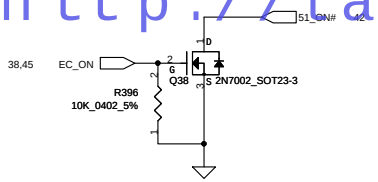
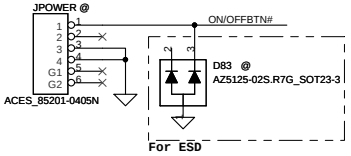
Power Button

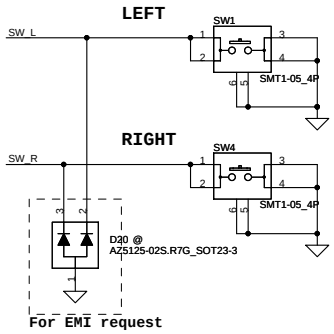


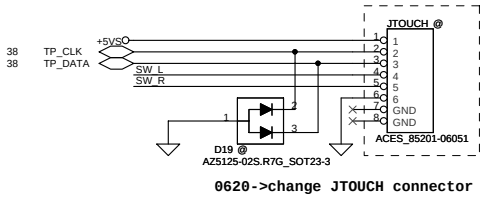


PWR/B to MB Conn.



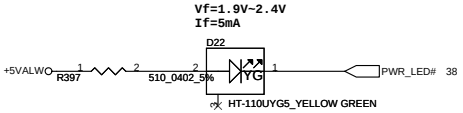
TP Button/Conn.





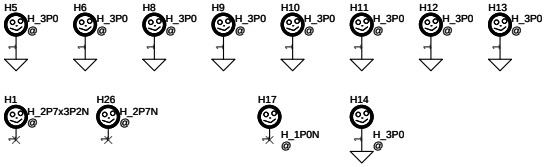
0620->change JTOUCH connector

POWER/SUSPEND LED



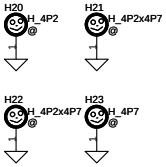
BATT CHARGE/FULL LED

Screw Hole

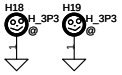


VGA

CPU



MINI CARD



SB

For Codec AGND
Dummy
3G
MDC

PCB Fedical Mark PAD

ISPD

PCB — ZZZ — PCB LA-6847P REV1

DC-IN — PJP1 — PJP1 45@

PCH — U11 — PCH HM55R3@

GPU — UV1 — GPU PARKR3@

UV1 — GPU ROBSONR3@

UV1 — GPU ROBSONR1@

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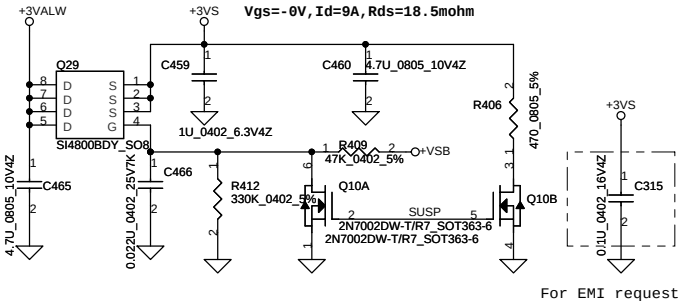
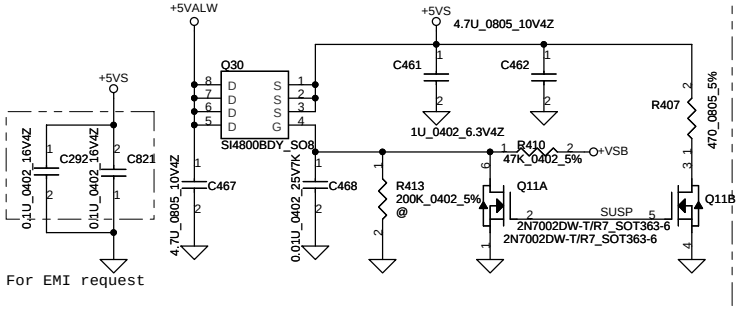
+3VALW TO +3VS

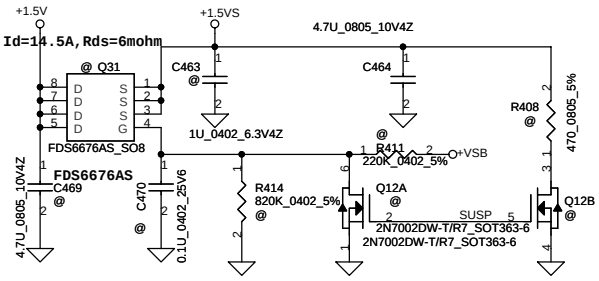


+5VALW TO +5VS



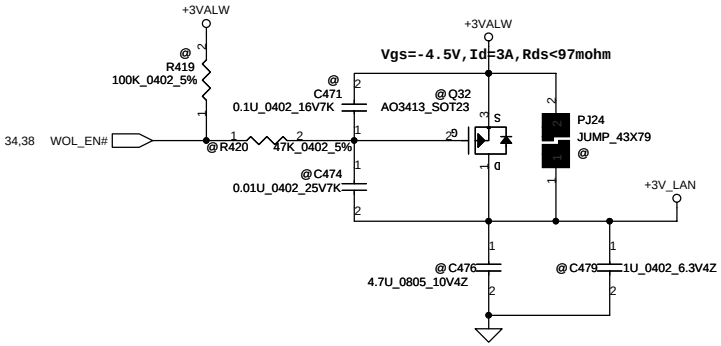
+1.5V to +1.5VS

Combine with +1.5V_CPU

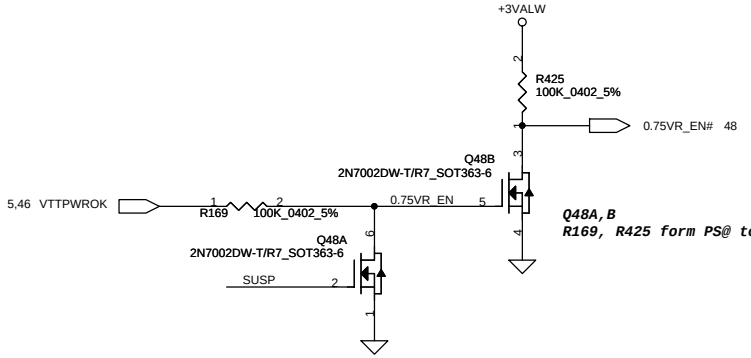


0715 --> Q31 change to SB548000310 the same as +5VS

+3VALW TO +3V_LAN

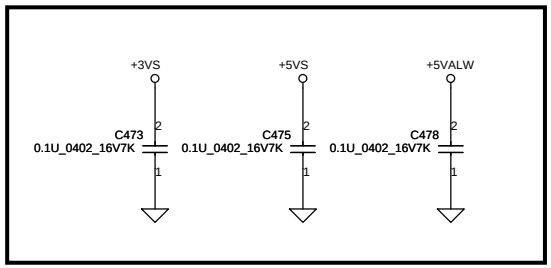


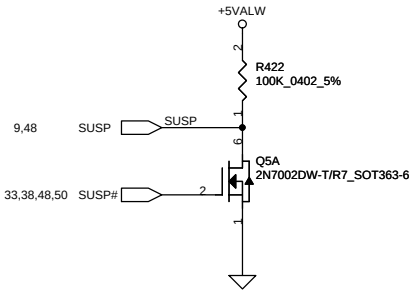
For S3 CPU Power Saving

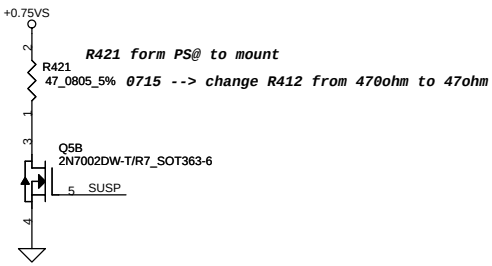


Q48A,B
R169, R425 form PS@ to mount

Reserve for EMI test







R421 form PS@ to mount
0715 --> change R412 from 470ohm to 47ohm

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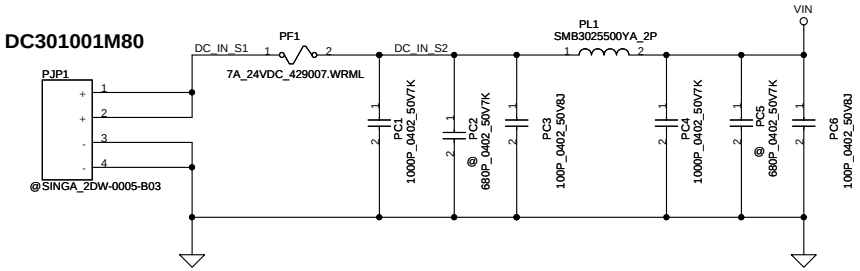
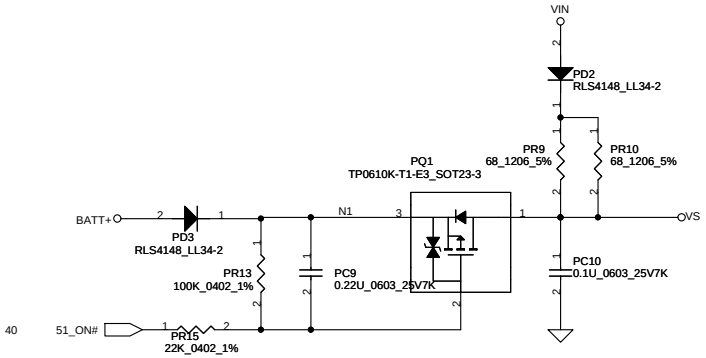
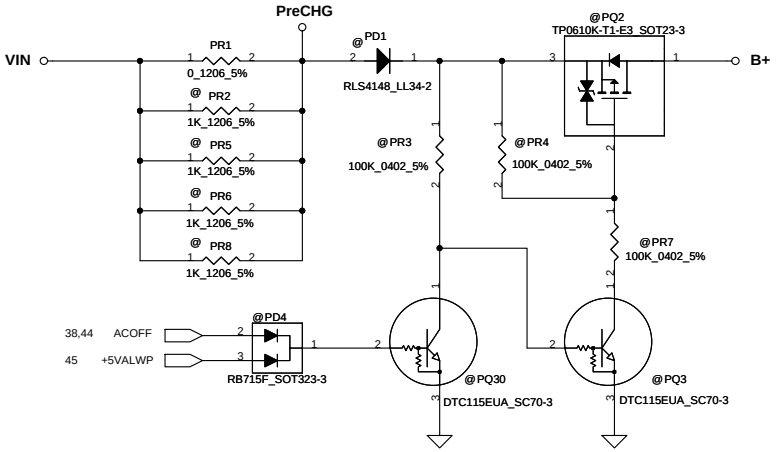
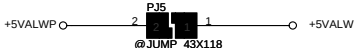






(5A,200mils ,Via NO.= 10)

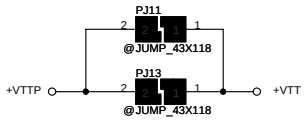
OCP(min)=7.7A



(5A,200mils ,Via NO.= 10)

OCP(min)=7.9A

(120mA,40mils ,Via NO.= 1)

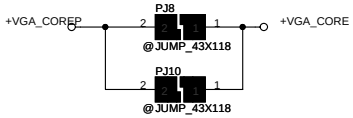


(20A,800mils ,Via NO.=40)

OCP(min)=22.9A

(14A,360mils ,Via NO.= 18)

OCP(min)=16.57A



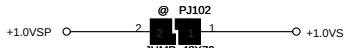
(20A,880mils ,Via NO.=44)

OCP(min)=24.49A

(1.5A,60mils ,Via NO.= 4)

(2A,80mils ,Via NO.= 4)

(100mA,40mils ,Via NO.= 2)



(1A,40mils ,Via NO.= 2)

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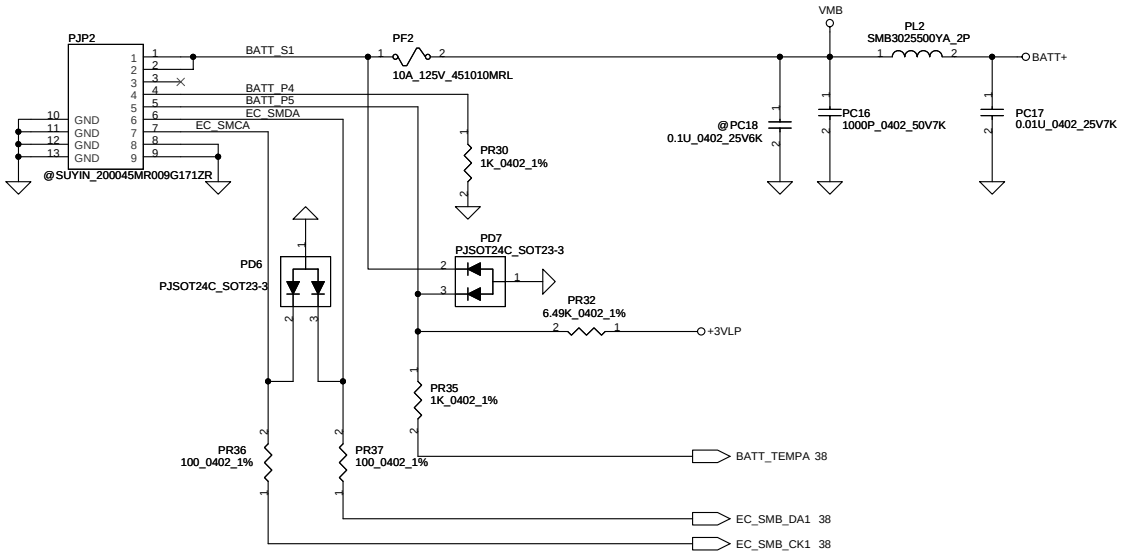
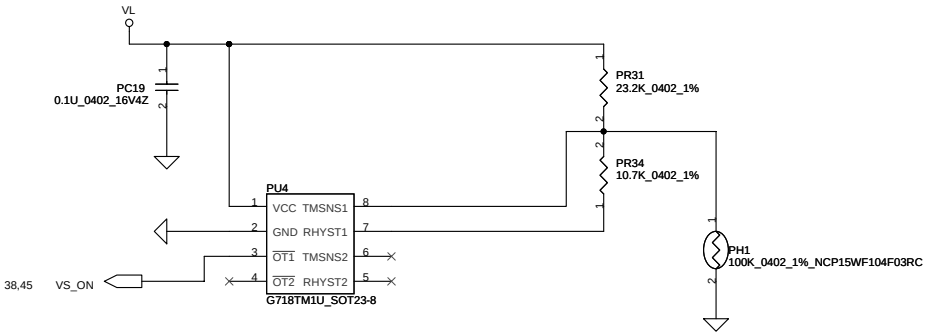
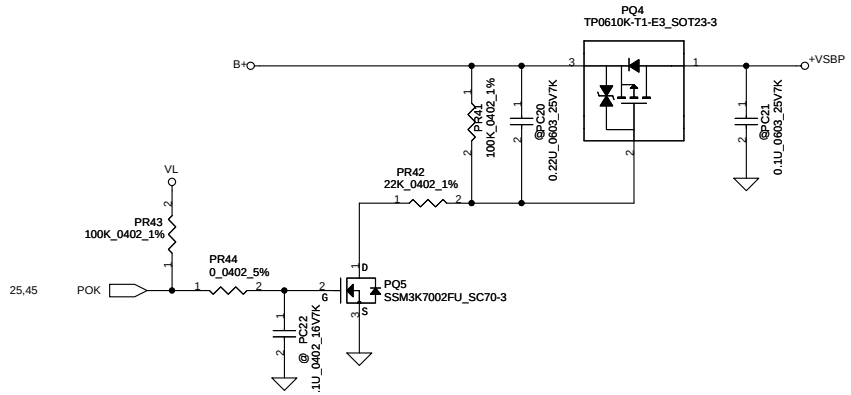


PH1 under CPU botten side :
CPU thermal protection at 90degree C
Recovery at 56 degree C





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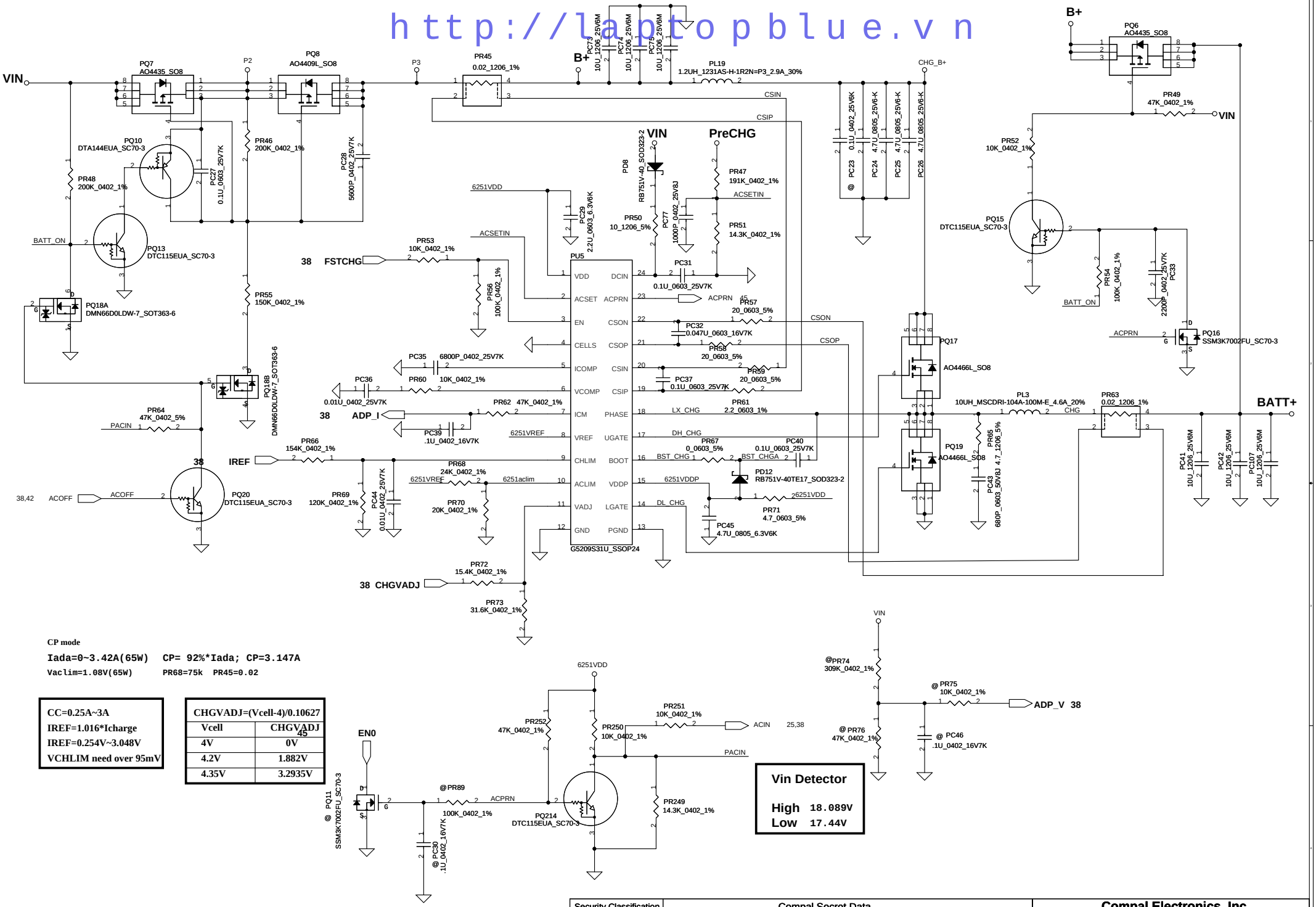

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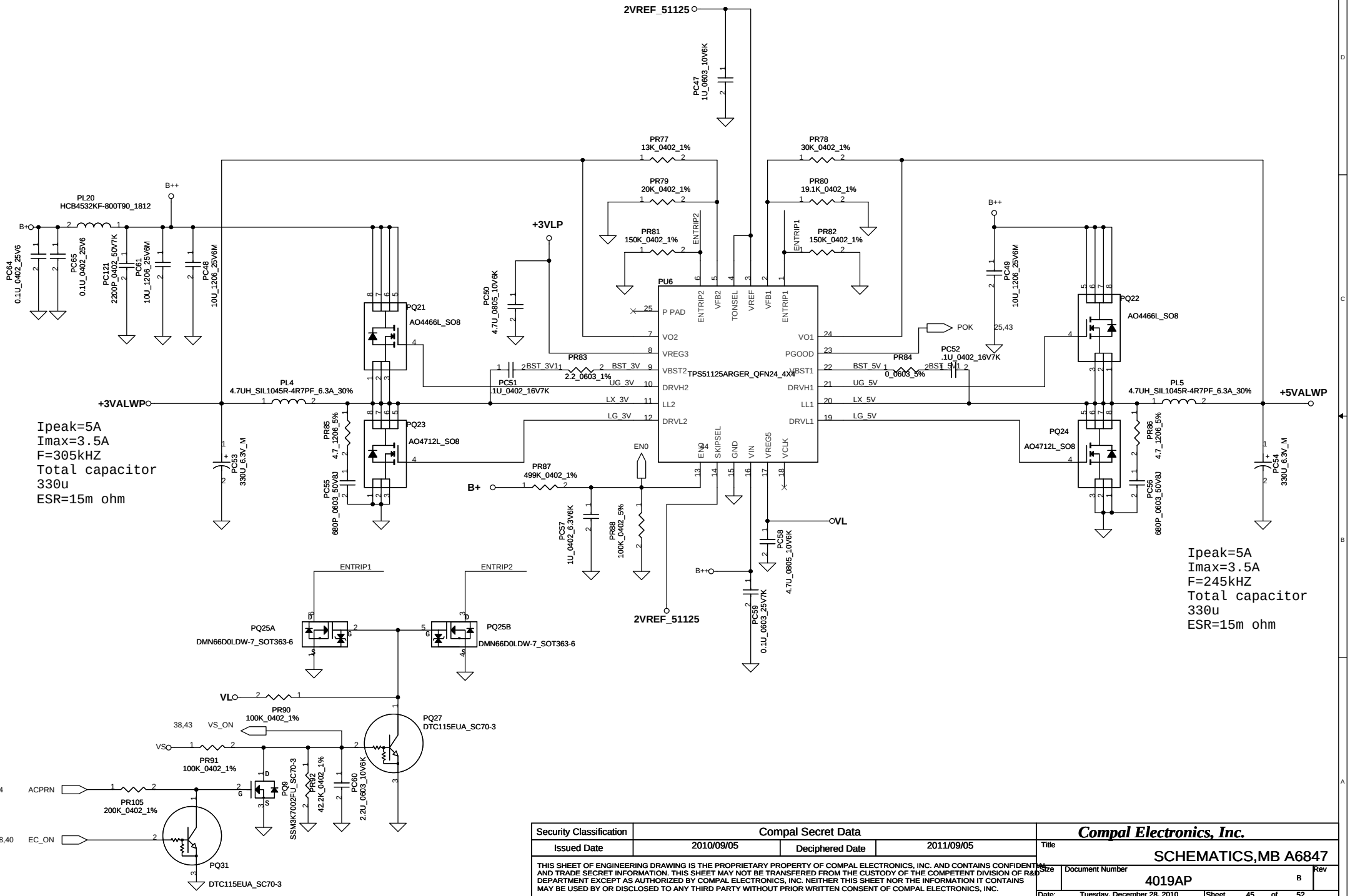

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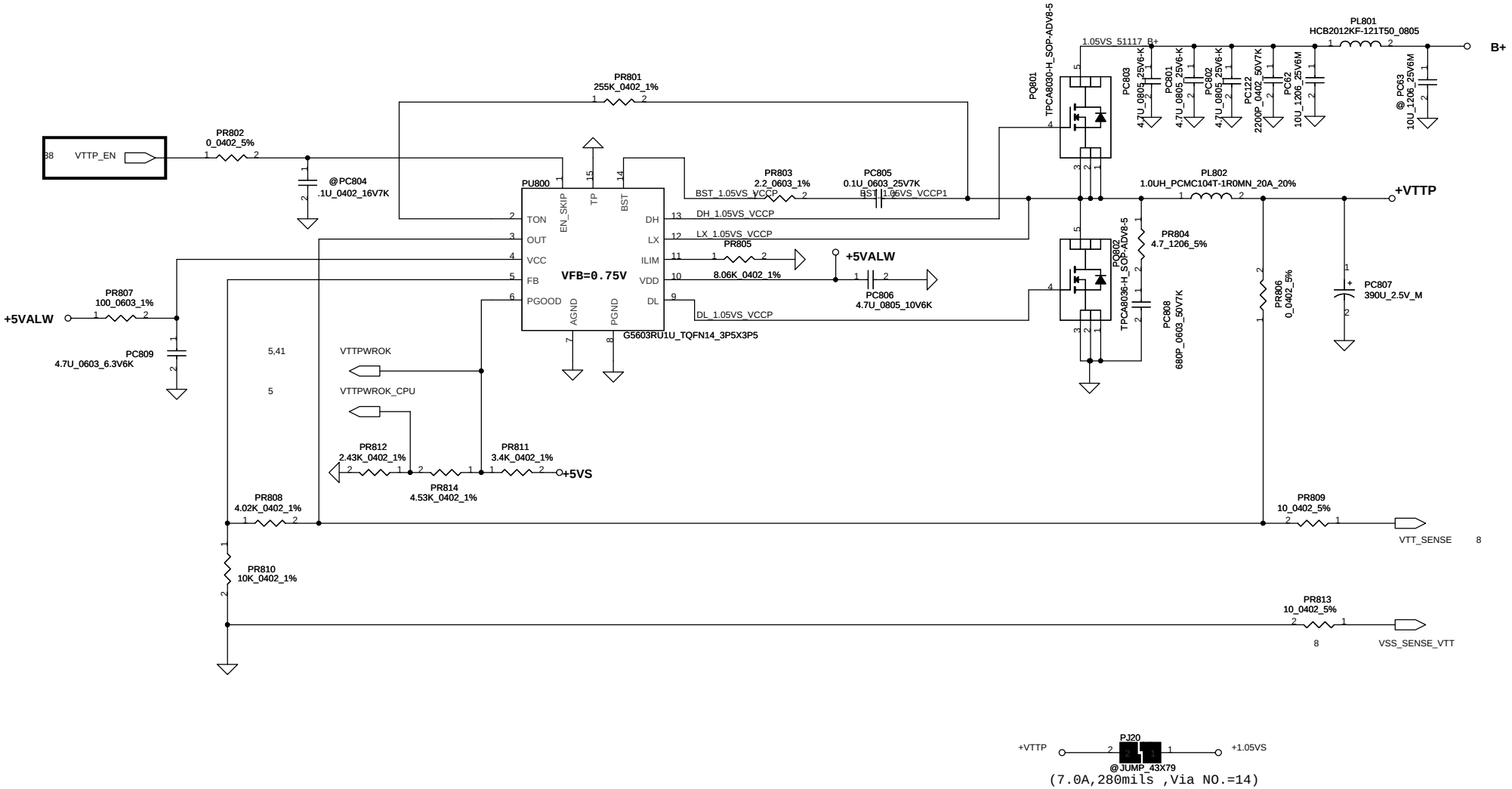

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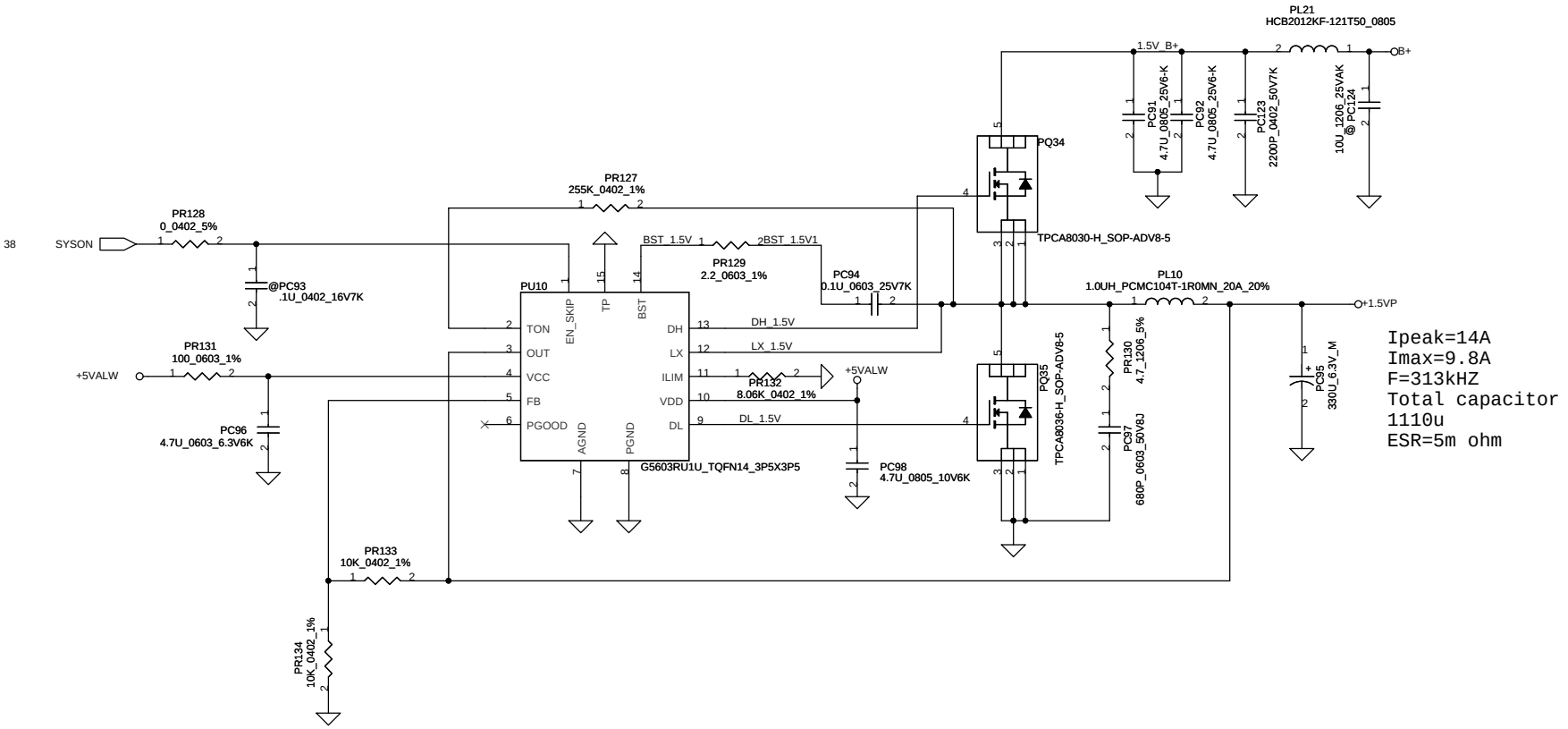

Ipeak=14A
Imax=9.8A
F=313kHZ
Total capacitor
1110u
ESR=5m ohm

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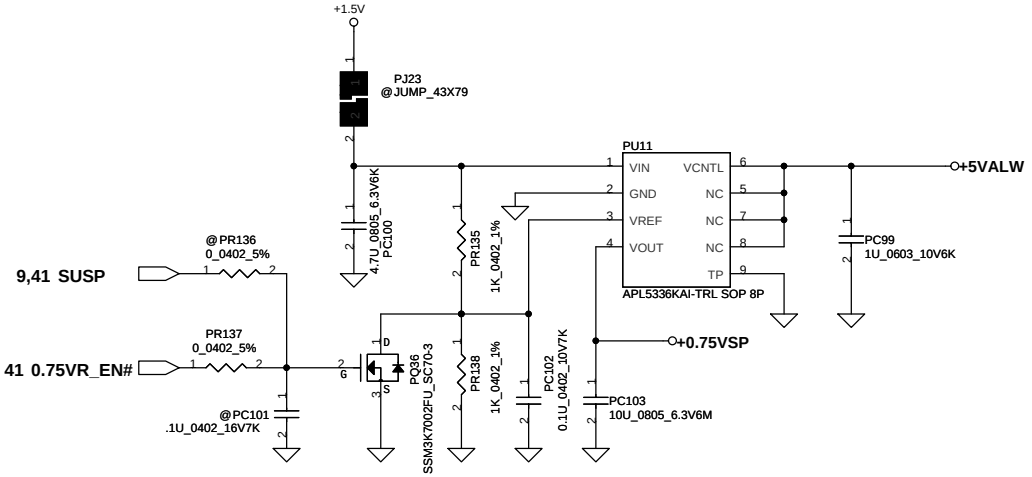

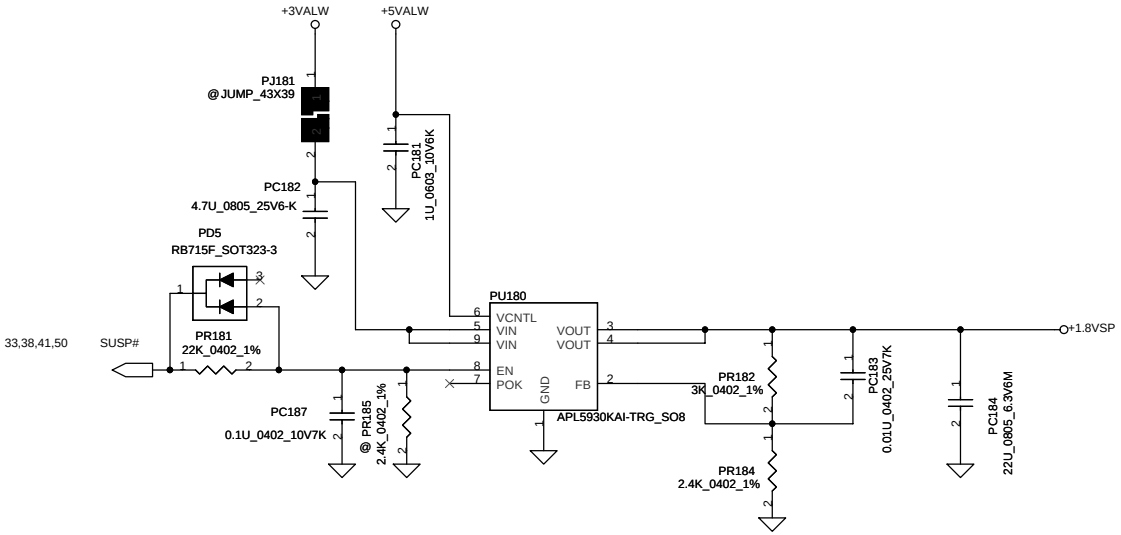

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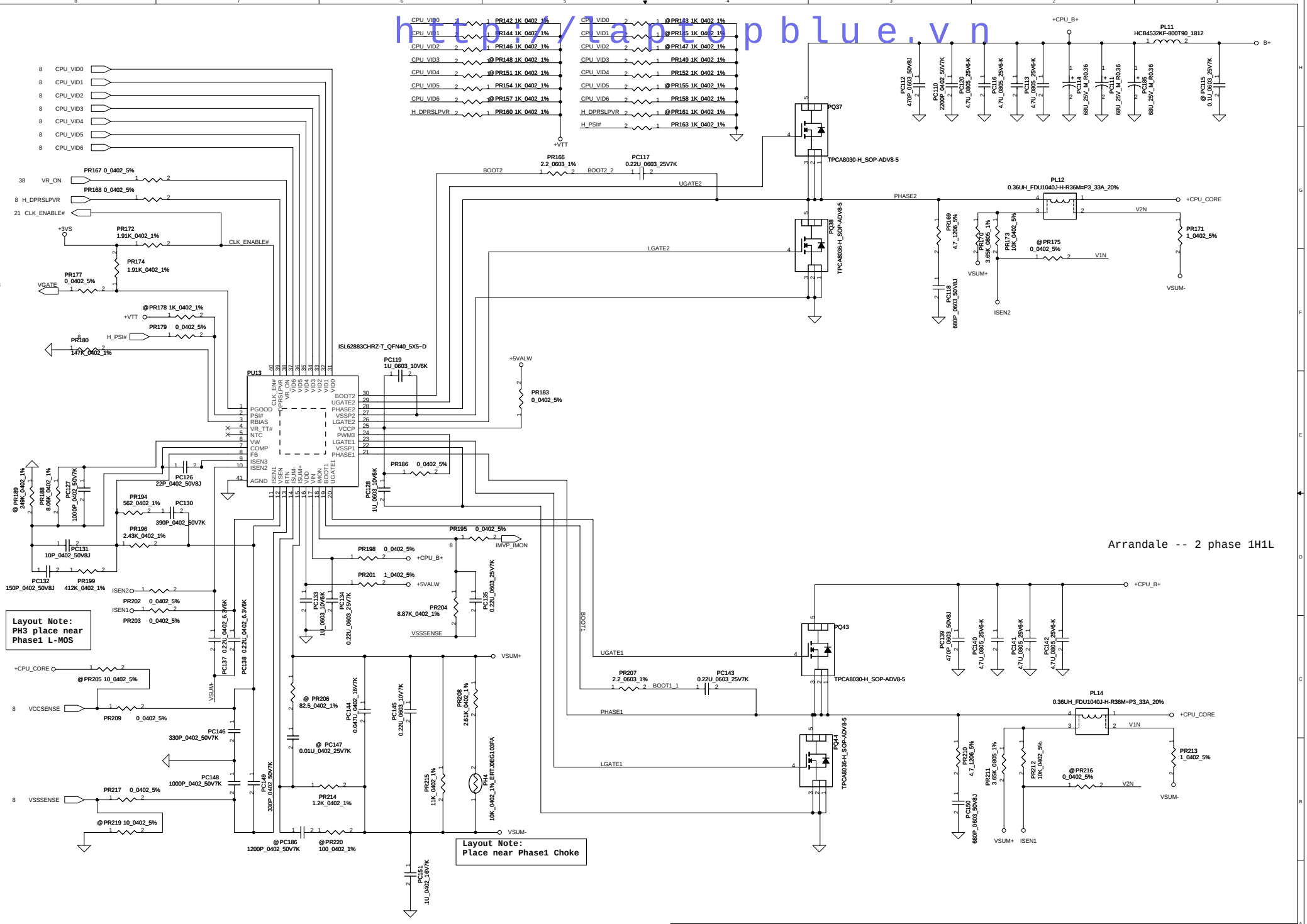

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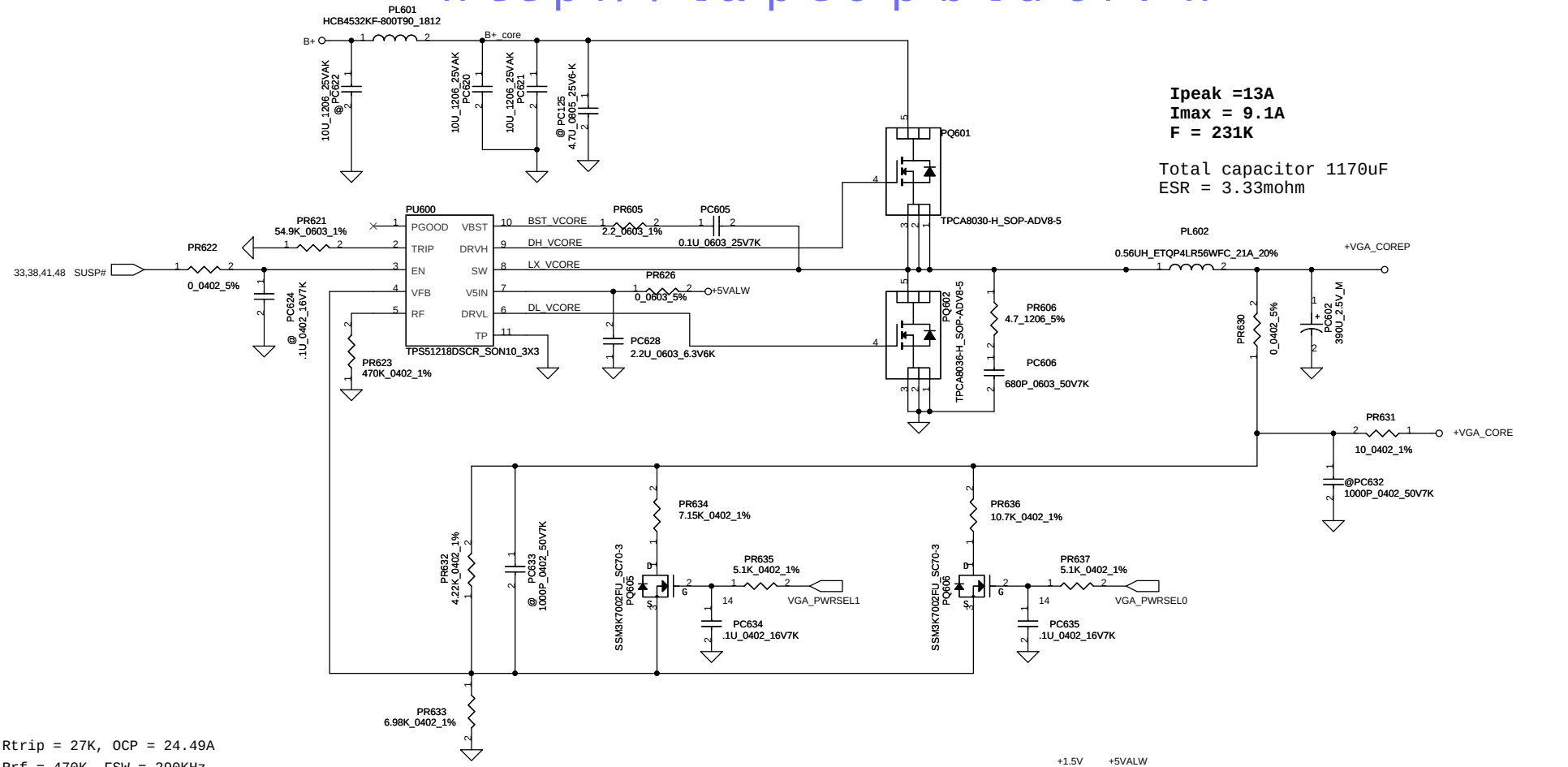


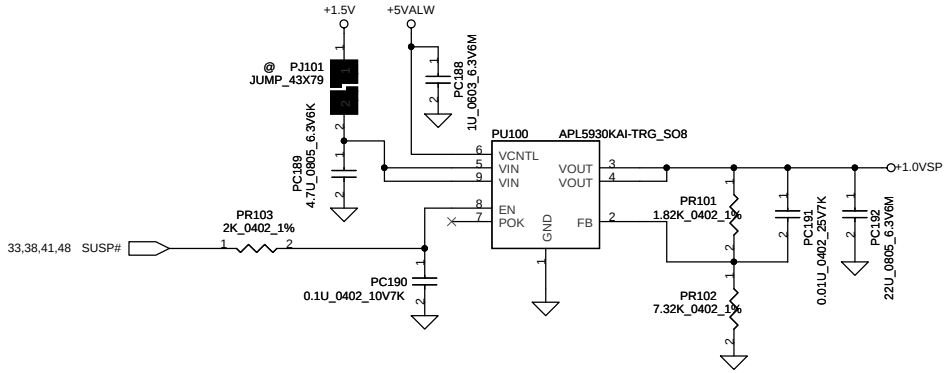
Ipeak =13A
Imax = 9.1A
F = 231K

Total capacitor 1170uF
ESR = 3.33mohm

Rtrip = 27K, OCP = 24.49A
Rrf = 470K, FSW = 290KHz

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

SEL1	SEL0	Robson LP	Park XT
L	L		1.12
L	H		
H	L	0.95	
H	H	0.9	0.9



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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2010/10/14	42	Remove PR2,PR3,PR4,PR5,PR6,PR7,PR8,PD1,PD4,PQ2,PQ3,PQ30 Change PR1 to 0_1206_5%	Remove Pre charge
	2010/10/14	44	Change PQ8 to AO4409L,remove PR89,PC30,PQ11 Change PR68 to 24K ohm,add PC107	Remove Pre charge Circuit modify
	2010/10/14	45	Change PU6 to TPS51125A	Circuit modify
	2010/10/14	46	Change PQ802 to TPCA8036	Circuit modify
	2010/10/14	48	Change PU11 to APL5336,PR181 to 15K ohm, add PC187(0.22U)	Circuit modify
	2010/10/14	50	Change PR621 to 54.9k ohm,Delete PR104,PC622 Add PR606,PC606	Circuit modify
	2010/10/21	45	Add PC64(0.1U_0402_25V)	EMI request
	2010/10/21	48	Change PR181 to 22k ohm,PC187 to 0.1UF,add PD5	HW request
	2010/10/21	50	Change PR605 to 2.2 ohm,PR635,PR637 to 5.1Kohm,PR103 to 2Kohm Add PC190	HW request

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PIR (Product Improve Record)

PWWAA LA-6847P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

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