

Compal confidential

Brazos-Delhi 10AB

PWWBE LA-6849P Schematics Document

Mobile AMD APU ZACATE-FT1 + FCH Hudson-M1

2010-11-22 Rev. 1.0

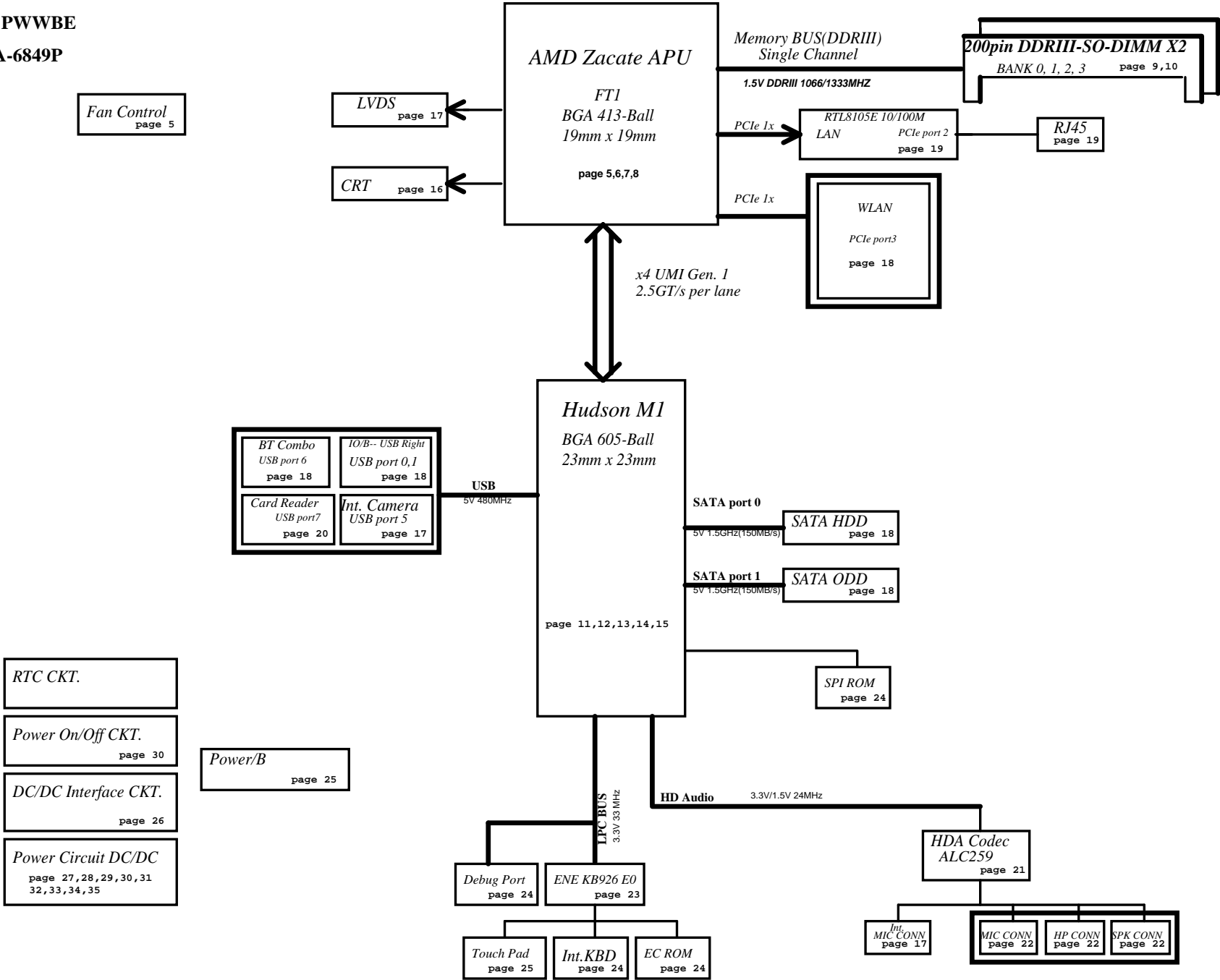
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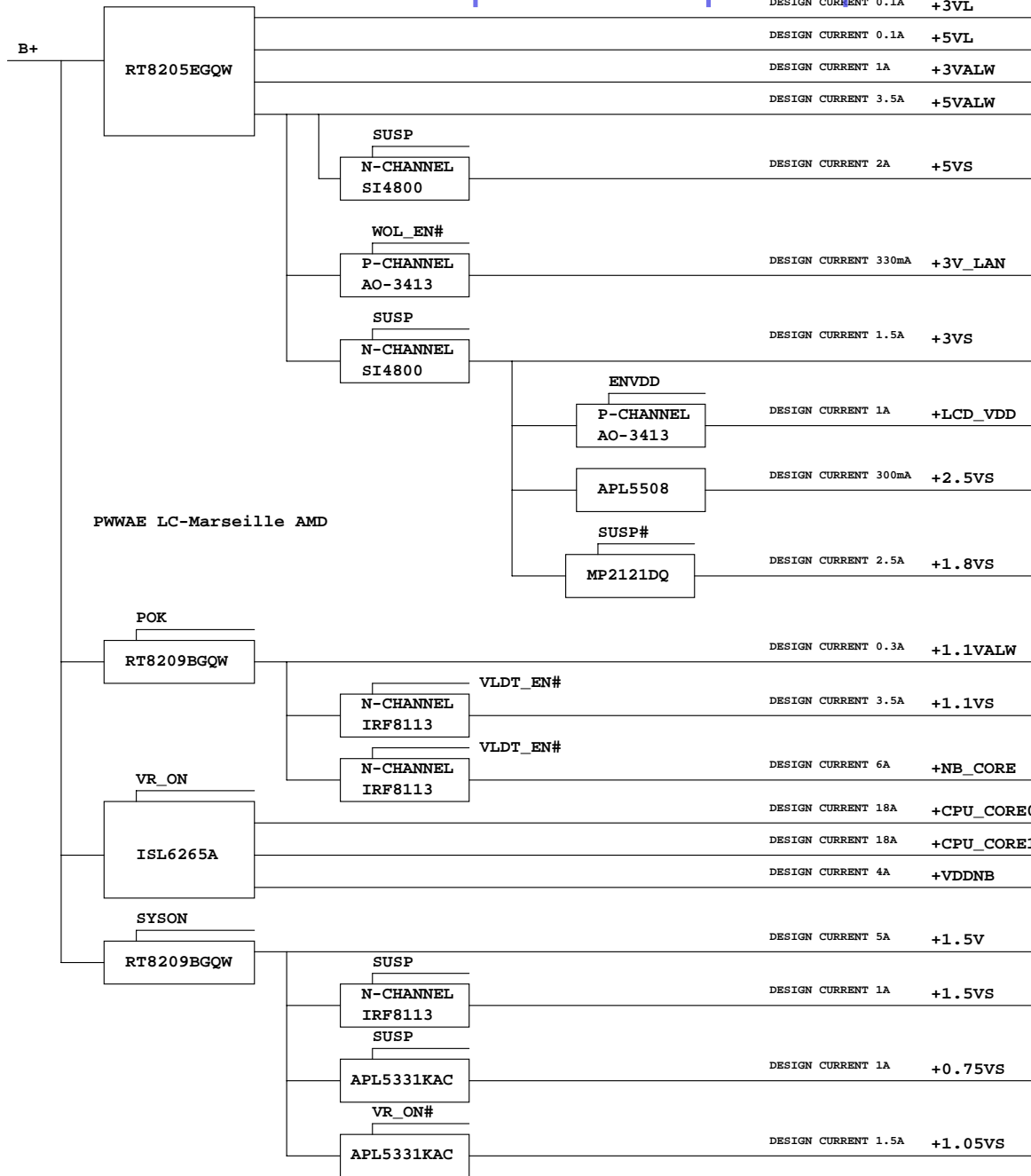
Model Name : PWWBE

File Name : LA-6849P

http://laptopblue.vn



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Voltage Rails

O : ON
X : OFF

power plane State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +AGP_CORE +APU_VDDNB
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

http://laptopblue.vn

Platform	CPU	SB	VGA	EC	Comment
Brazos	APU FT1	FCH M1	NA	KB926	

@ : just reserve , no build
CONN@ : just reserve for Connector only
8105E_VC@: just reserve for 10/100 LAN VC version only
8105E_VB@: just reserve for 10/100 LAN VBversion only
HDT@:just reserve for JHDT connector
E240@ : AMD E240 1.5Ghz CPU only
E350@ : AMD E350 1.6Ghz CPU only

FCH SM Bus0 address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0 A0 H	1010 0000 b	
+3VS	DDR SO-DIMM 1 A4 H	1010 0100 b	

FCH SM Bus1 address

Power	Device	HEX	Address
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EC SM Bus1 address

Power	Device	HEX	Address
+3VL	Smart Battery 16H	0001 011X b	

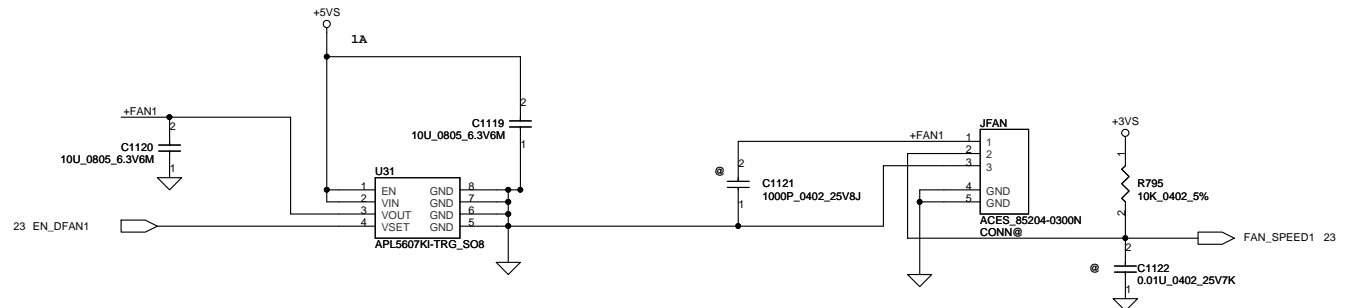
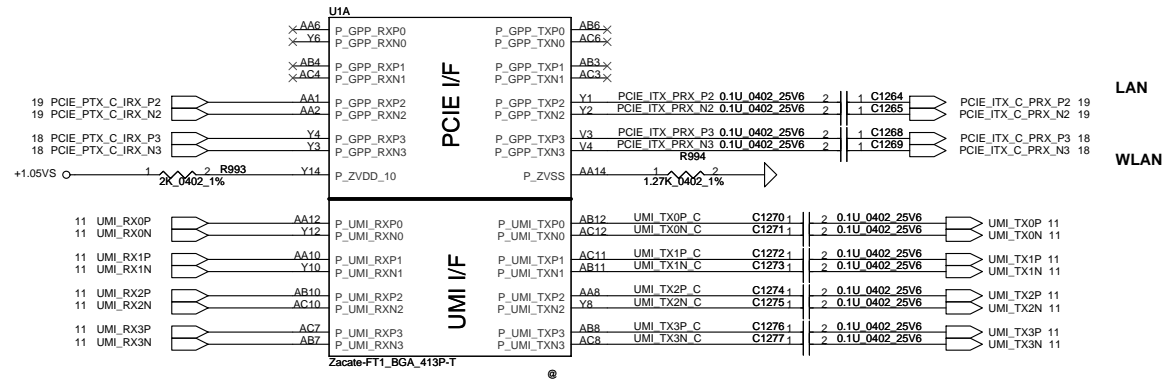
EC SM Bus2 address

Power	Device	HEX	Address
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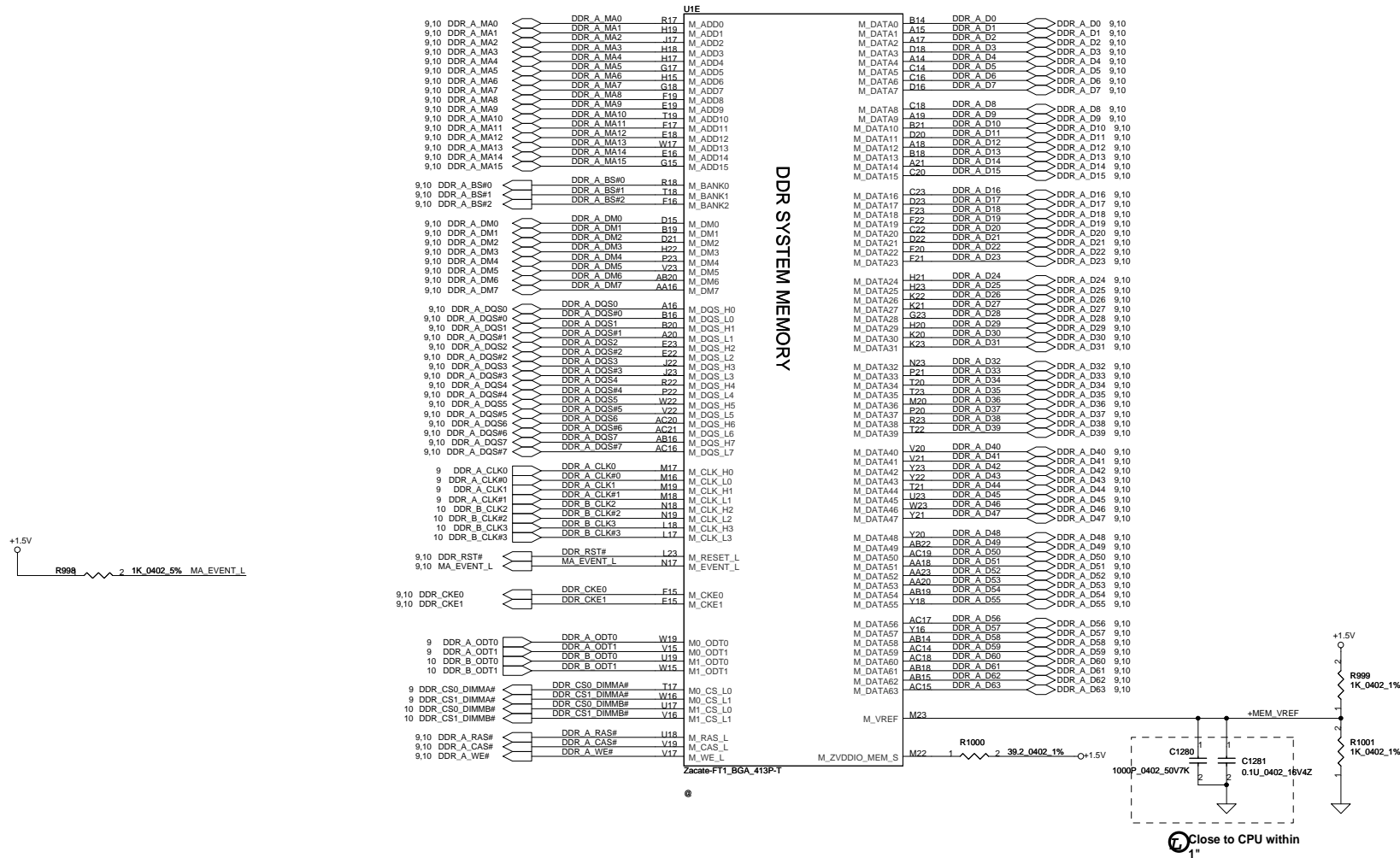
SMBUS Control Table

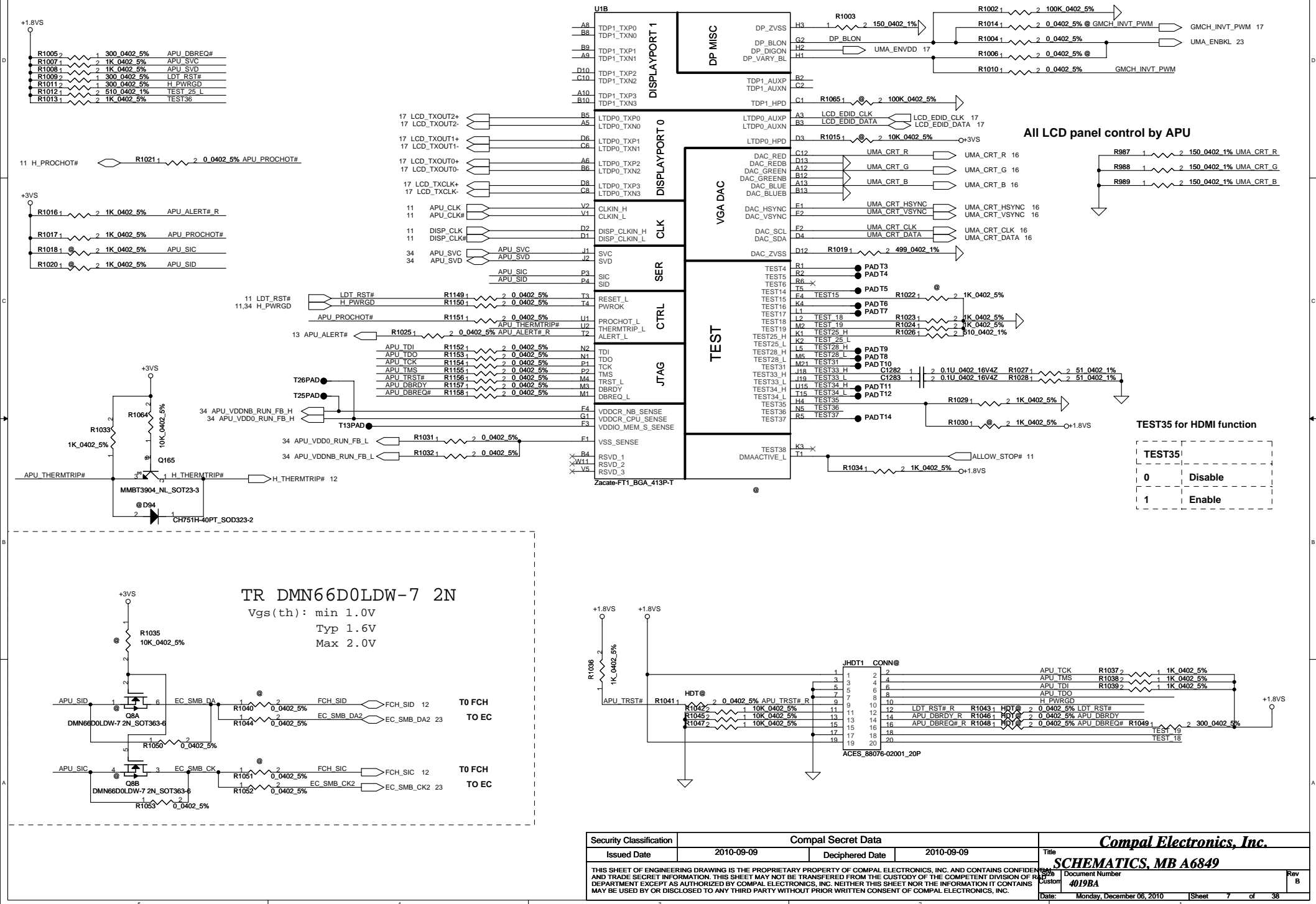
	SOURCE	BATT	SODIMM I / II	CRT DDC ROM	WLAN	LCD DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB926	V					
EC_SMB_CK2 EC_SMB_DA2	KB926						V
LCD_EDID_CLK LCD_EDID_DATA	APU FT1					V	
D_DDCCLK D_DDCDATA	APU FT1			V			
FCH_SMCLK0 FCH_SMDAT0	FCH M1		V				
FCH_SMCLK1 FCH_SMDAT1	FCH M1				V		

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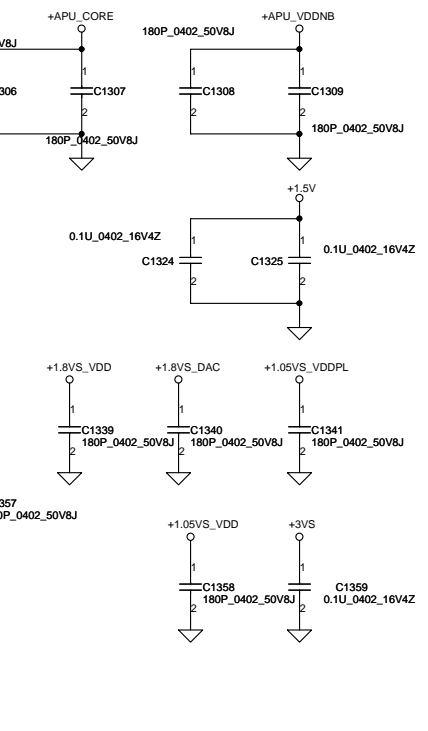


U1D		
A7	VSS_1	VSS_50
B7	VSS_2	VSS_51
B11	VSS_3	VSS_52
B17	VSS_4	VSS_53
B22	VSS_5	VSS_54
C4	VSS_6	VSS_55
D5	VSS_7	VSS_56
D7	VSS_8	VSS_57
D9	VSS_9	VSS_58
D11	VSS_10	VSS_59
D14	VSS_11	VSS_60
D15	VSS_12	VSS_61
D17	VSS_13	VSS_62
D19	VSS_14	VSS_63
E7	VSS_15	VSS_64
E9	VSS_16	VSS_65
F12	VSS_17	VSS_66
F20	VSS_18	VSS_67
F8	VSS_19	VSS_68
F11	VSS_20	VSS_69
F13	VSS_21	VSS_70
G4	VSS_22	VSS_71
G5	VSS_23	VSS_72
G7	VSS_24	VSS_73
G9	VSS_25	VSS_74
G12	VSS_26	VSS_75
G20	VSS_27	VSS_76
G22	VSS_28	VSS_77
G25	VSS_29	VSS_78
H11	VSS_30	VSS_79
H13	VSS_31	VSS_80
J4	VSS_32	VSS_81
J6	VSS_33	VSS_82
J7	VSS_34	VSS_83
J20	VSS_35	VSS_84
K10	VSS_36	VSS_85
K14	VSS_37	VSS_86
L4	VSS_38	VSS_87
L6	VSS_39	VSS_88
L8	VSS_40	VSS_89
L11	VSS_41	VSS_90
L13	VSS_42	VSS_91
L20	VSS_43	VSS_92
L22	VSS_44	VSS_93
M7	VSS_45	VSS_94
N4	VSS_46	VSS_95
N6	VSS_47	VSS_96
N8	VSS_48	VSS_97
N11	VSS_49	VSS_98

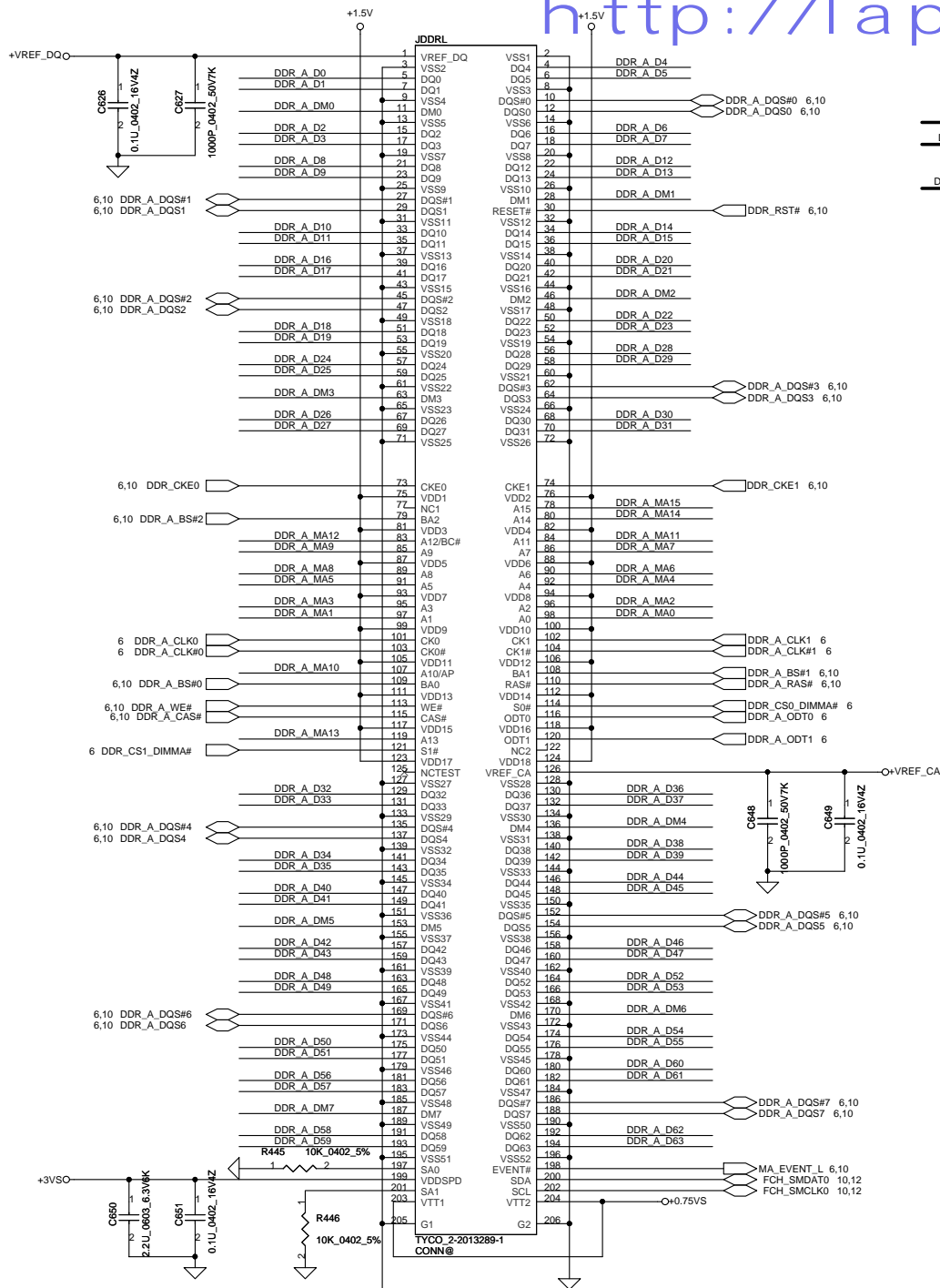
GND

VSSBC_DAC

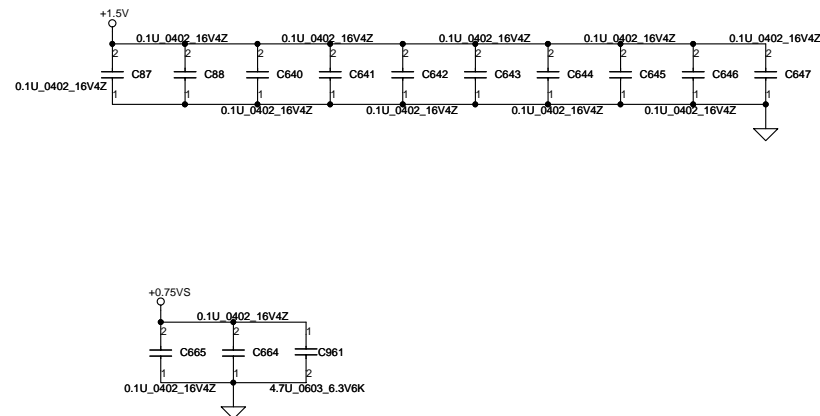
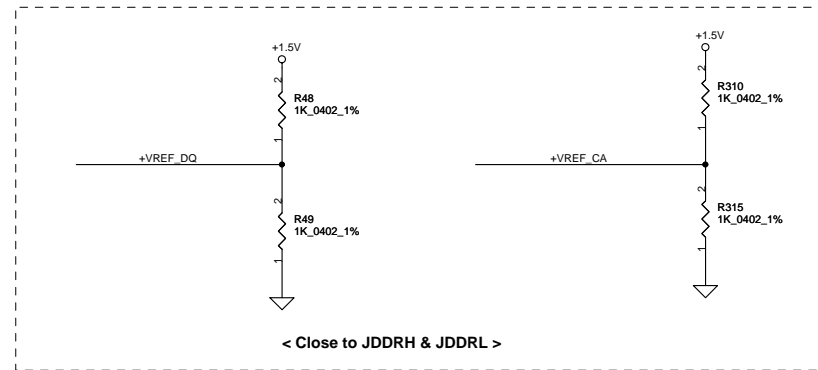
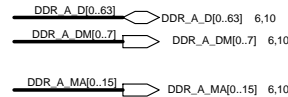
Zacate-FT1_BGA_413P-T



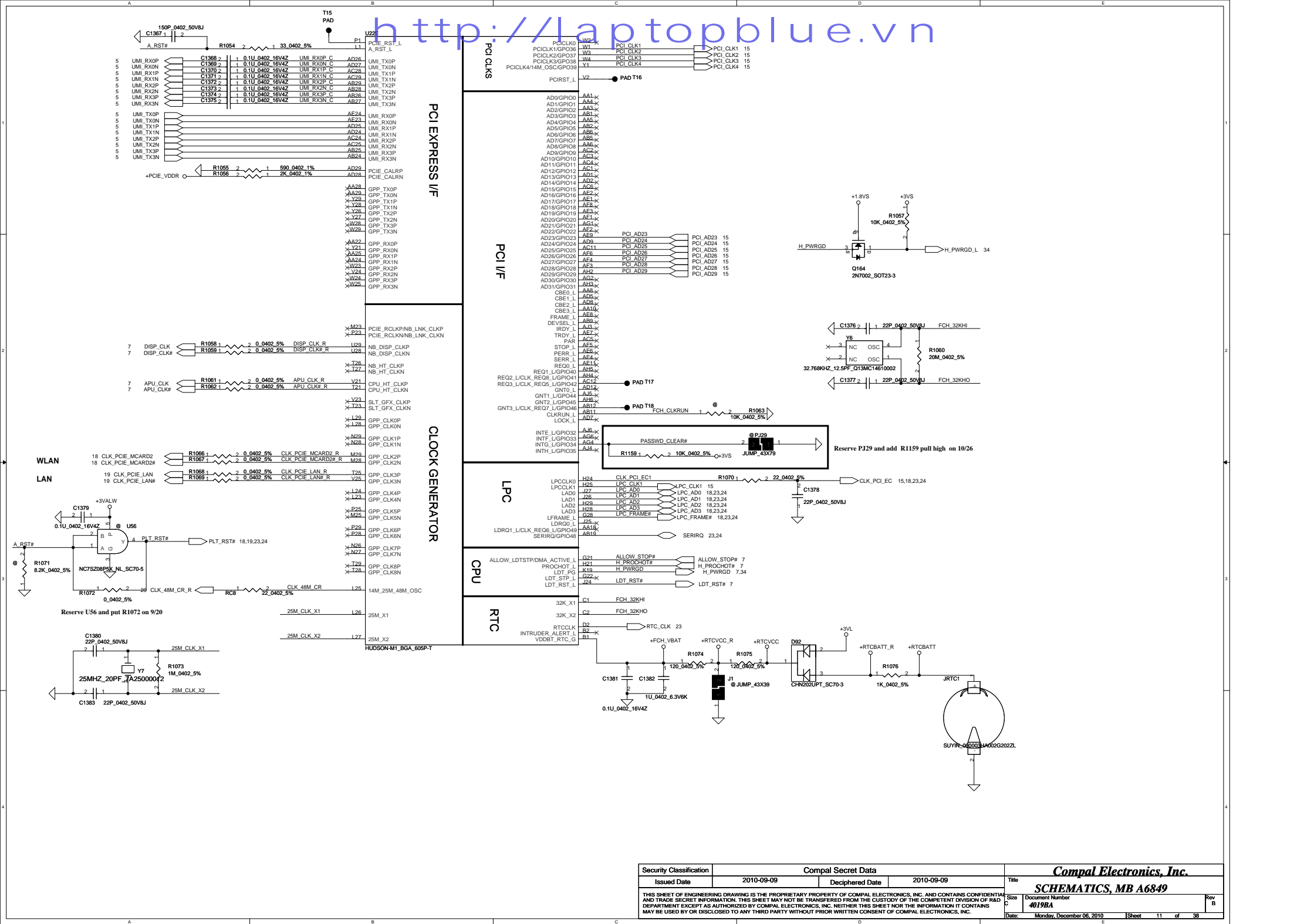
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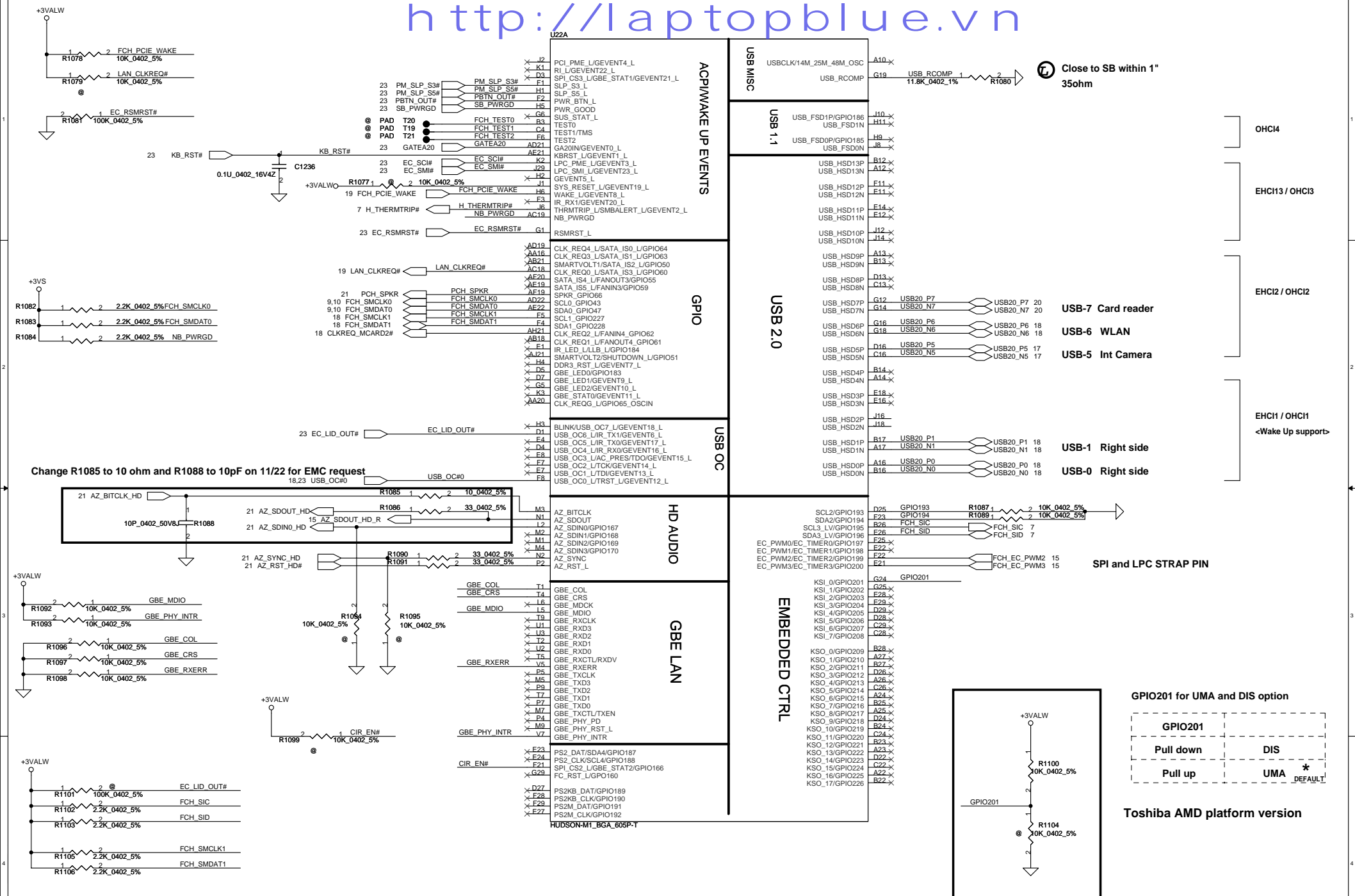


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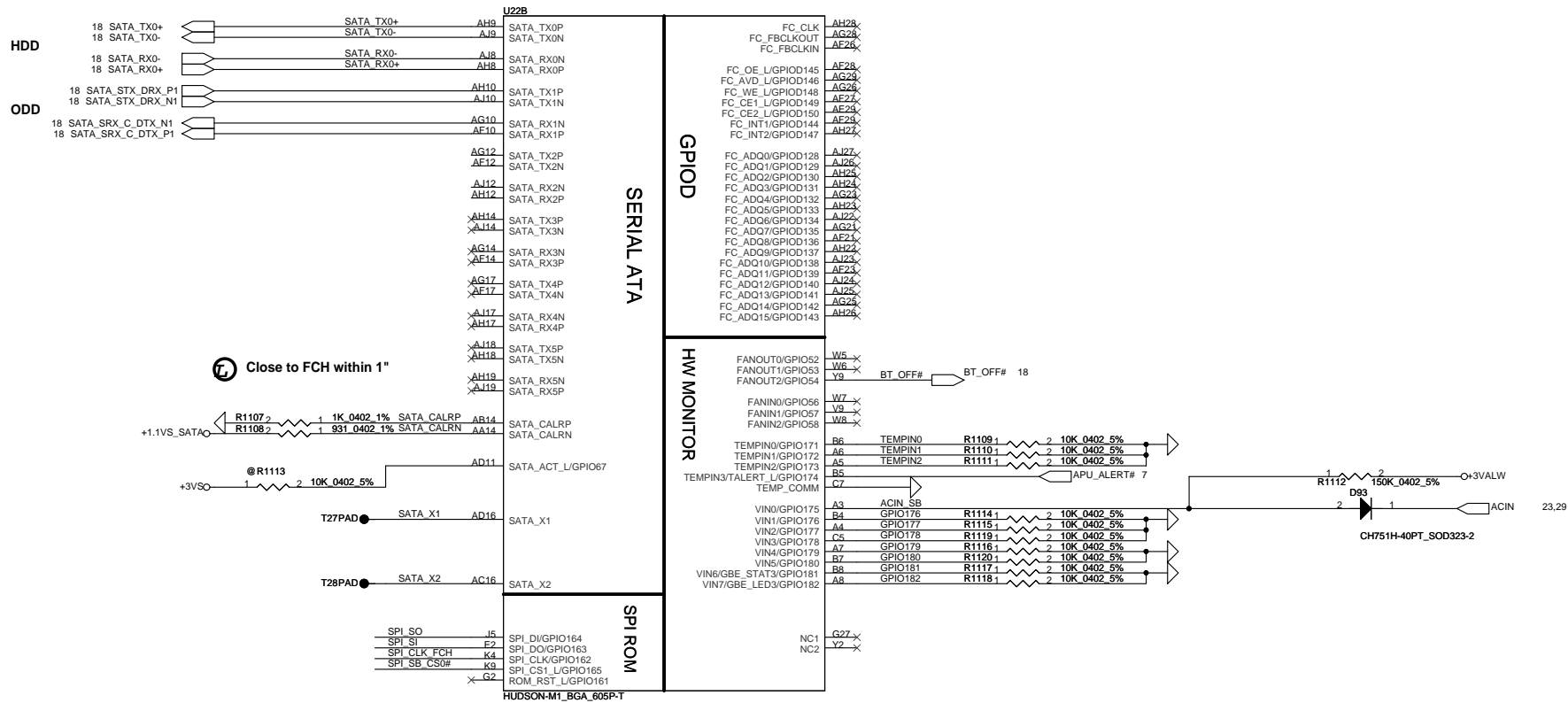


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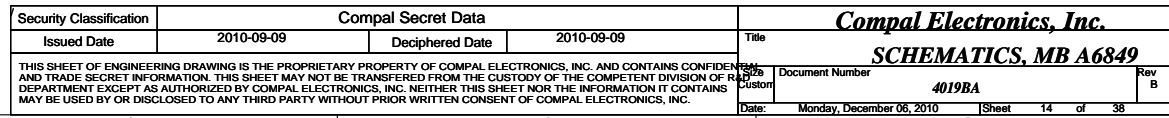




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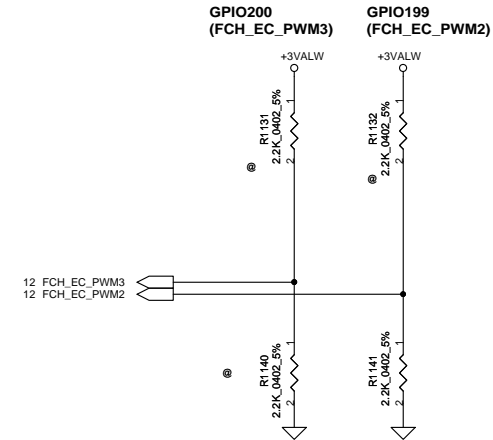
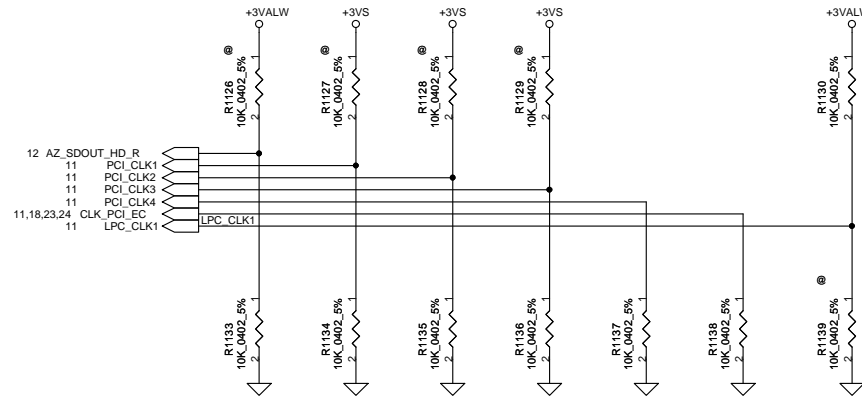
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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Disable	EC ENABLE	CLOCKGEN ENABLE	
							*	DEFAULT
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Enable	EC DISABLE	CLOCKGEN DISABLE	
	*	*	*	*	*	*		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		

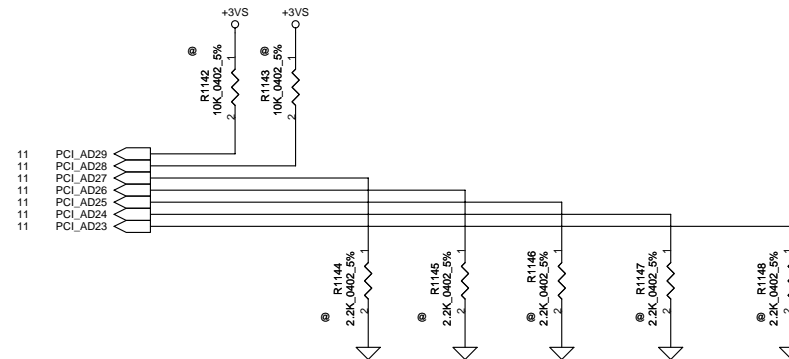
	GPIO200 (FCH_EC_PWM3)	GPIO199 (FCH_EC_PWM2)	
Reserved	2.2k pull down	2.2k pull down	
* SPI	Not contact	2.2k pull down	DEFAULT
LPC	2.2k pull down	Not contact	
Reserved	Not contact	Not contact	



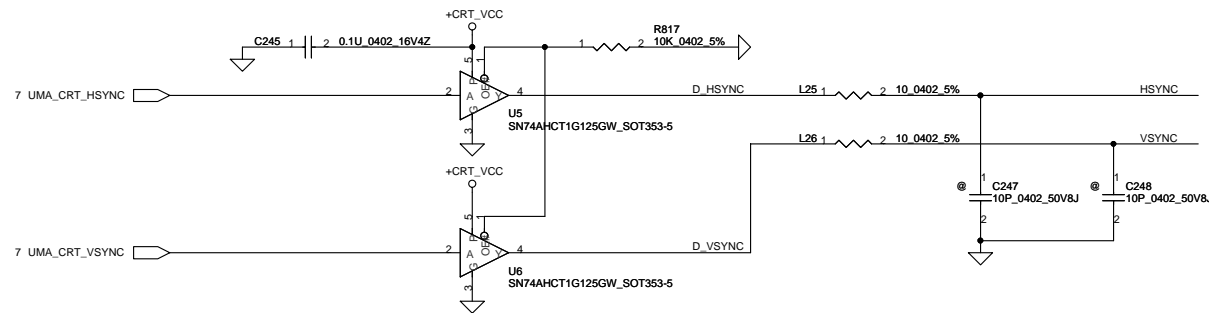
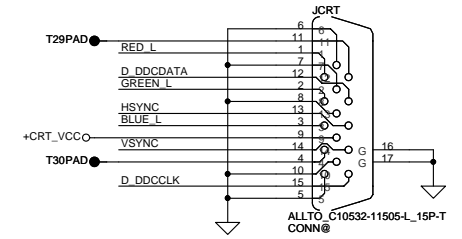
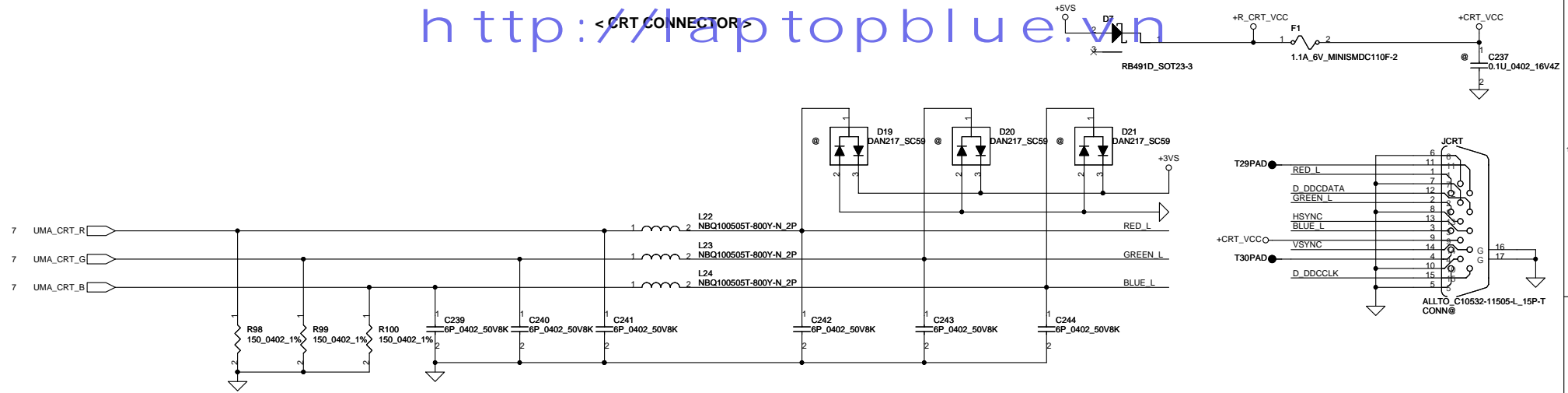
DEBUG STRAPS

M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

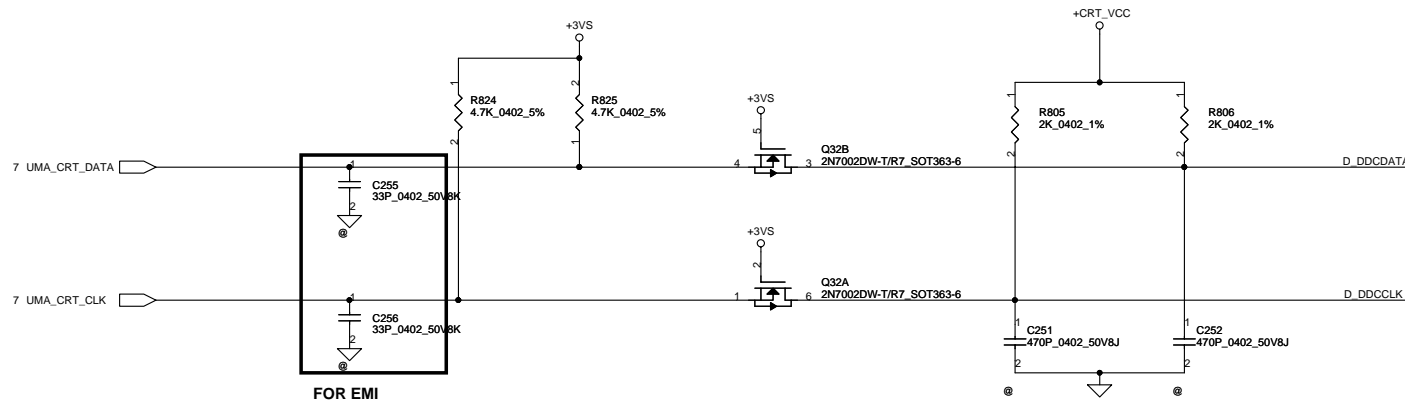
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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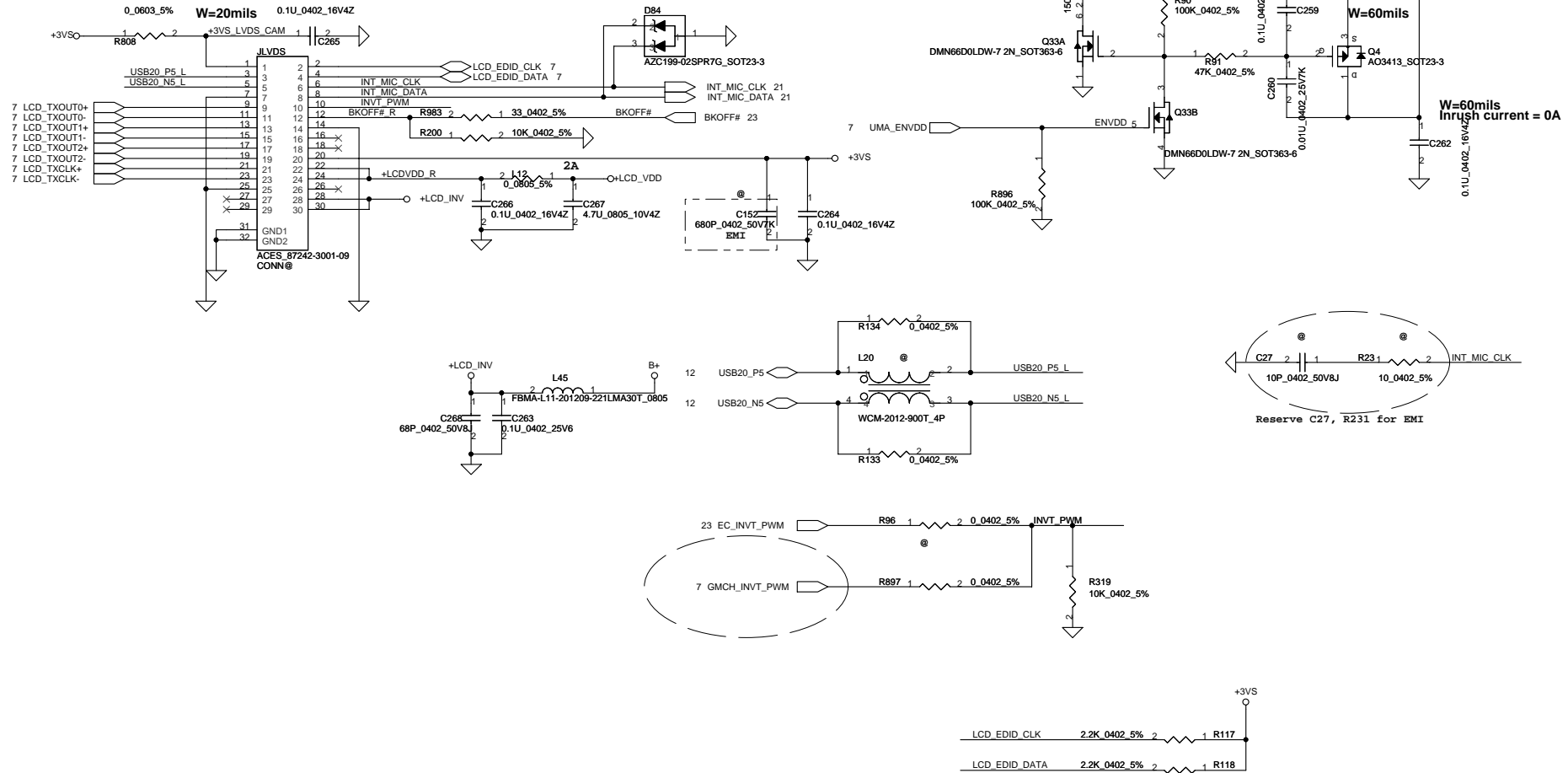


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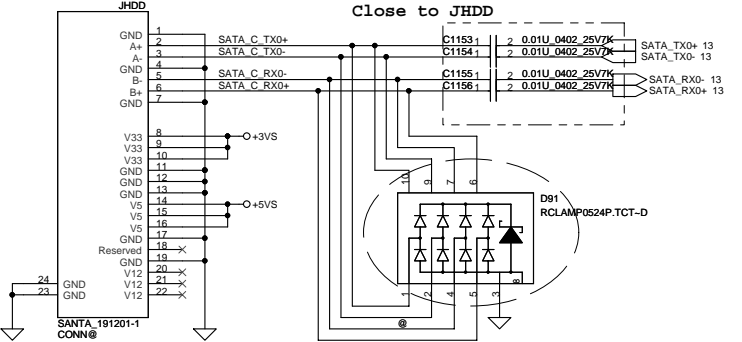
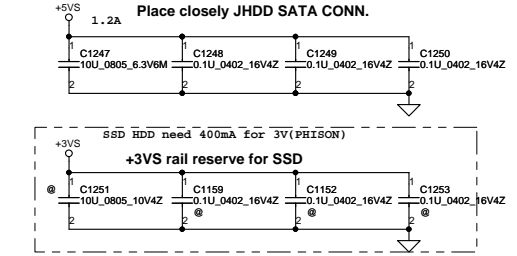
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LCD/PANEL BD. Conn.

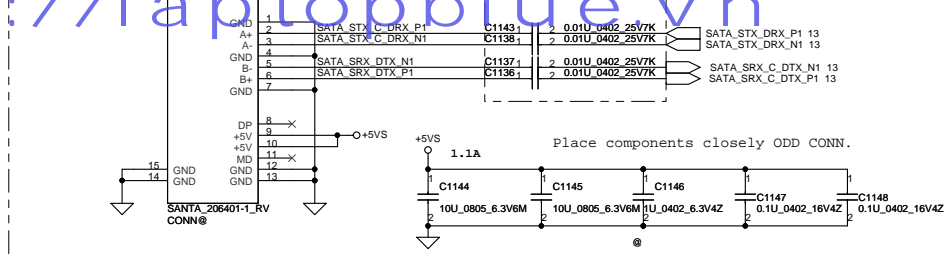


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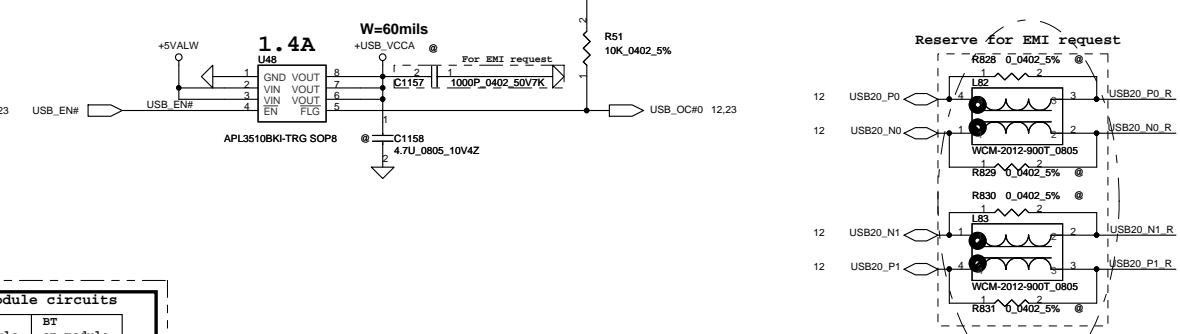
SATA HDD Conn.



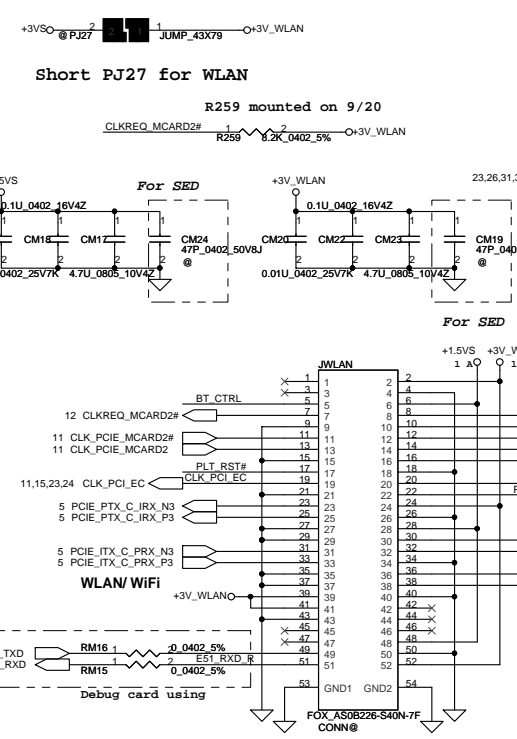
SATA ODD Conn

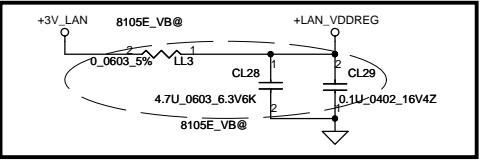
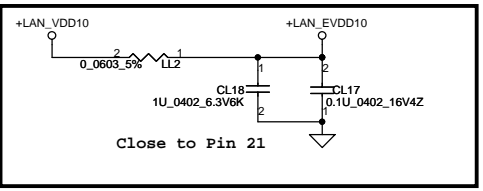
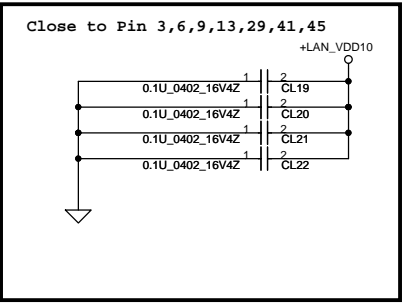
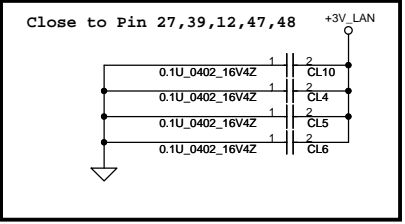
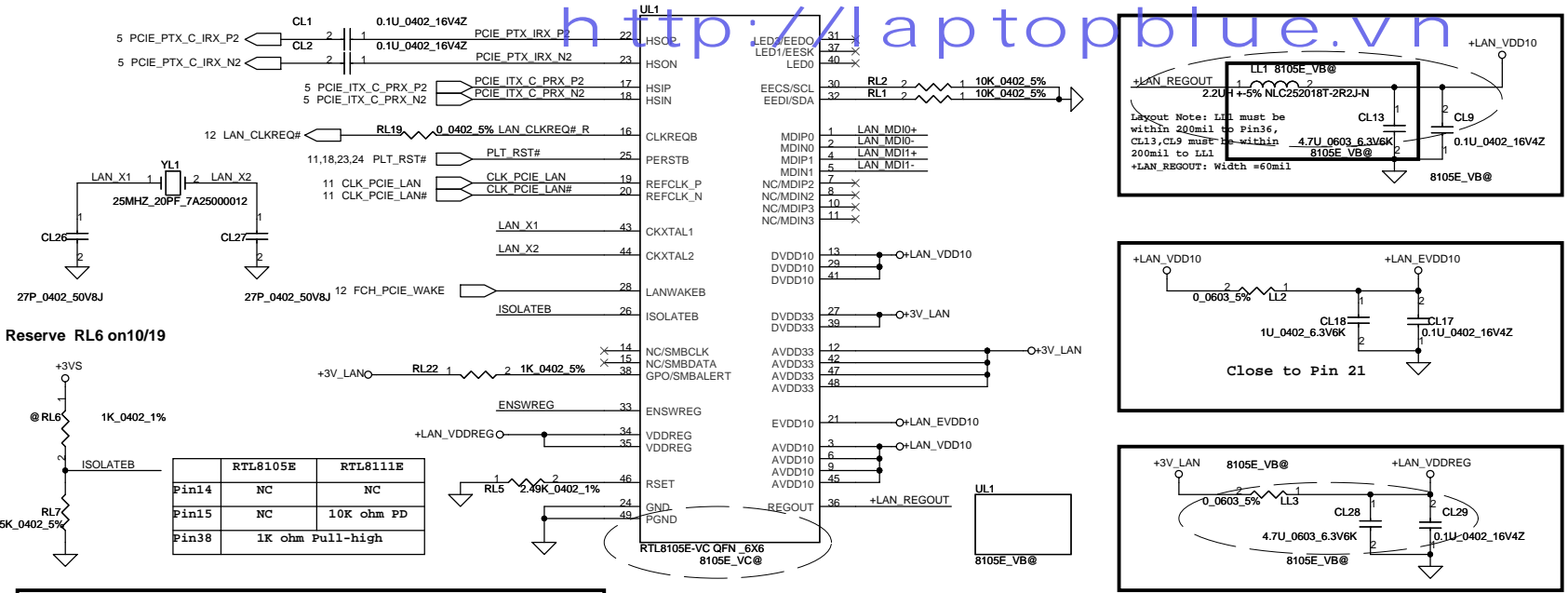


USB Port 0 & Port1

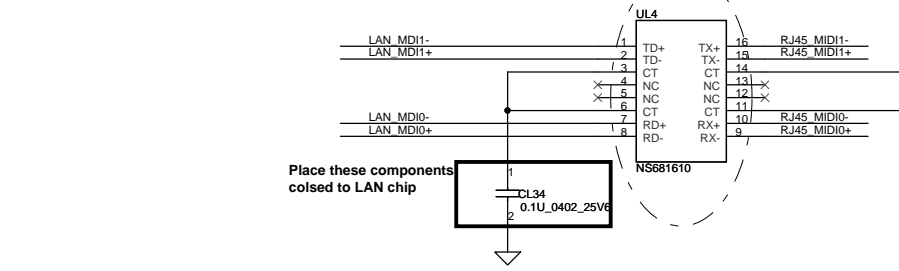
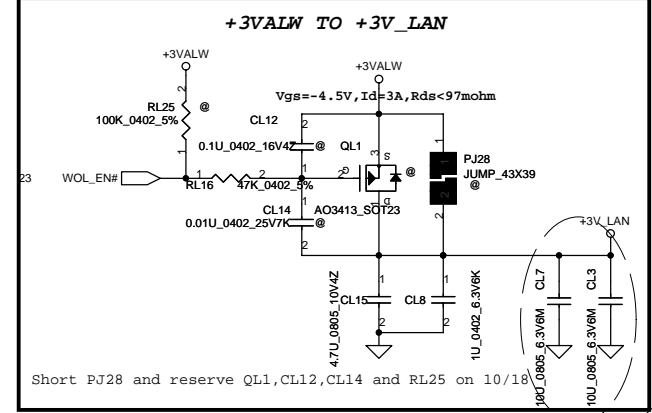
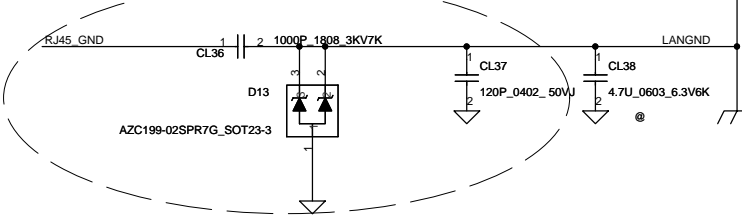
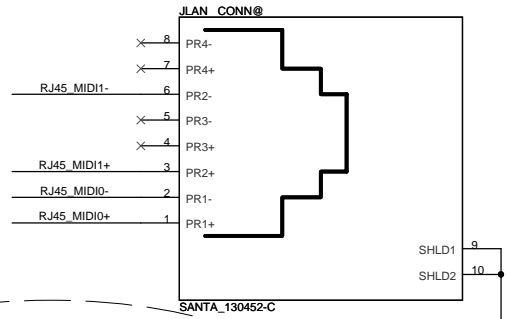
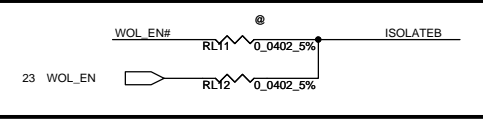
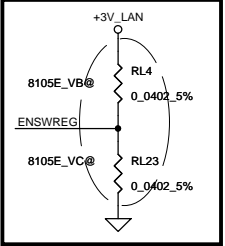


Slot#1 Half PCIe Mini Card-WLAN

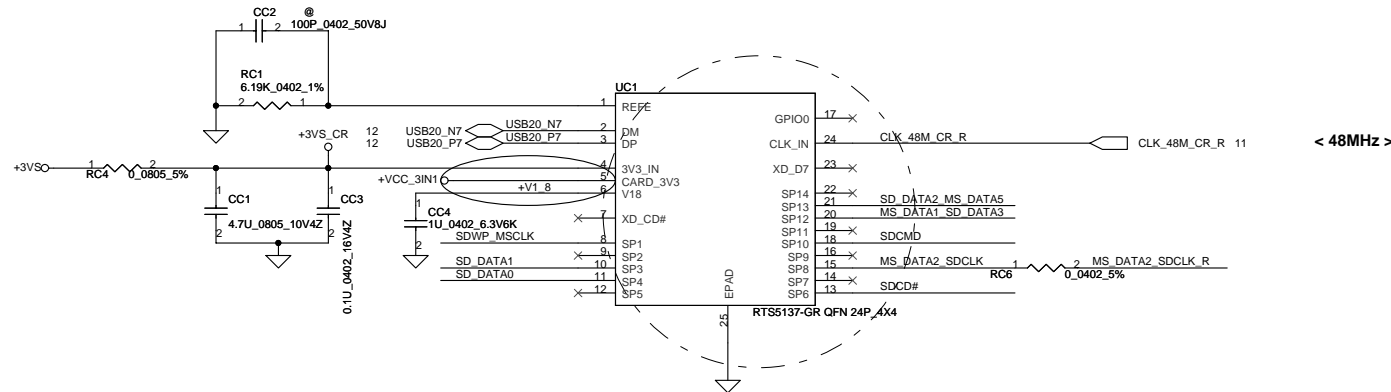




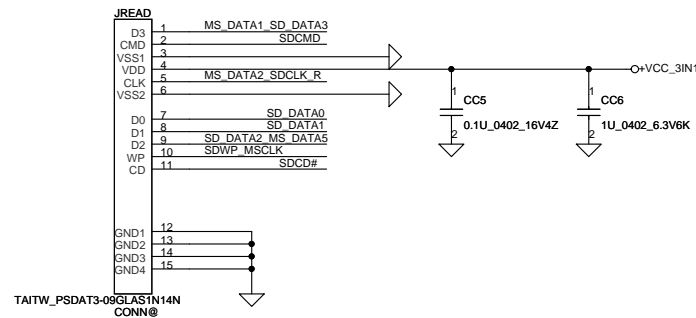
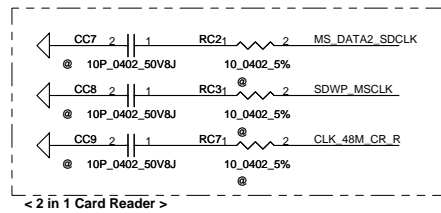
LAN Conn.



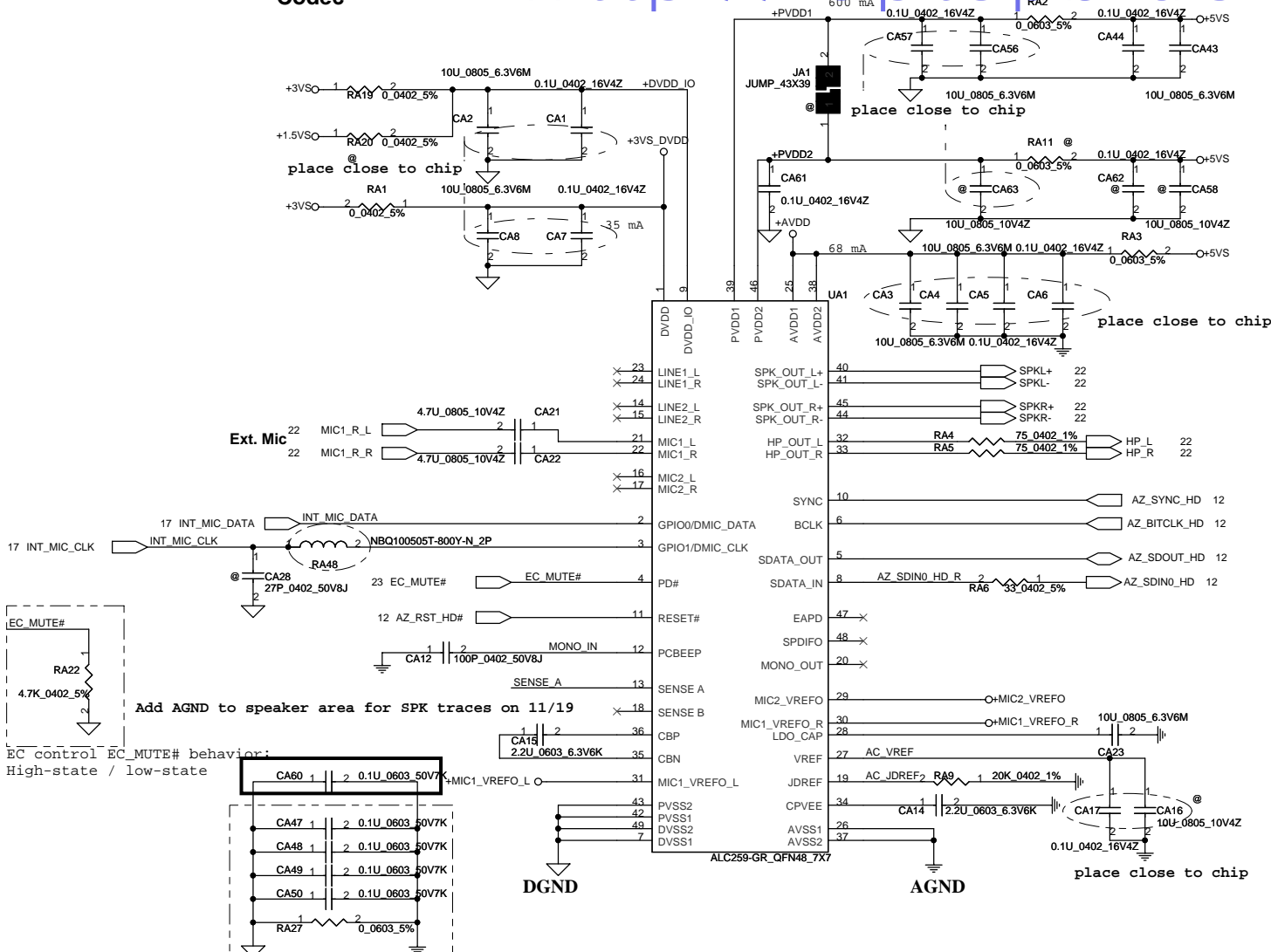
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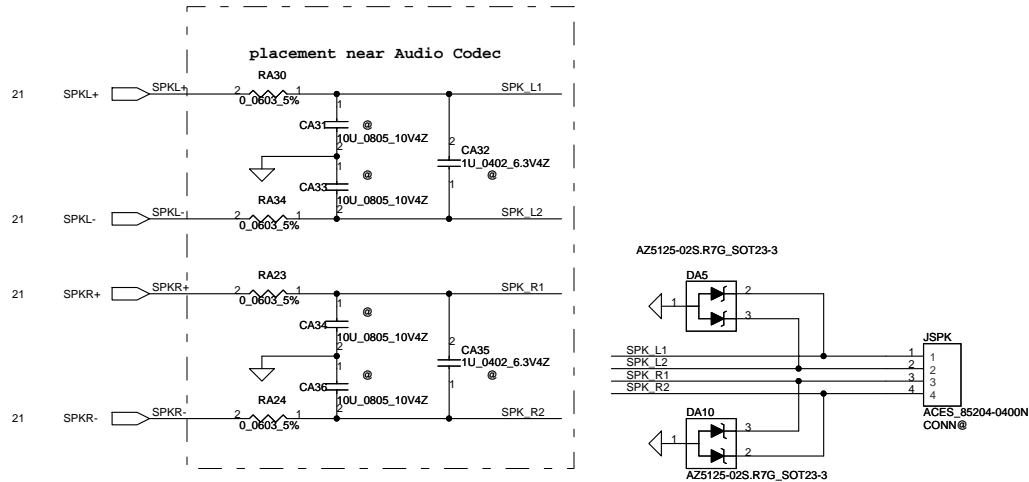
for EMI request



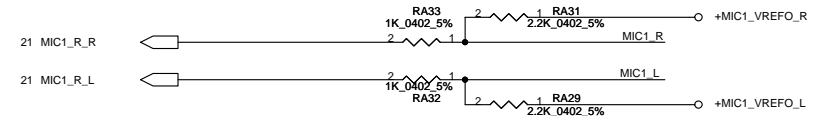
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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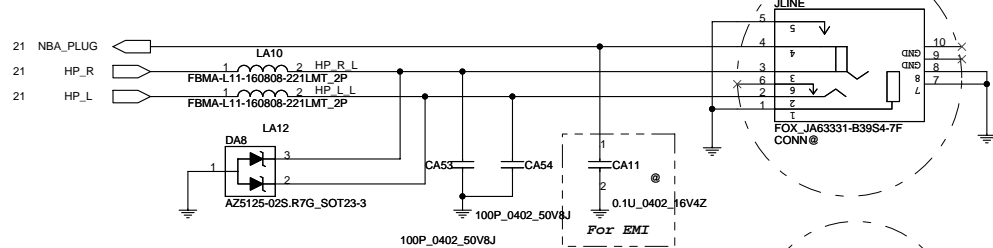
Speaker Connector



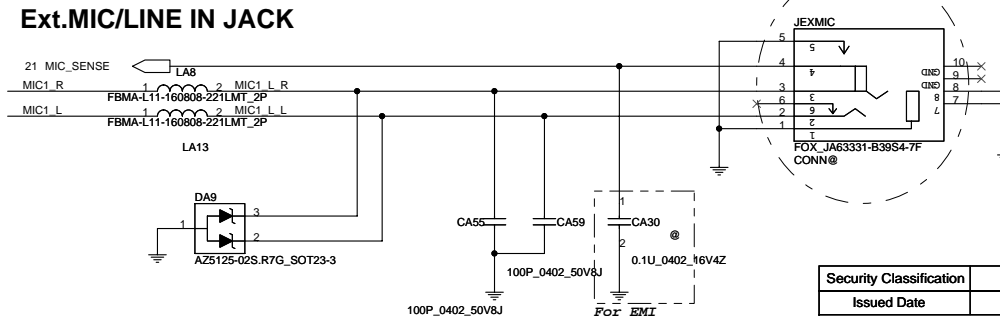
Ext.MIC/LINE IN JACK



HeadPhone/LINE Out JACK

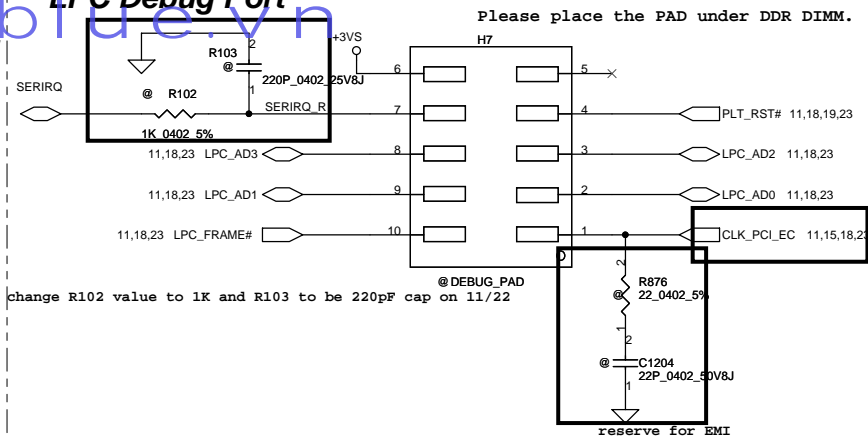


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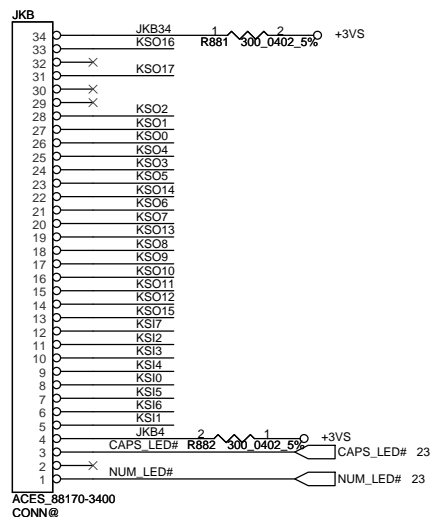


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http://laptopblue.vn



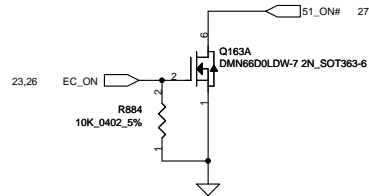
Reversed with KB Membrane Pin Definition



Please close to JKb1		
KSO16	1	2
KSO17	C1207	100P_0402_50V8J
	1	2
KSO2	C1208	100P_0402_50V8J
	1	2
KSO1	C1209	100P_0402_50V8J
	1	2
KSO0	C1210	100P_0402_50V8J
	1	2
KSO4	C1211	100P_0402_50V8J
	1	2
KSO3	C1212	100P_0402_50V8J
	1	2
KSO5	C1213	100P_0402_50V8J
	1	2
KSO14	C1214	100P_0402_50V8J
	1	2
KSO6	C1215	100P_0402_50V8J
	1	2
KSO7	C1216	100P_0402_50V8J
	1	2
KSO13	C1217	100P_0402_50V8J
	1	2
KSO8	C1218	100P_0402_50V8J
	1	2
KSO8	C1219	100P_0402_50V8J
	1	2
KSO9	C1220	100P_0402_50V8J
	1	2
KSO10	C1221	100P_0402_50V8J
	1	2
KSO11	C1222	100P_0402_50V8J
	1	2
KSO12	C1223	100P_0402_50V8J
	1	2
KSO15	C1224	100P_0402_50V8J
	1	2
KSI7	C1225	100P_0402_50V8J
	1	2
KSI2	C1226	100P_0402_50V8J
	1	2
KSI3	C1227	100P_0402_50V8J
	1	2
KSI4	C1228	100P_0402_50V8J
	1	2
KSI0	C1229	100P_0402_50V8J
	1	2
KSI5	C1230	100P_0402_50V8J
	1	2
KSI6	C1231	100P_0402_50V8J
	1	2
KSI1	C1232	100P_0402_50V8J
	1	2
CAPS LED#	C1233	100P_0402_50V8J
	1	2
NUM LED#	C1234	100P_0402_50V8J
	1	2

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Q163A change part number from SB00000AR00 to SB00000DH00 on 9/15



23 ON/OFFBTN#

ON/OFFBTN#

D12

1
2
3
4
5
6

POWER

1
2
3
4
5
6

ACES_85201-0405N

CONN@

AZ5125-02S.R7G_SOT23-3

[illegible]

$V_F = 1.9V(\text{typ}), 2.4V(\text{max})$
 $I_F = 20mA(\text{max})$

+5VALVO R768 2 510_0402 5% 2
 HT-110UYGS_YELLOW GREEN
 PWR_LED1 Z3

PCB

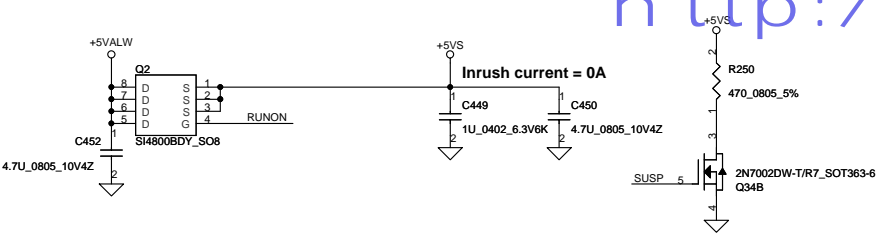
PCB SKU LA-6849P & LS-6841P Rev10

DC-IN

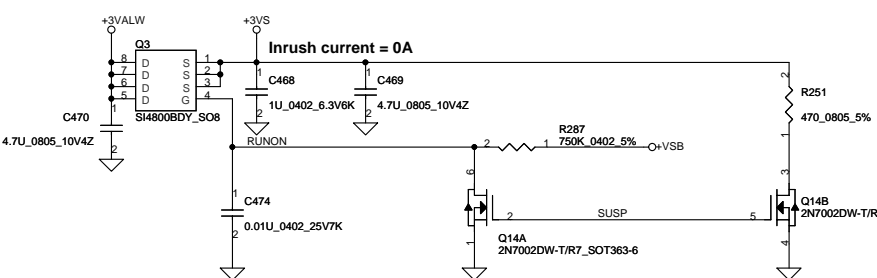
PJP1 45@

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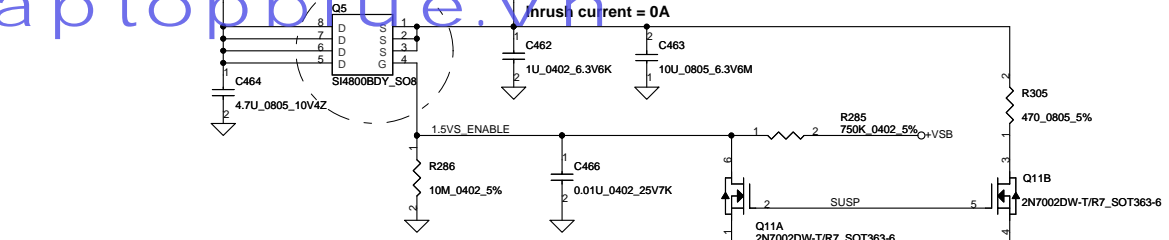
< +5VALW TO +5VS >



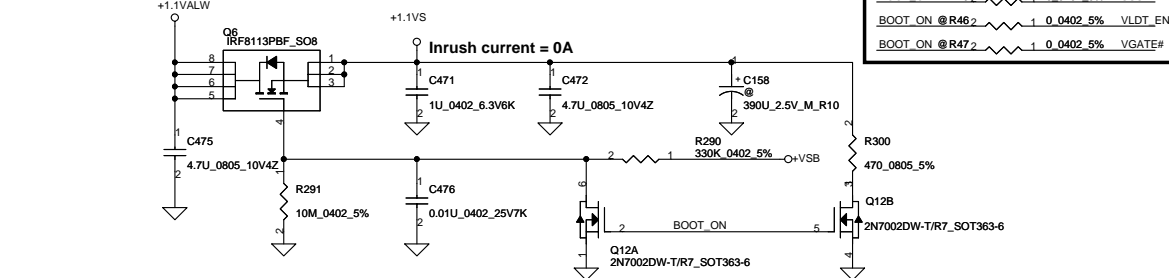
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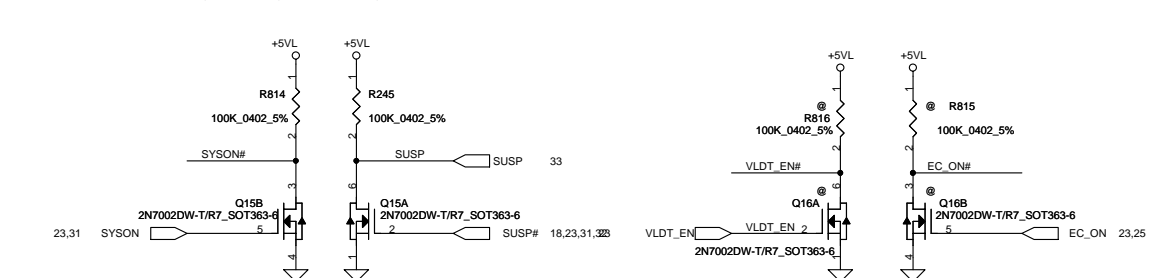
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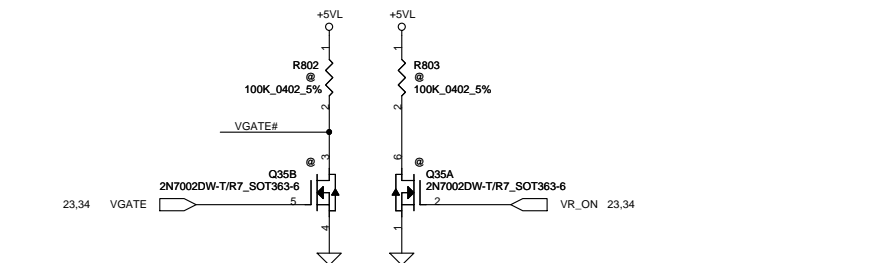
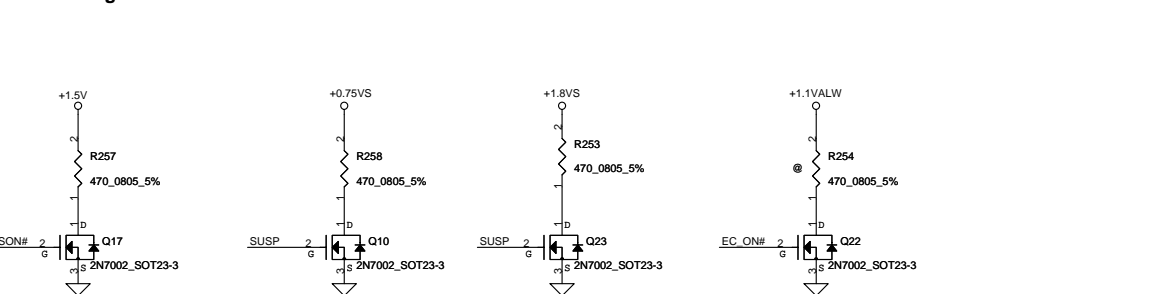
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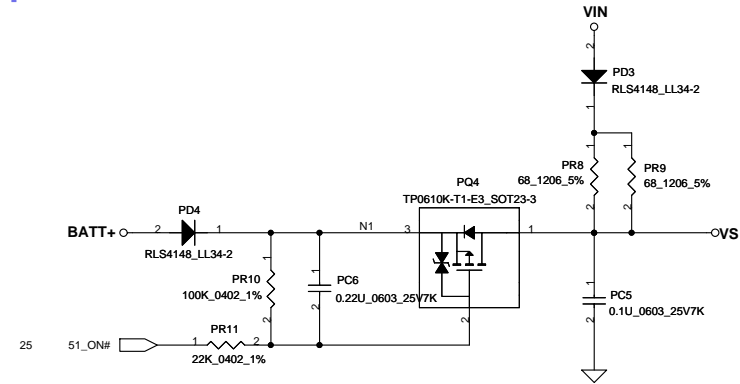
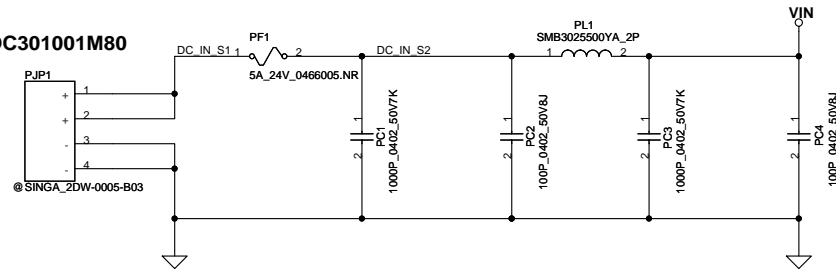
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



< Discharge circuit >



DC301001M80



③ PJ332
JUMP_43X118
(5A,200mils ,Via NO.= 10)
OCP=8.6A

③ PJ2
JUMP_43X39
(120mA,20mils ,Via NO.= 1)

③ PJ112
JUMP_43X118
(10A,600mils ,Via NO.= 10)
OCP=A

③ PJ352
JUMP_43X118
(5A,200mils ,Via NO.= 10)
OCP=7.9A

③ PJ182
JUMP_43X118
(2.15A,100mils ,Via NO.= 5)
OCP=A

③ PJ102
JUMP_43X118
(5.7A,240mils ,Via NO.= 12)
OCP=A

③ PJ3
JUMP_43X39
(100mA,20mils ,Via NO.= 1)

③ PJ152
JUMP_43X118
(5A,200mils ,Via NO.= 10)
OCP=A

③ PJ76
JUMP_43X79
(0.5A,20mils ,Via NO.= 1)

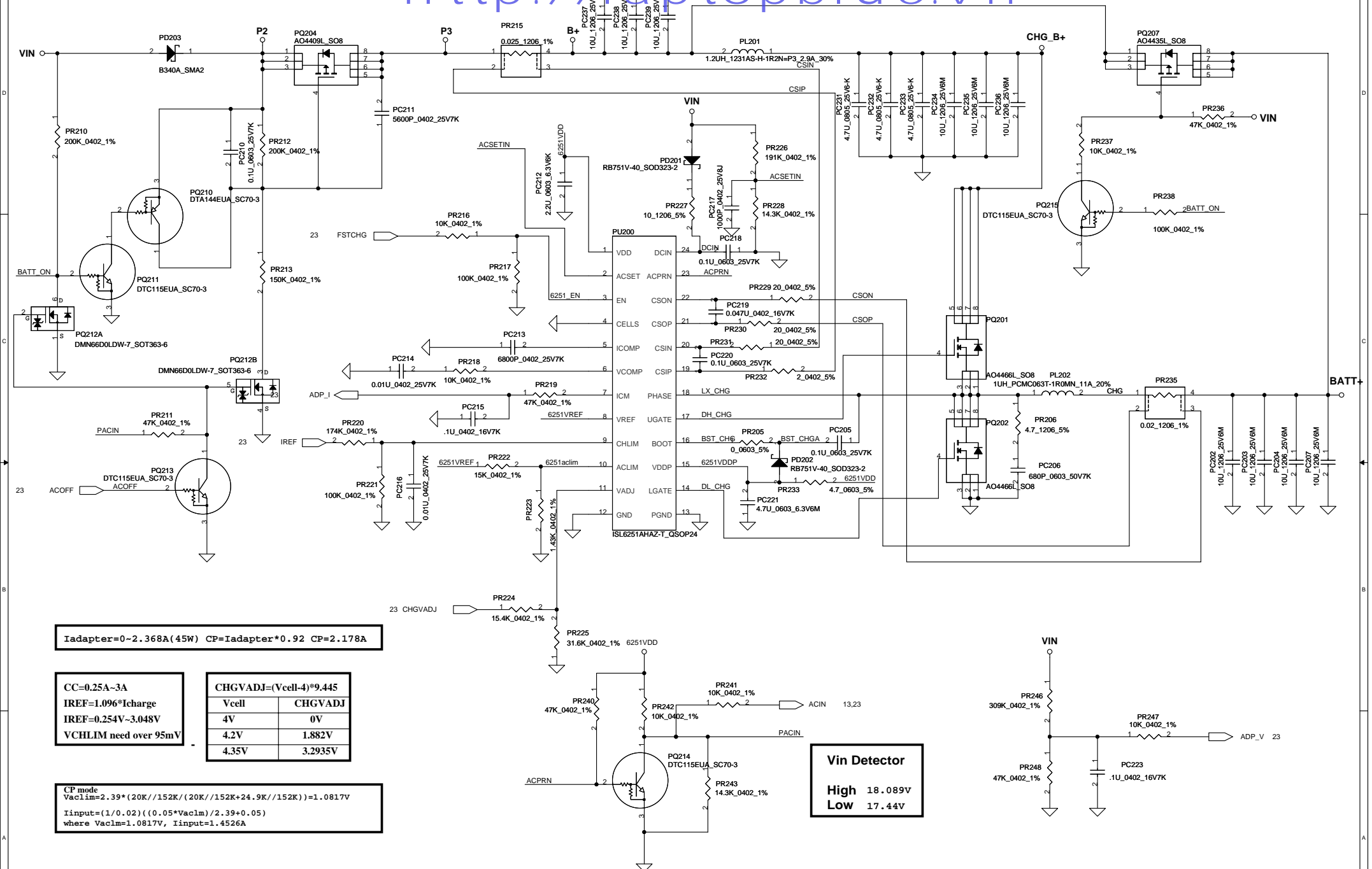
③ PJ4
JUMP_43X39
(100mA,20mils ,Via NO.= 1)

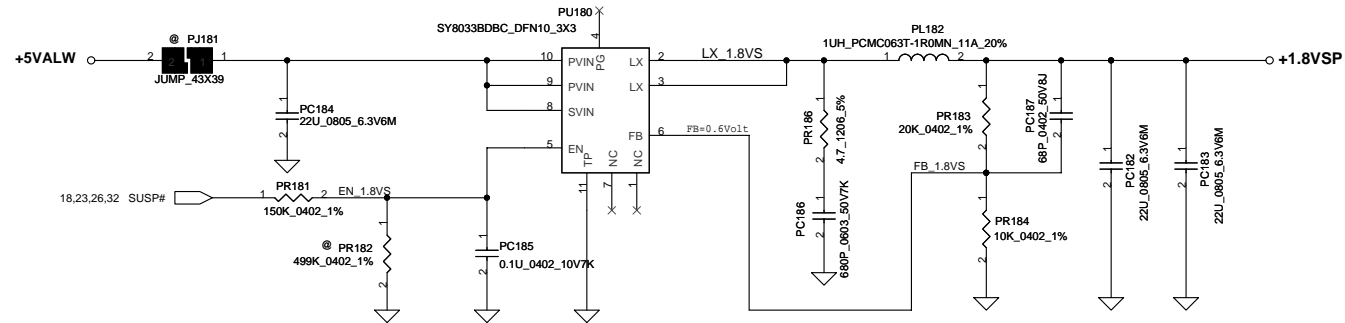
③ PJ5
JUMP_43X118
(10A,400mils ,Via NO.= 20)
OCP=A

ACIN

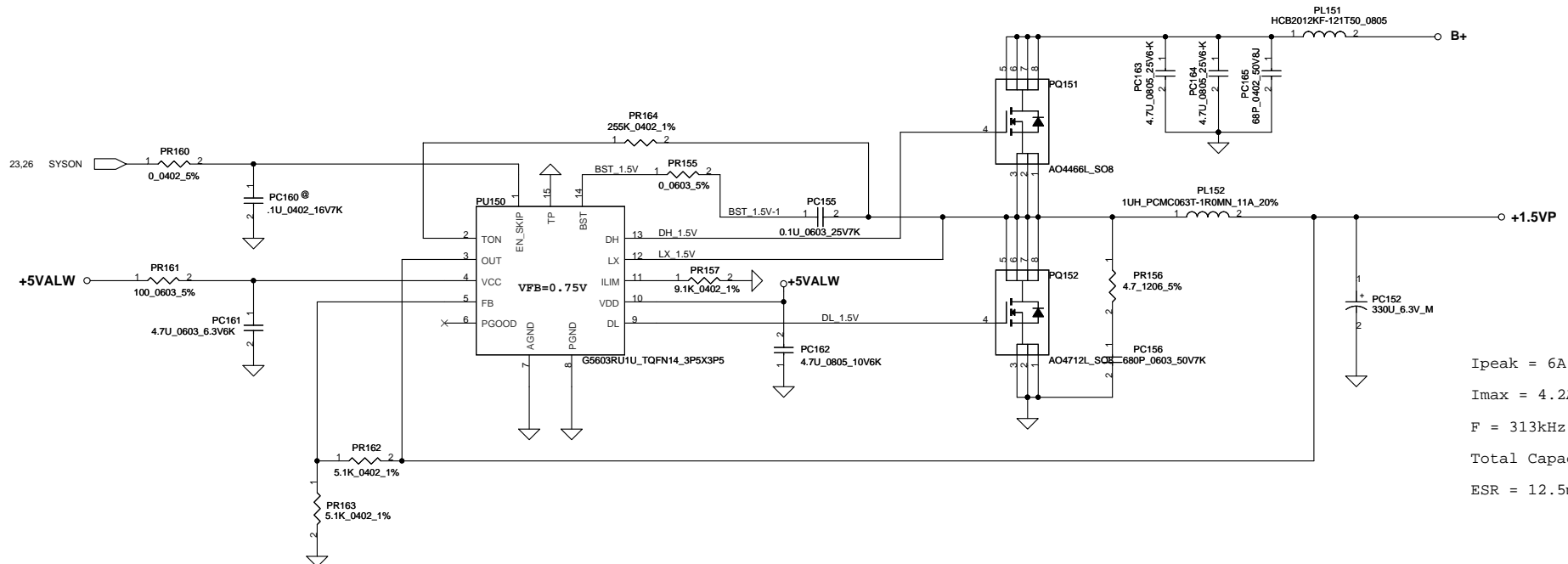
Precharge detector			
Min.	typ.	Max	
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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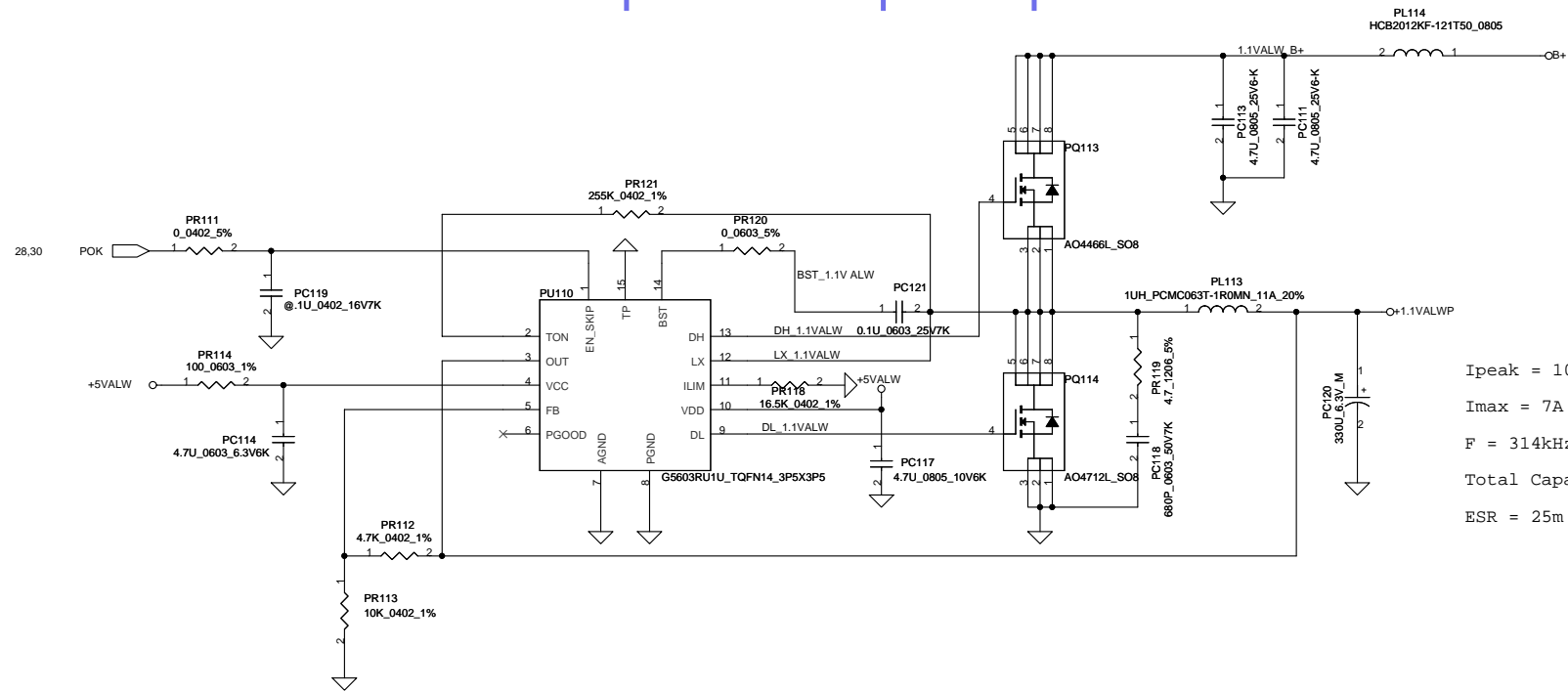




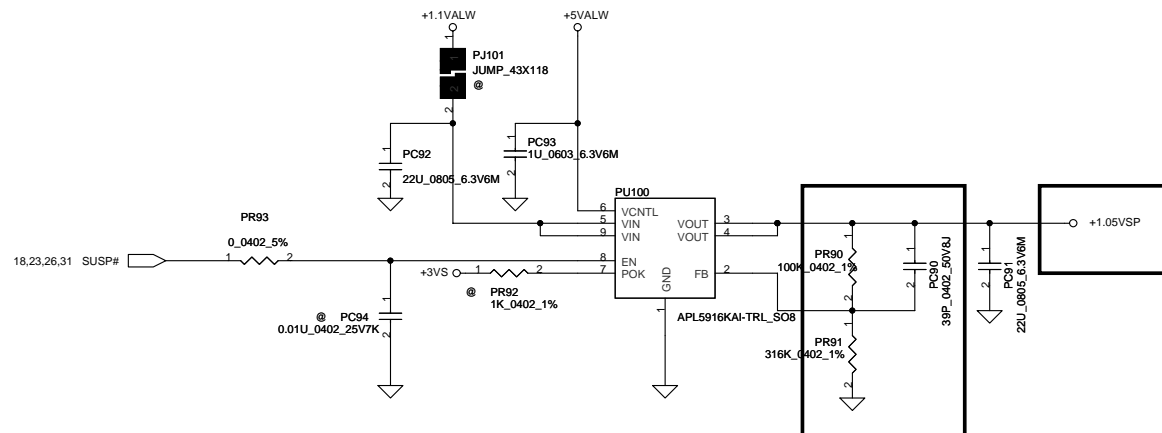
Ipeak = 2.15A
 Imax = 1.505A
 ILIM = 4A
 F = 1M Hz
 Total Capacitor = 264 uF
 ESR = 2.273m Ohm

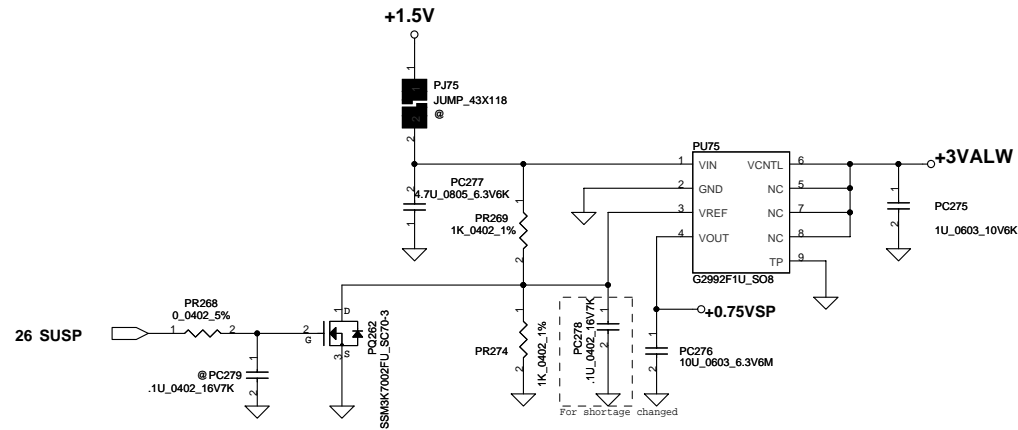


Ipeak = 6A
 Imax = 4.2A
 F = 313kHz
 Total Capacitor = 440 uF
 ESR = 12.5m Ohm



Ipeak = 10A
 Imax = 7A
 F = 314kHz
 Total Capacitor = 220 uF
 ESR = 25m Ohm





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Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2010/08/01	POWER		Release
P31	BATTERY CONN / OTP	2010/09/02	POWER	Add PD5,PD6 (For ESD)	DVT
P32	CHARGER	2010/09/02	POWER	Add PR246,PR247,PR248,PC223 (ADP_V)	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR337,PR357 change to 121k	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR365 change to 19.6k	DVT
P34	1.8VSP/1.5VP	2010/09/02	POWER	PR181 change to 150k, PC185 0.1uF	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PR91 change to 316k(For 1.05VSP)	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PC90 change to 39pF(1.05VSP)	DVT
P37	ACPU_CORE	2010/09/02	POWER	Add PR578 10_0402_5% , PR573 unpop.	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR577 change to 23.7k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR539 change to 26.1k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR540 change to 90.9k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PC551 change to 100pF	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR546 change to 0_0402_5%	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR580 change to 6.98k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR581 change to 1.87k	DVT
P32	CHARGER	2010/09/06	POWER	Add PC207,PC239 10uF (EMI)	DVT

Version change list (P.I.R. List)

H/W section

Item	Reason for change	P6#	Modify List	Date	Ver#		
1	Change pull up voltage from +5VALW to +5VL	26	Change Q15A,Q15B,Q16A,Q16B,Q35A,Q35B from +5VALW to +5VL	2010/09/15			
2	Net VR_ON# is unused	26	Delete net VR_ON# on 9/15	2010/09/15			
3	Sleep and Charge function unused	13	Delete R1119 & R1120 & net SLP_CHG_M3, & SLP_CHG_M4	2010/09/15			
4	Change power from 1.0V to 1.05V	8	Net +1.0V8_VDDOL ---->+1.0V88_VDDOL Net +1.0V8_VDD ---->+1.0V88_VDD	2010/09/15			
5	Add debug card port on wlan connector	18	Add LPC_AD0,LPC_AD1,LPC_AD2,LPC_AD3,LPC_FRAME# on Jwlan	2010/09/15			
6	Change H7 Pin	24	Connect H7 Pin1 from CLK_PCI_IO0 to LPC_CLK1	2010/09/15			
7	Add debug card port on Jwlan	18	Pin17 => FLT_RST# and Pin19 => CLK_PCI_EC	2010/09/15			
8	Change Q33A,Q33B,Q8A,Q8B,Q163 Part Number	7,17,25	change part number from SB00000A800 to SB00000D800	2010/09/15			
9	For EMS request	12,23	Add C1198,C1236,C1237	2010/09/15			
10	For EMS request	7	Add R1149 to R1158	2010/09/15			
11	H_THERMTrip# leakage risk	7	Add Q183 and R184 and W094 to enable H_THERMTrip# on 9/18	2010/09/18			
12	Change H7 Pin	24	Connect H7 Pin1 from LPC_CLK1 to CLK_PCI_EC	2010/09/20			
13	Remove 75W_65W net name in UMA platform.	23	Remove 75W_65W net name in UMA platform.	2010/09/20			
14	USB_OC#0 add pull high 10K to +3VALW	18	USB_OC#0 add pull high R51 to +3VALW	2010/09/20			
15	use VLDT_EN# to turn on +1.1VALW to +1.1VS	26	Reserve R46 and stuff R45	2010/09/20			
16	use BT_OFF# to control BT_CTRL	11	Delete net BT_FWR#	2010/09/20			
17	use BT_OFF# to control BT_CTRL	13	Add bat BT_OFF# on U22.Y9	2010/09/20			
18	use BT_OFF# to control BT_CTRL	18	Change control net from BT_FWR# to BT_OFF# and add R116 bypass BT_OFF# & BT_CTRL, and reserve GM1	2010/09/20			
19	For desigh change	26	Reserve Q16A,Q16B,Q35A,Q35B,R802 ,R803,R815,R816	2010/09/20			
20	For desigh change	18	Put R259	2010/09/20			
21	For desigh change	11	Reserve U56 and put R1072	2010/09/20			
22	HDMI unused	11	TEST35 pull down through R1029	2010/09/20			
23	For desigh change	7	Reserve R1014 and R1006,put R1002 ,R1004, and R1010	2010/09/20			
24	For desigh change	7	Remove R92 ,R93,and R94 pull up and down resistor	2010/09/23			
25	For desigh change	13	Pull down GP10178 and GP10180 with R1119 & R1120	2010/09/23			
26	For desigh change	19	Mount RL6 on 10/4	2010/10/04			
27	For desigh change	25	Delete H3 and H5	2010/10/04			
28	Change +3VL_LID power rail from +3VALW to +3VL	24	Add R97 and reserve R101/Add net name +3VL_LID	2010/10/13			
29	Change +3VL_LAN turn on pin from WOL_EN# to +3VALW	19	Short D728 and reserve Q11,CL12,CL14 and RL25	2010/10/18			
30	Use WOL_EN to enable ISOLATEB	19	Reserve RL6 on 10/4	2010/10/19			
31	Change Q164 footprint to SOT23-3	15	Change Q164 P/N to SB8570020020	2010/10/19			
32	Add clearing password feature controlled by bios	15	Reserve D729 and add R1159 pull high	2010/10/26			
33	For mechanical desigh change	25	Delete H15	2010/10/27			
34	H7 debug port function unused	25	Add R103 and reserve R102	2010/11/17			
35	H7 debug port function unused	24	Change R102 value to 1K and R103 to be 220pF cap	2010/11/22			
36	For EMS request	21	Change R1085 to 10 ohm and R1088 to 10pF	2010/11/22			
37	Add AGND to speaker area for SPK traces	21	Add CA60 capacitor to short GND and AGND	2010/11/19			

Version Change List (P. I. R. List) for Power Circuit

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	Rev.
2010 . 06 . 21 Release					
2010 . 07.25 modification list					
	P 33		PC16 change to SE070104Z80	Defore material EOL	PVT
	P 38		PU12 change to SA000022M80	Before material MP schedule will impact PWWAE MP schedule	PVT
	P 33		Remove PD6 , PD8 @	ESD test fail	PVT
	P 34		Add PC132 , remove PC130 , PC131 , PR69 , PC41 @	For EMI fail	PVT
	P 35		Add PC51 , remove PC49 , PC46 , PC57 , PC58 , PR89 , PR90 @	For EMI fail	PVT
	P 36		Add PC79 , PC91 , PC133 , remove PR100 , PR108 , PC68 , PC77 @	For EMI fail	PVT
	P 38		Remove PR125 , PR139 , PR151 , PC106 , PC111 , PC117 @	For EMI fail	PVT
2010 . 08.10 modification list					
	P 37		Change PU9 , PU11 to SA053310110	UP7711 stop using from now on	Pre-MP
	P 38		Add PC218 , PC219 , PC371	For VCORE Ripple	Pre-MP
	P 32		Add PR8	For Precharge rising current	Pre-MP
	P 32 , P 33		PQ1 , PQ2 , PQ6 change to SB900840003	SB906100210 material delivery had problem	Pre-MP
2010 . 08.16 modification list					
	P 35		Change PU5 to SA000020C80	UPI product stop using	Pre-MP
2010 . 08.17 modification list					
	P 34		Change PU4 to SA00001EP80	SA00003TK00 stop using	Pre-MP
	P 38		Remove PR127 @	To solve +1.1VALW noise	Pre-MP
2010 . 08.23 modification list					
	P 34		Remove PR193 , PQ39 @	For PWWAE MP use 25W CPU	Pre-MP

AC POWER ON AMD APU Brazos FT1-FCH Hudson M1

