

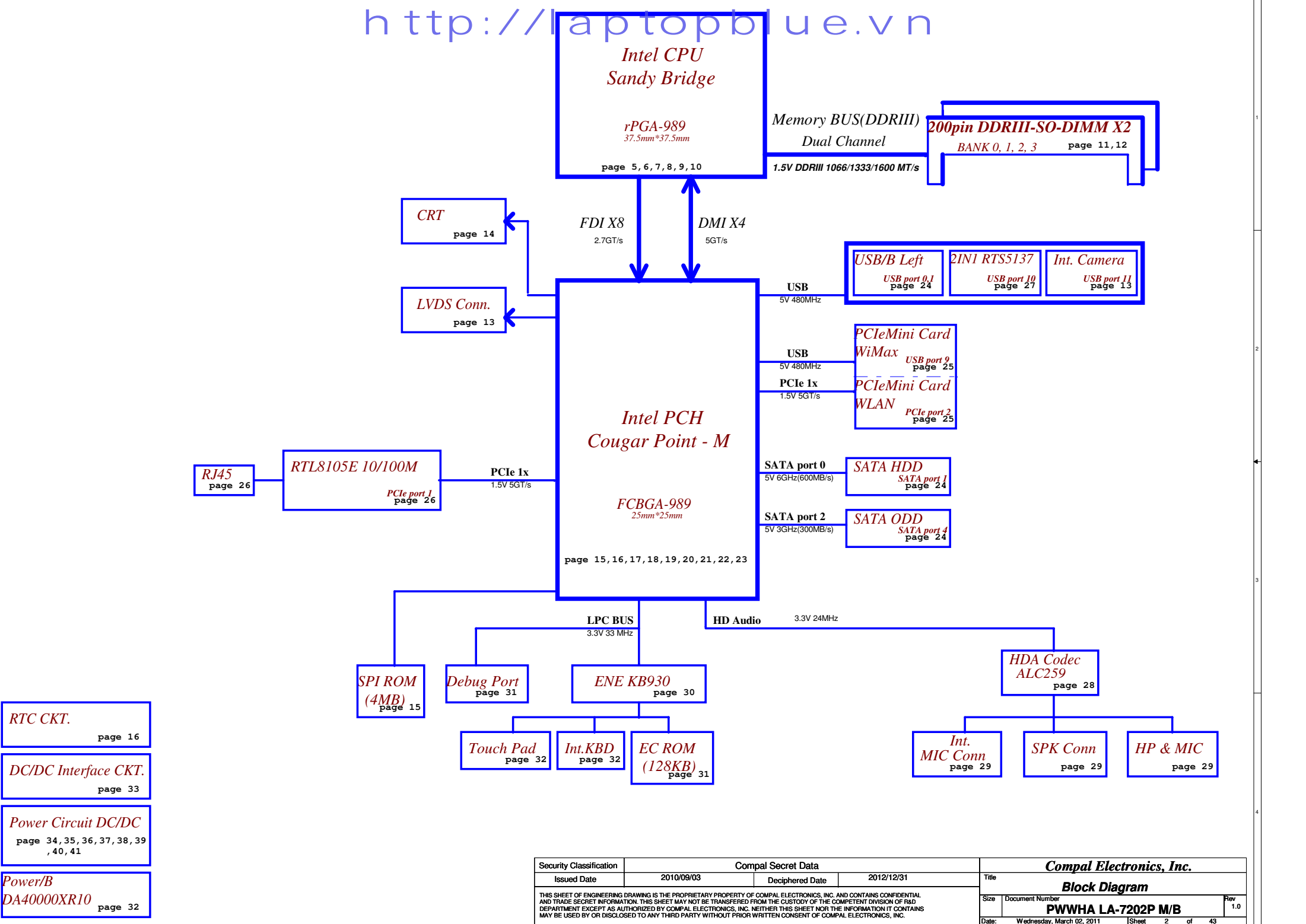
PWWHA

Delhi 10R

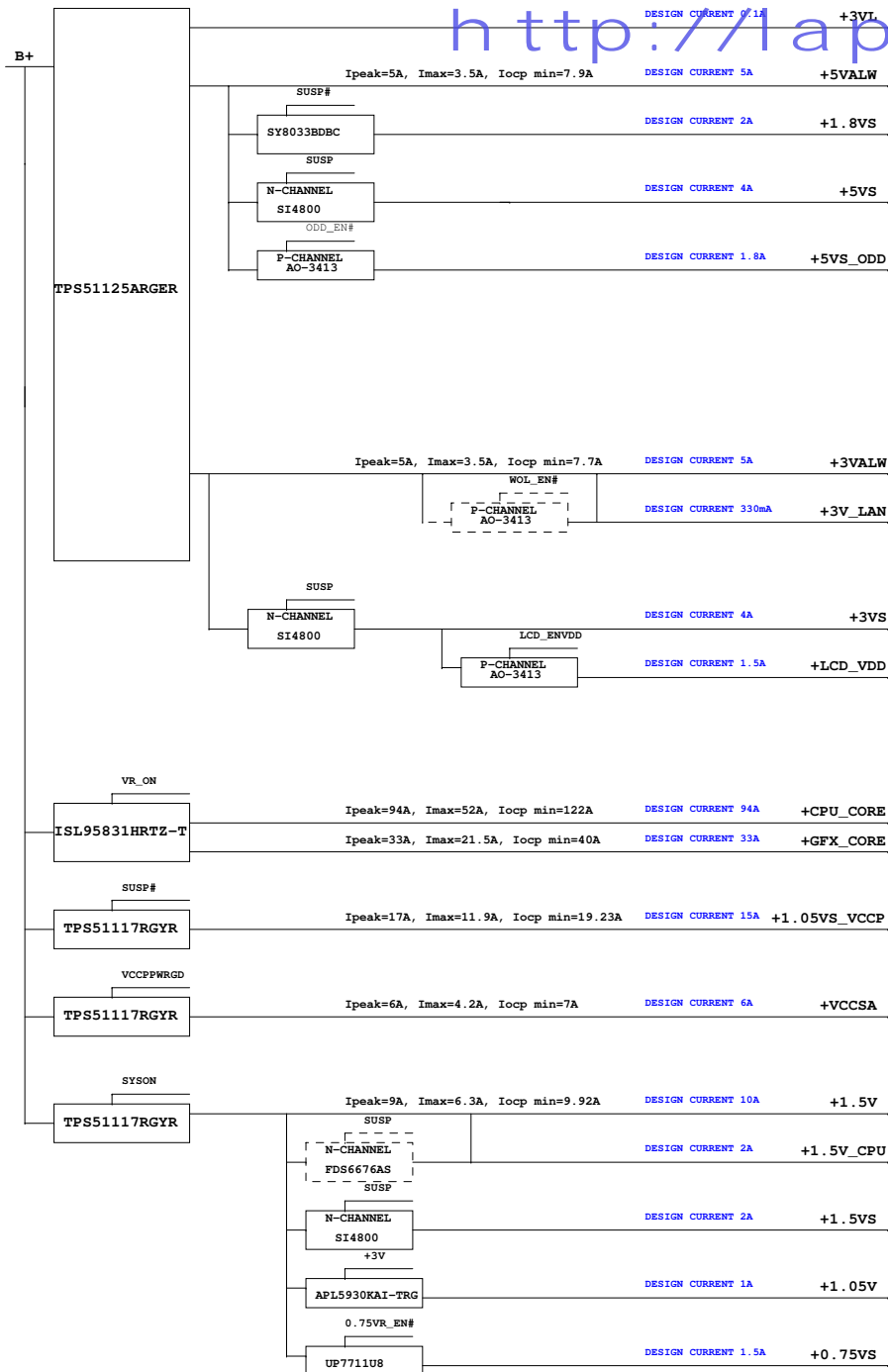
LA-7202P REV 1.0 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2011-02-08 Rev 1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

http://laptopblue.vn

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
	S0	O	O	O	O	O
	S1	O	O	O	O	O
	S3	O	O	O	O	X
	S5 S4/AC	O	O	O	X	X
	S5 S4/ Battery only	O	O	O	X	X
	S5 S4/AC & Battery don't exist	O	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

EC SM Bus2 Address

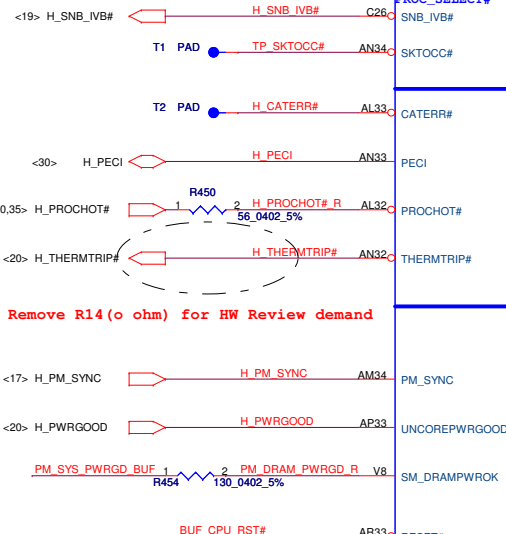
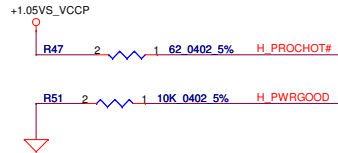
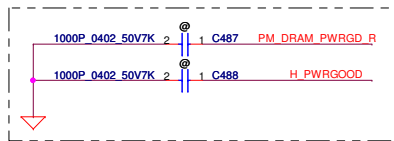
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b

BTO Option Table

Function	MINI PCI-E SLOT	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
description	SLOT1	LAN		Camera & Mic	FAN		S3 Power Saving		Load Power Switch	
explain	WIMAX	10/100M	Giga	Camera & Mic	PWM	RPM	1.5V	1.5VS	Old Sch.	New Sch.
BTO	WIMAX@	8105E@	8111E@	CAM@	PWM@	RPM@	WPS3@	PS3@	OLS@	NLS@

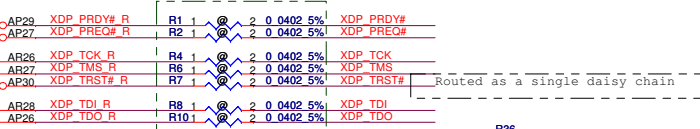
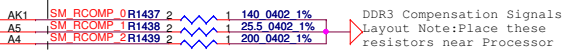
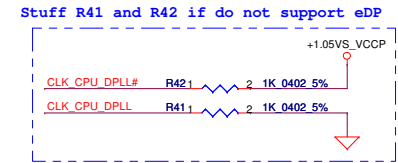
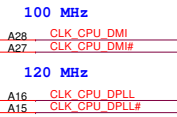
STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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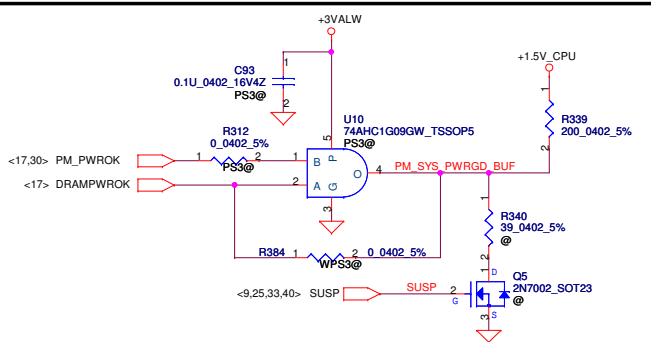
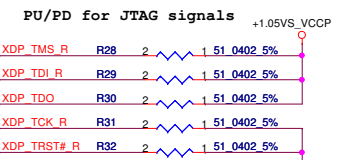


Remove R14(0 ohm) for HW Review demand

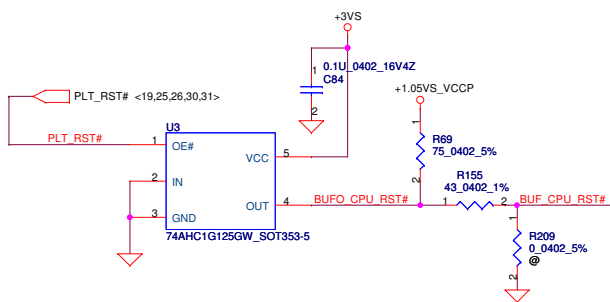
Sandy Bridge_rPGA_Rev0p61



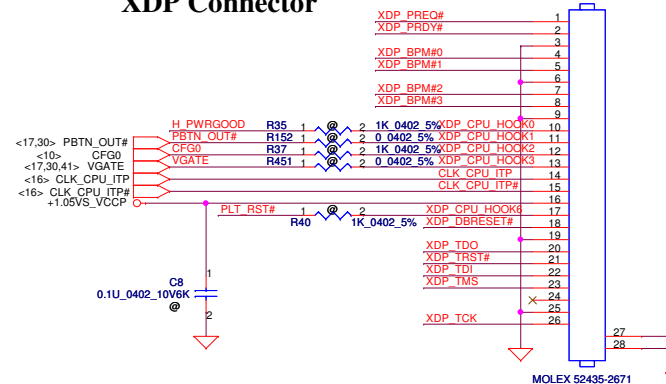
Close to CPU side



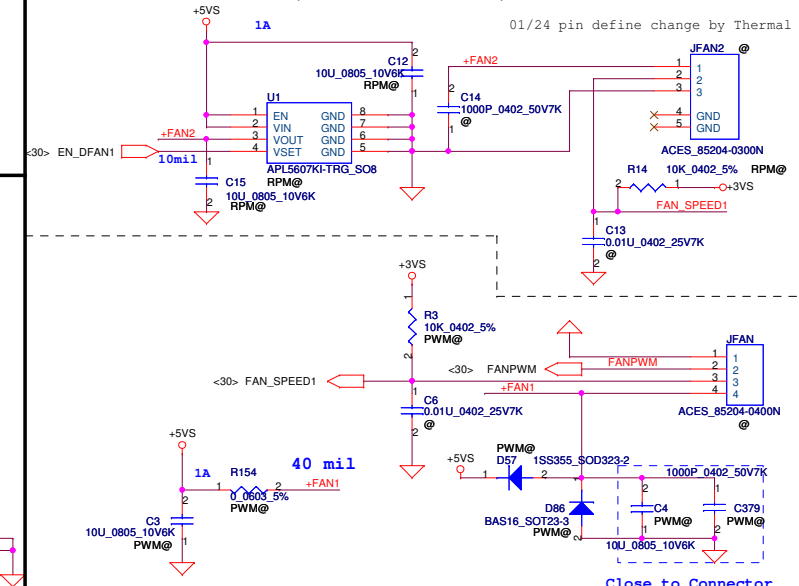
Buffered Reset to CPU



XDP Connector

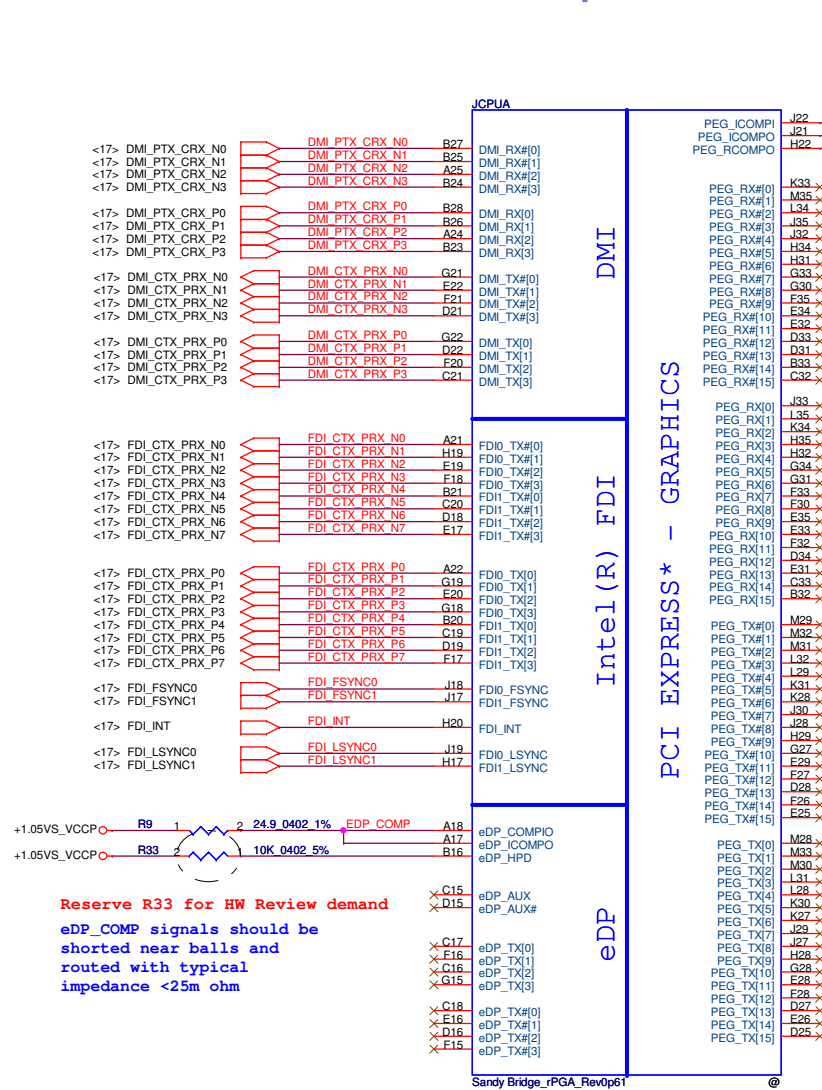


FAN Control Circuit (RPM and PWM)



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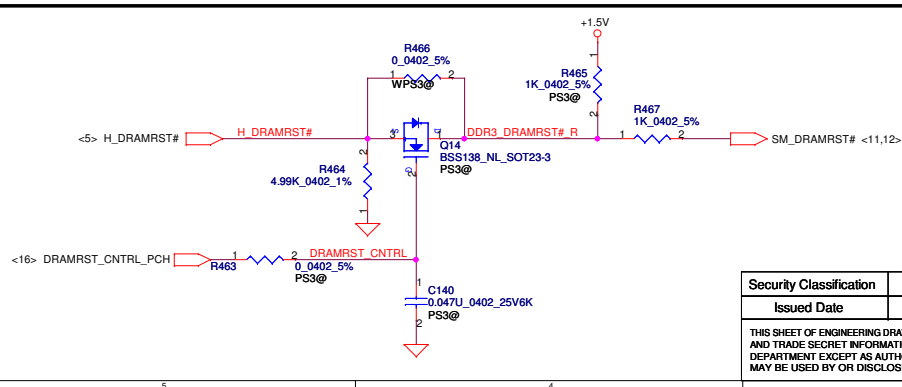
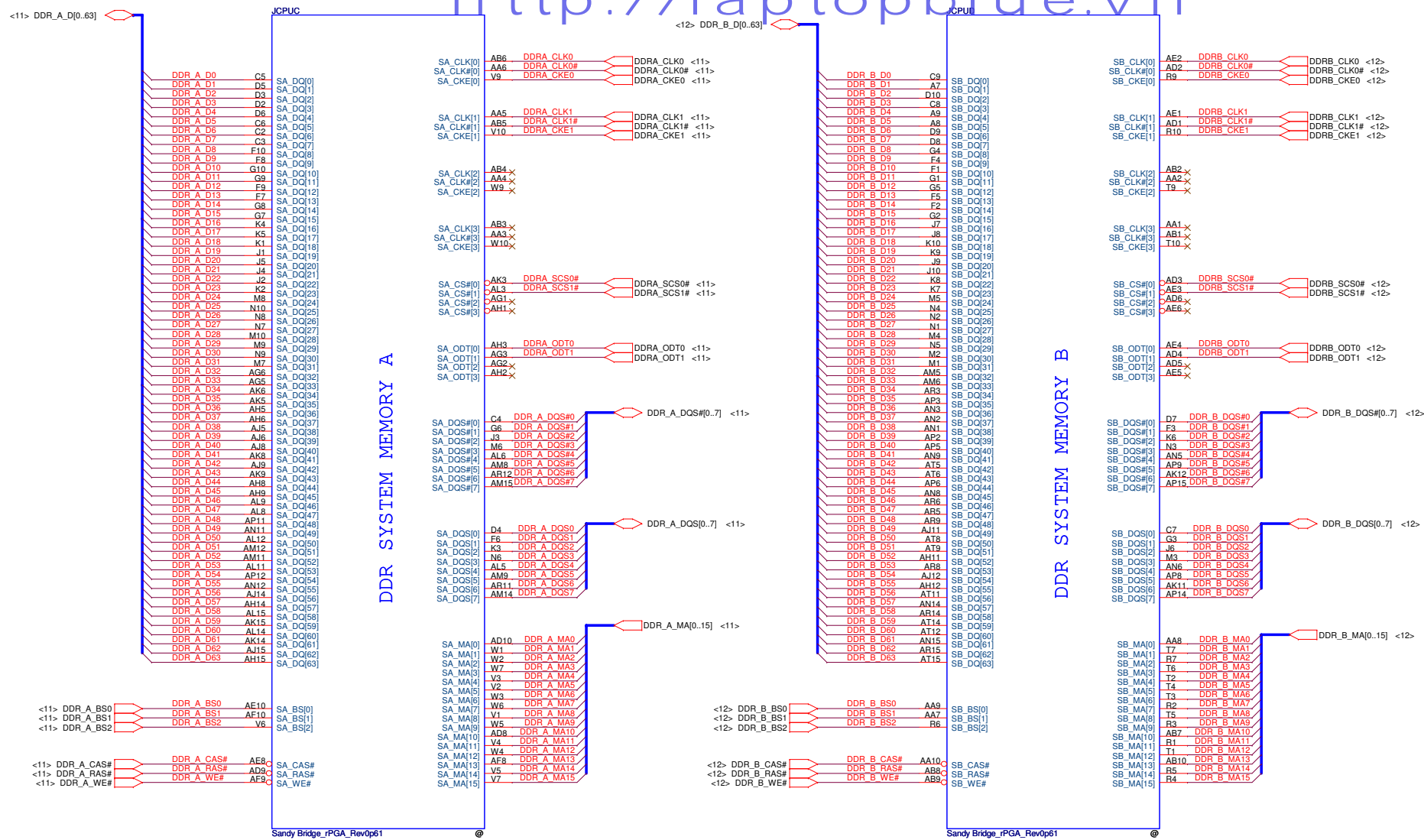
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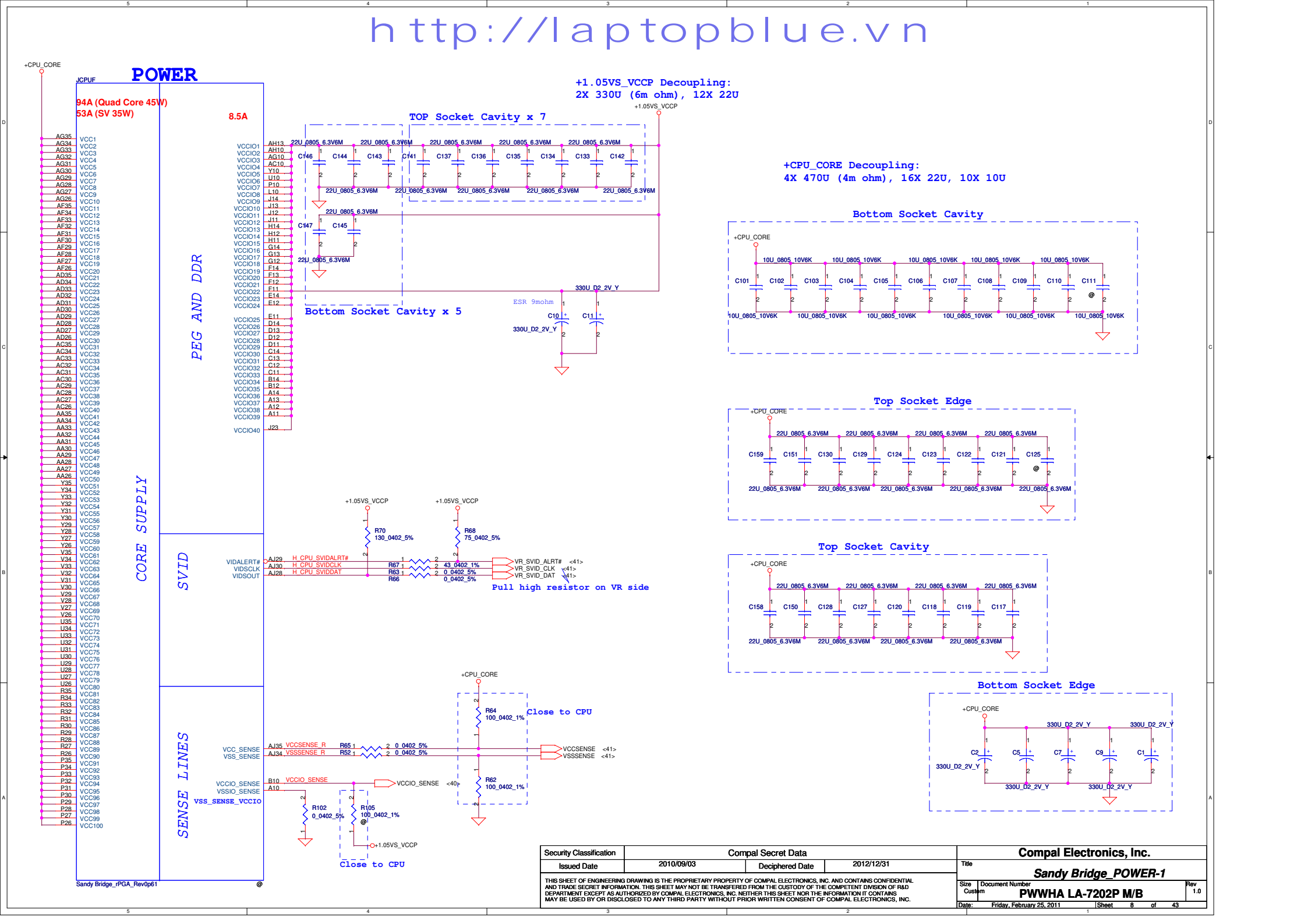
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

Reserve R33 for HW Review demand
 eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

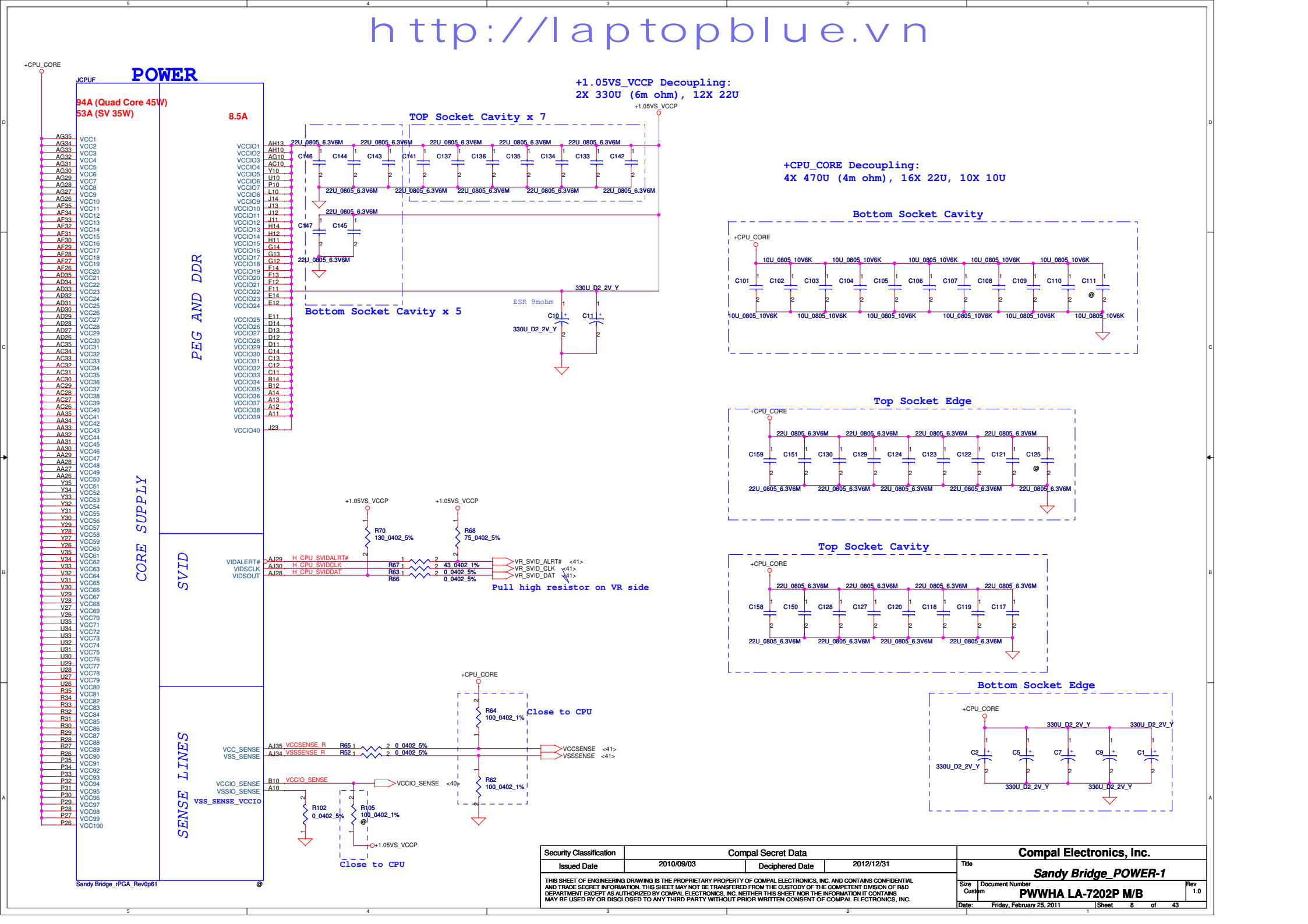
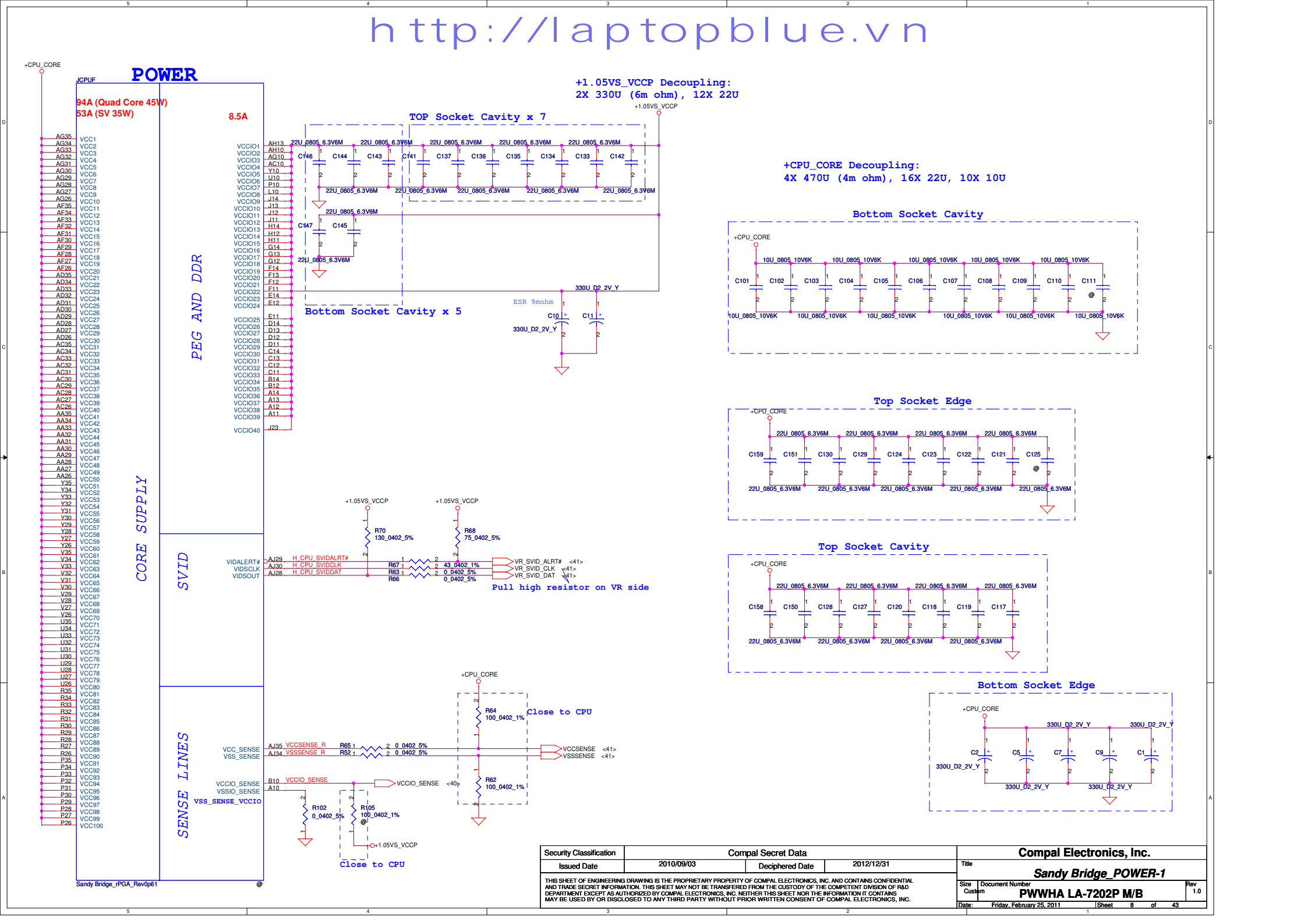
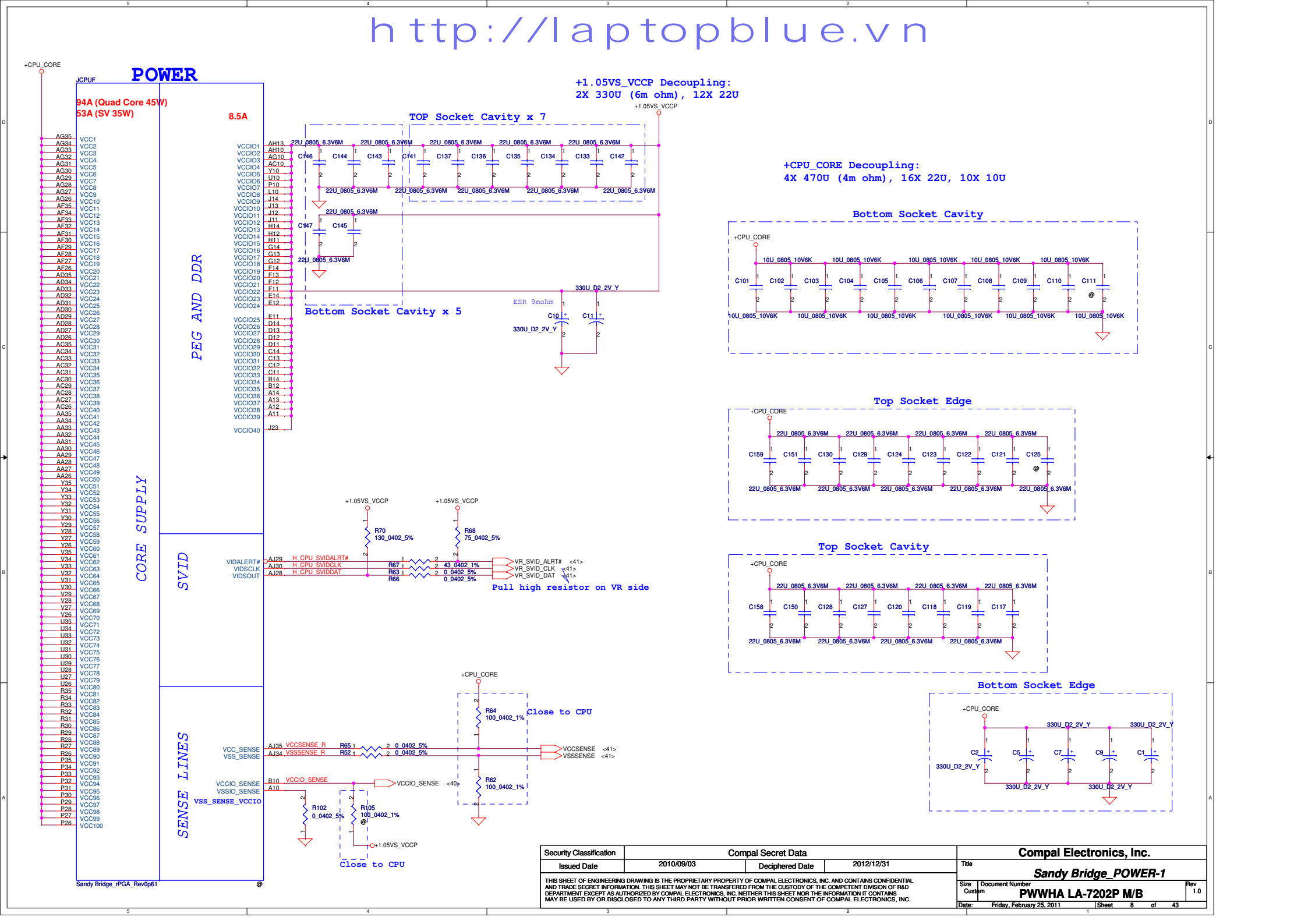
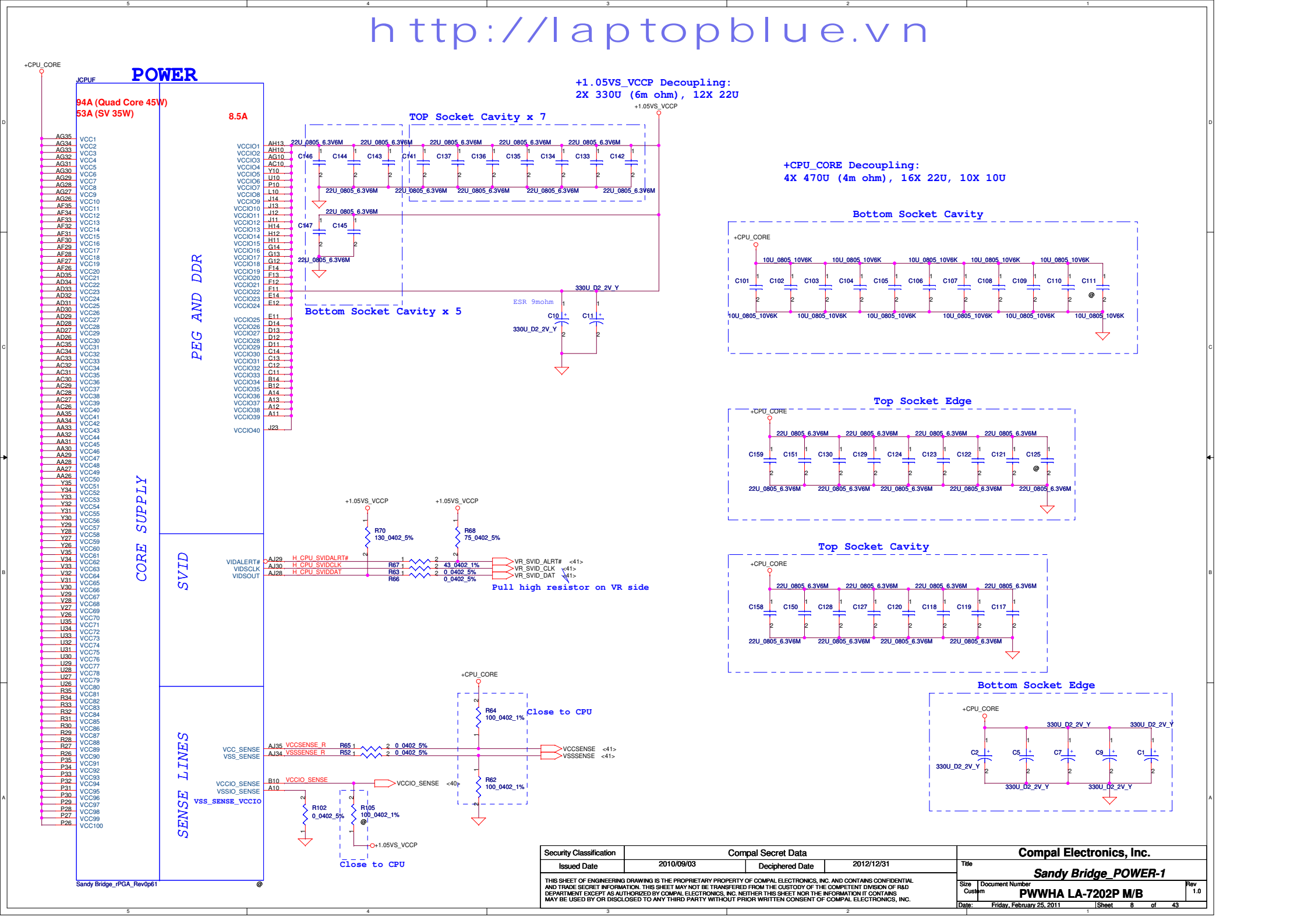
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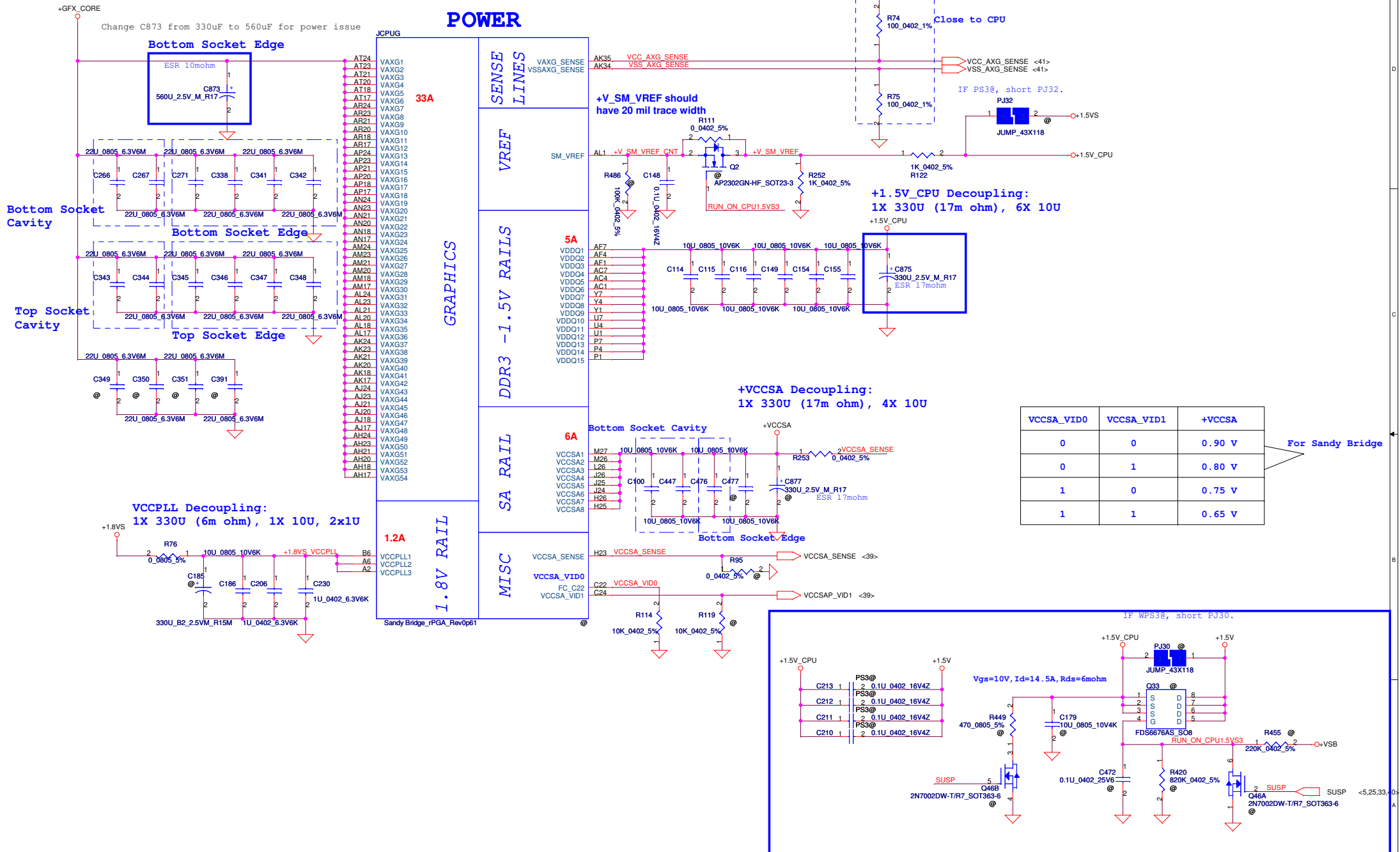


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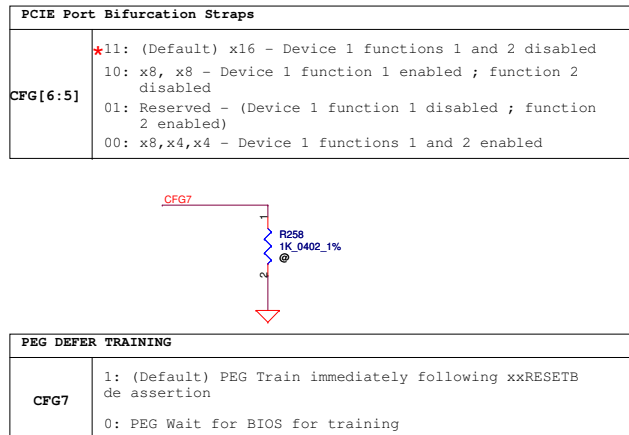
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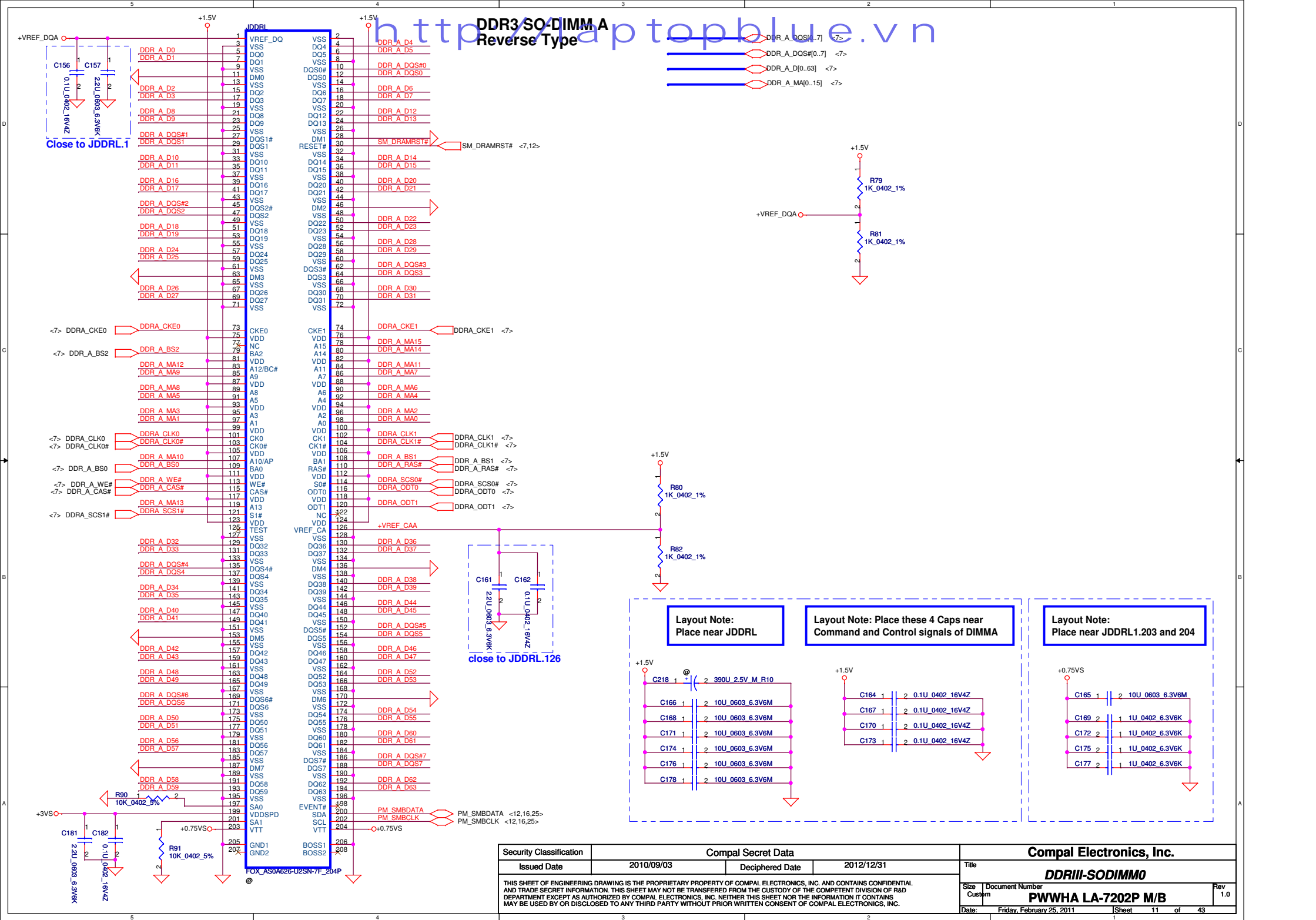
+GFX_CORE Decoupling:
1X 560U (10m ohm), 12X 22U



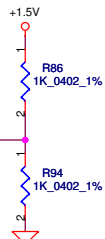
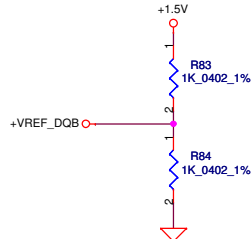
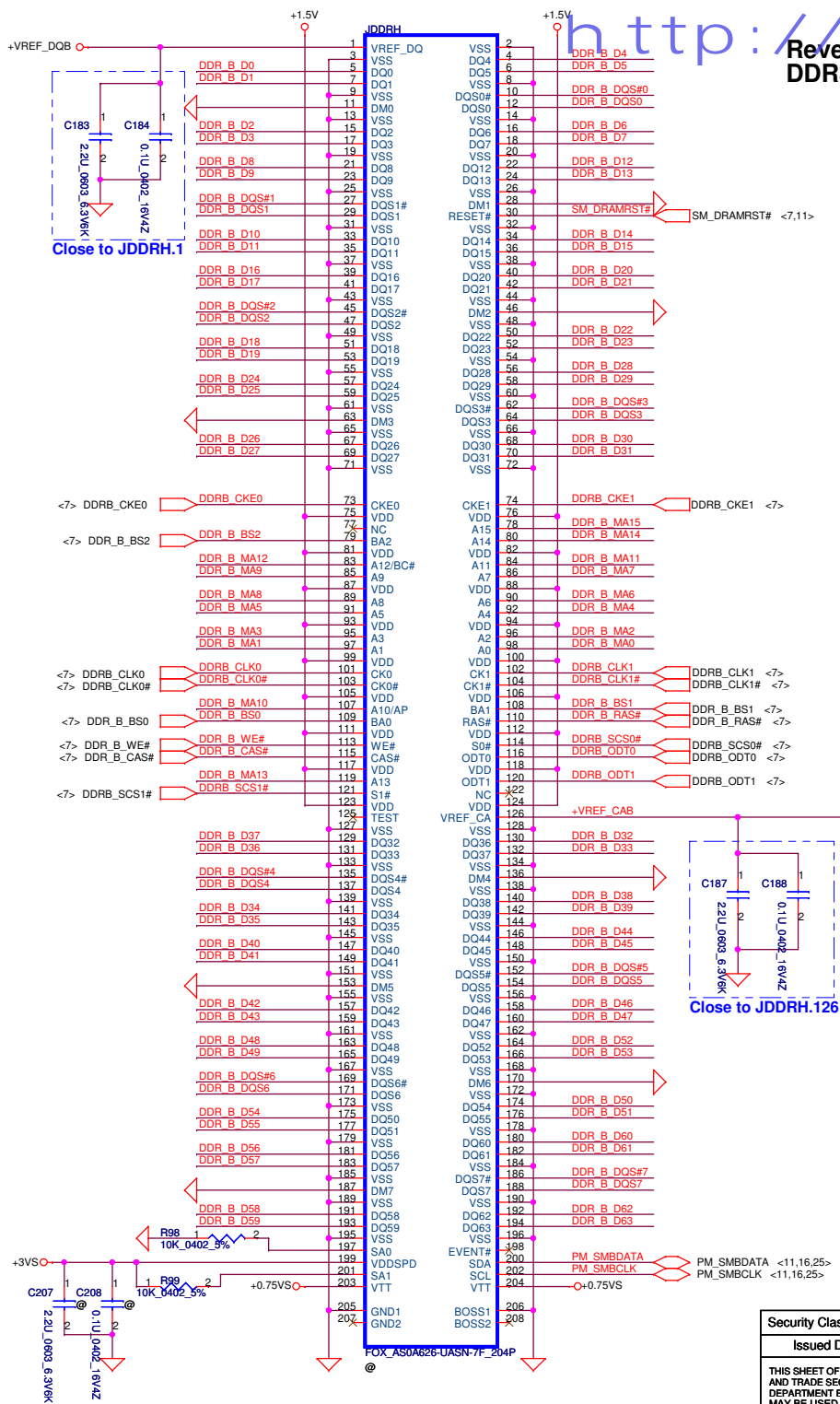
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge





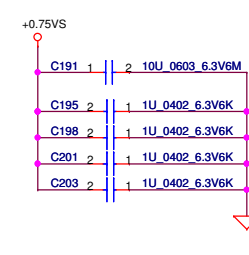
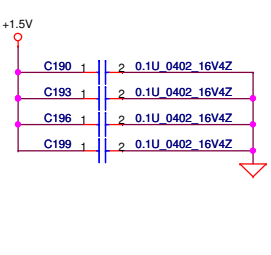
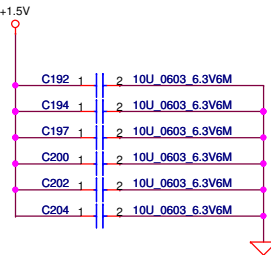
Reverse Type
DDR3 SO-DIMM B



Layout Note:
Place near JDDRH

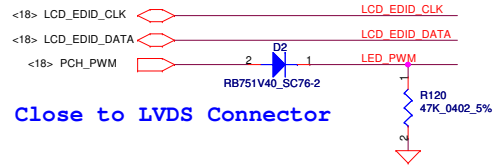
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

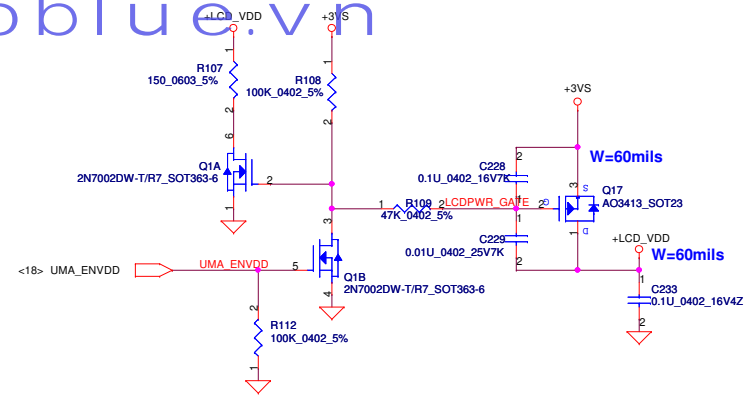
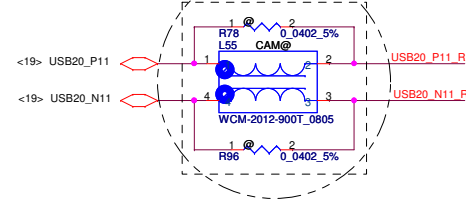


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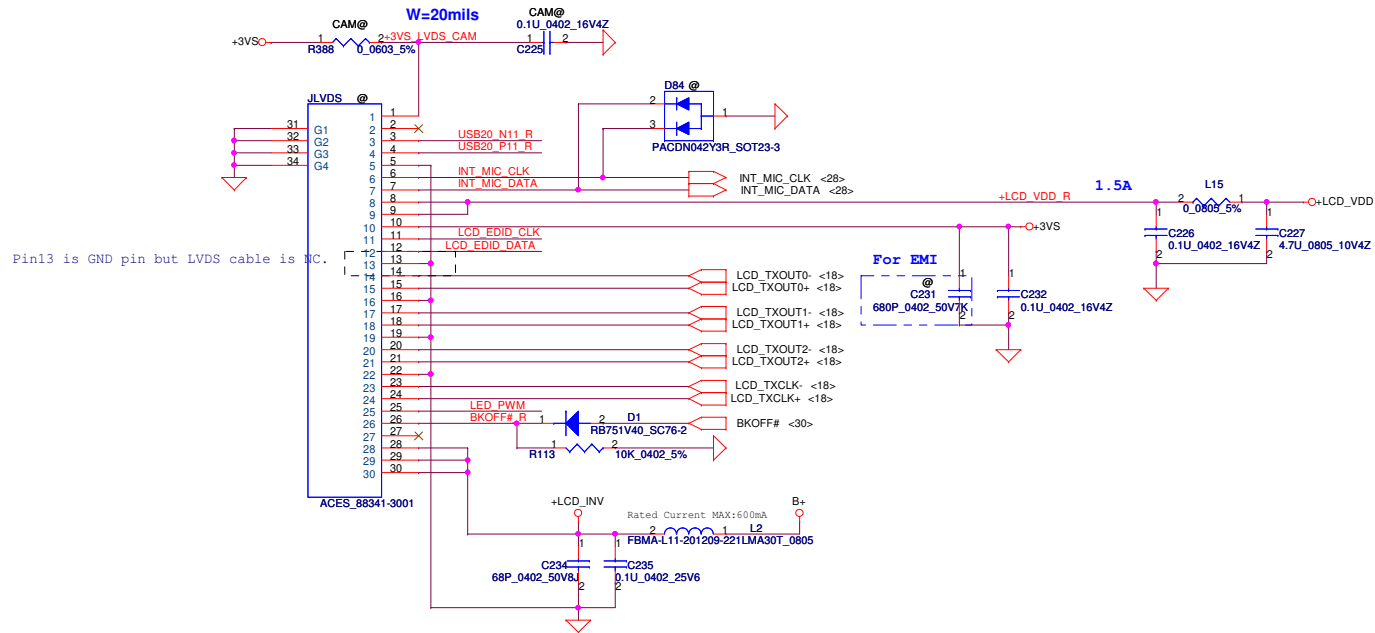
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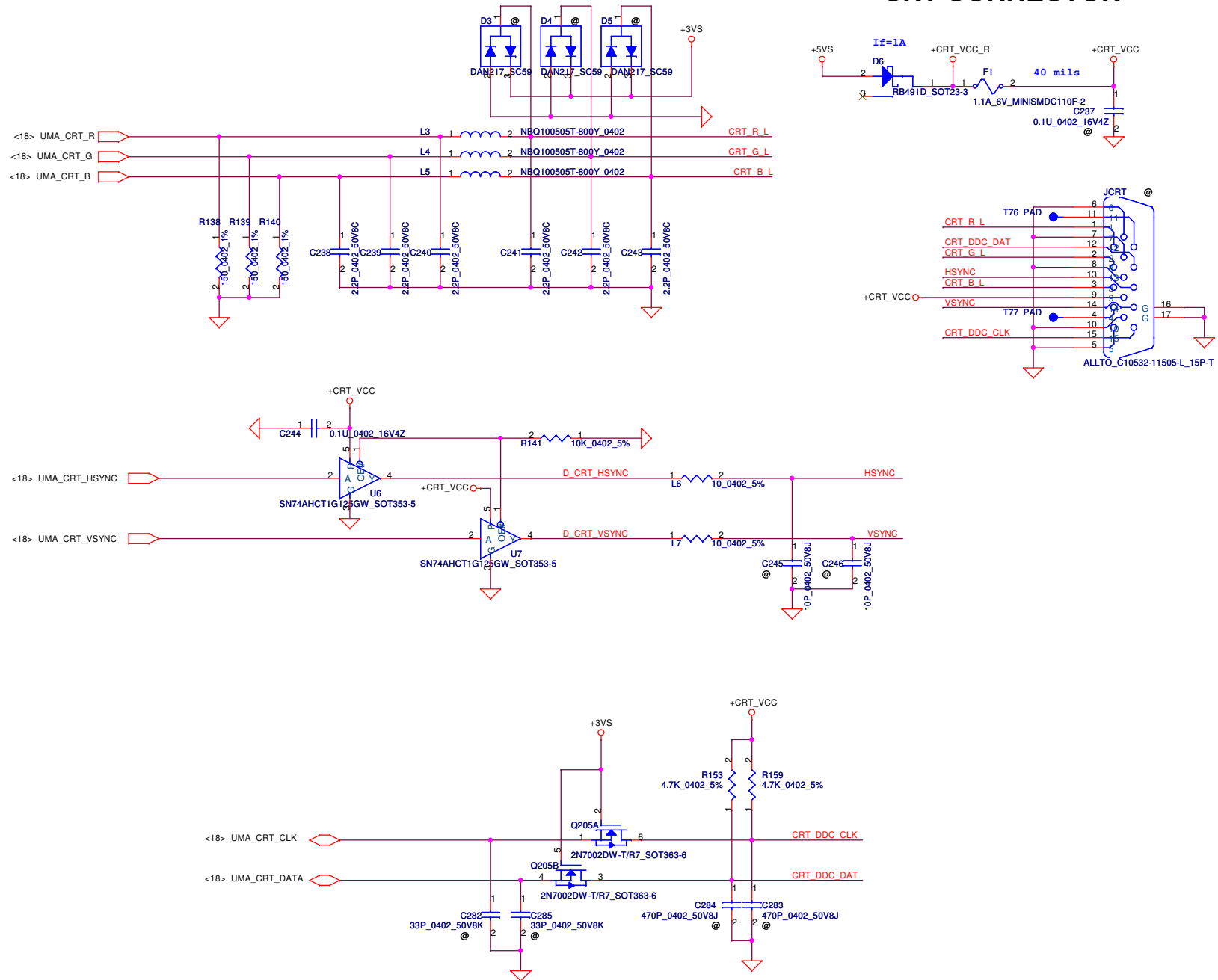
Reserve for EMI request



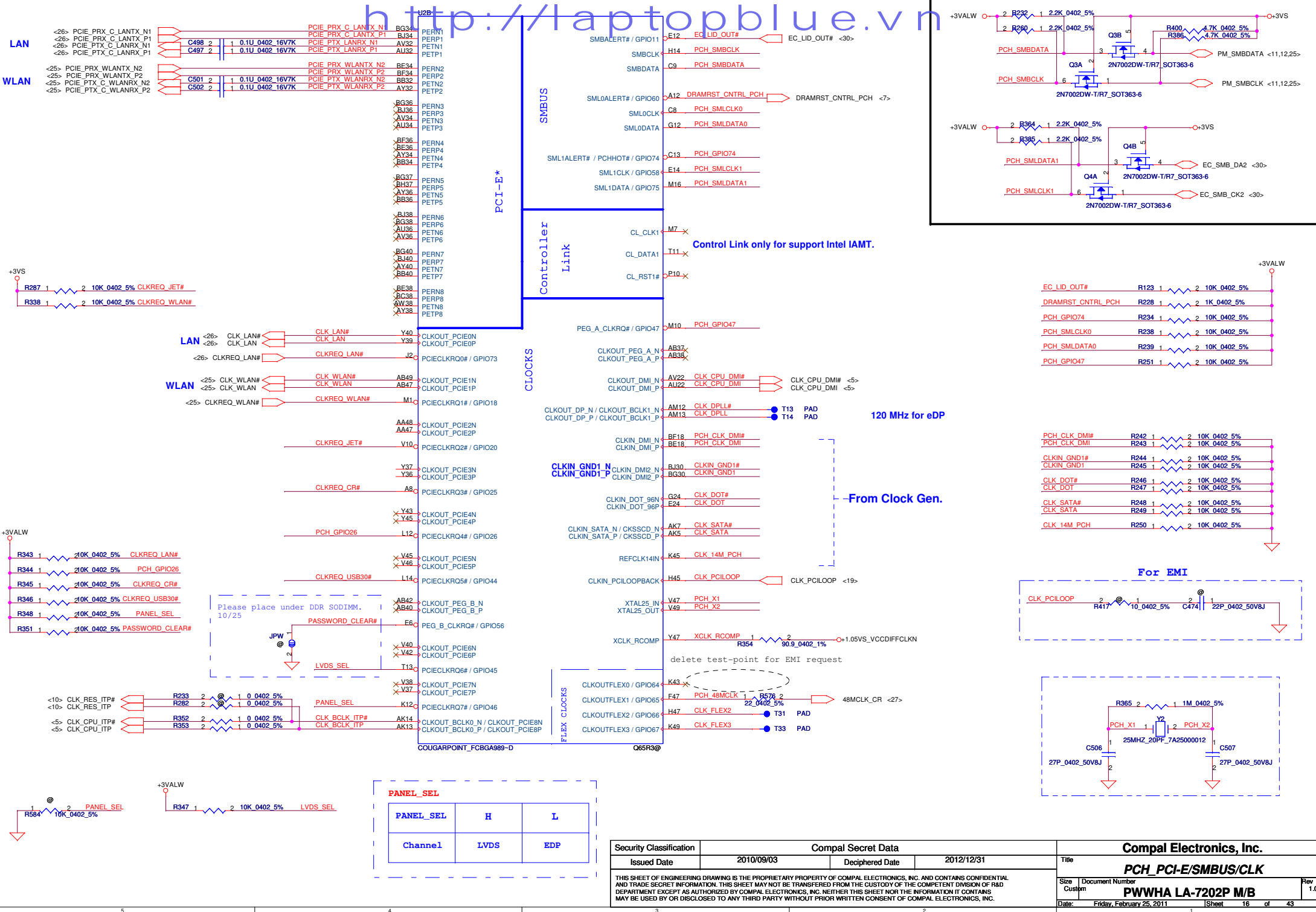
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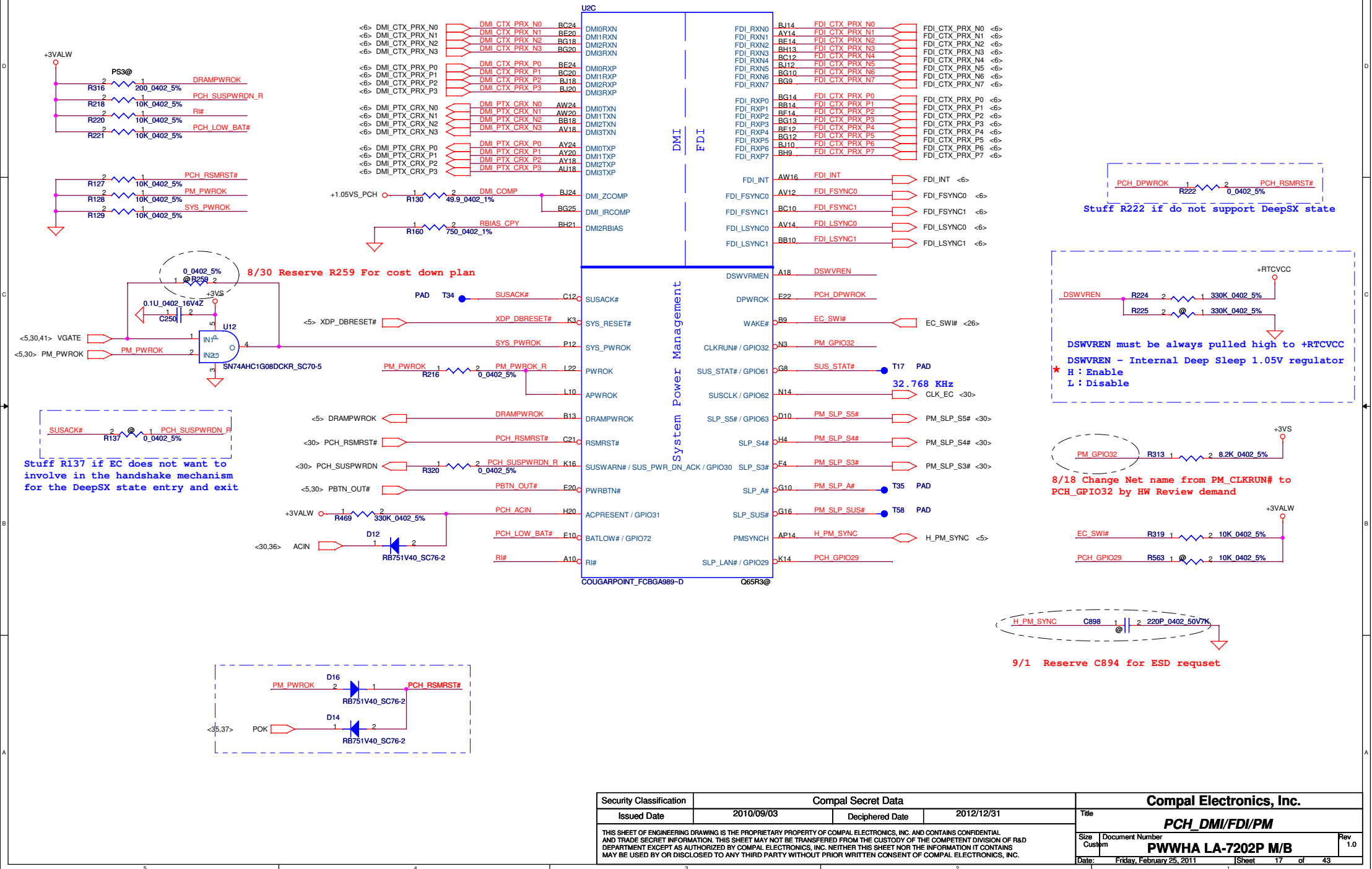


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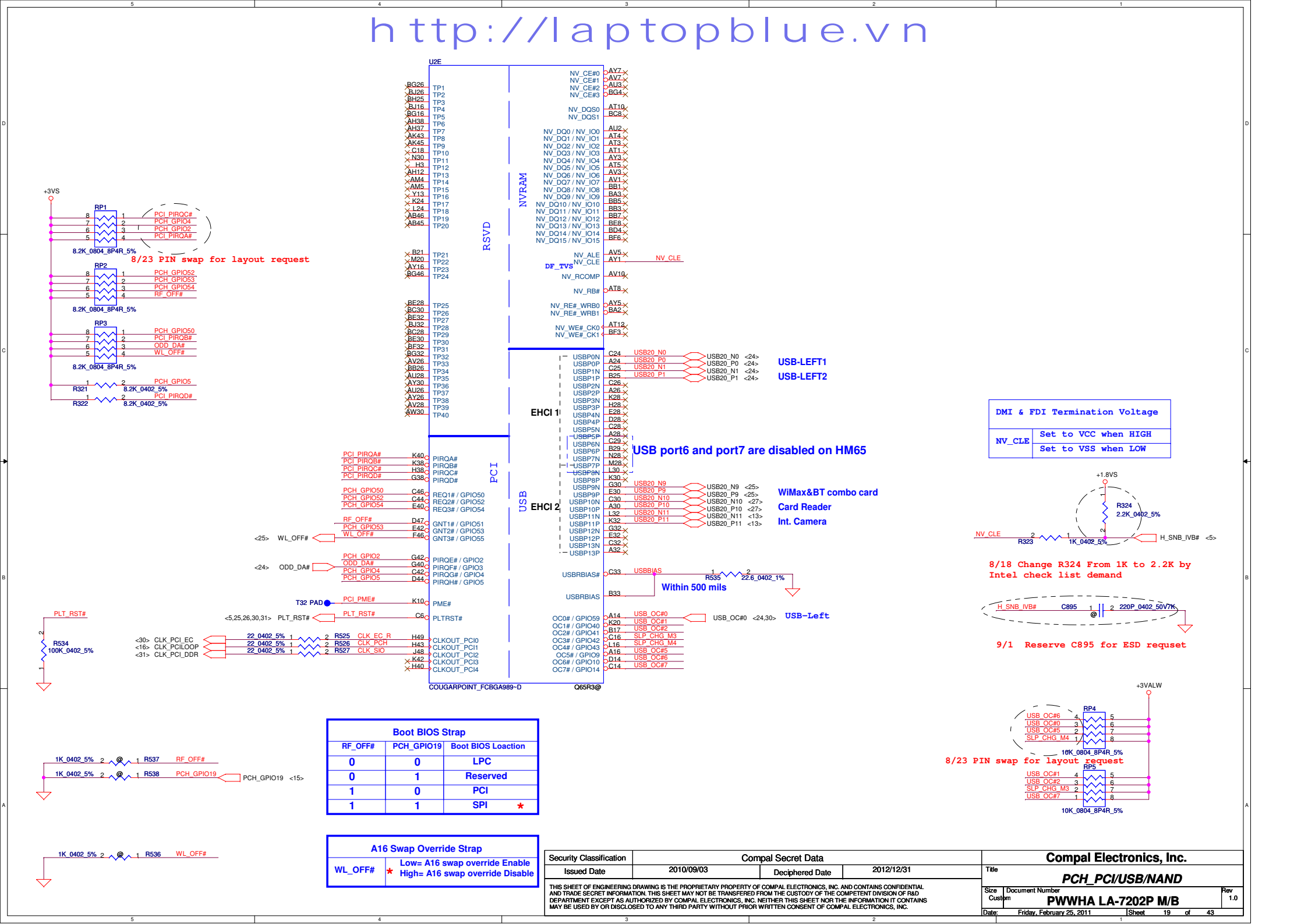
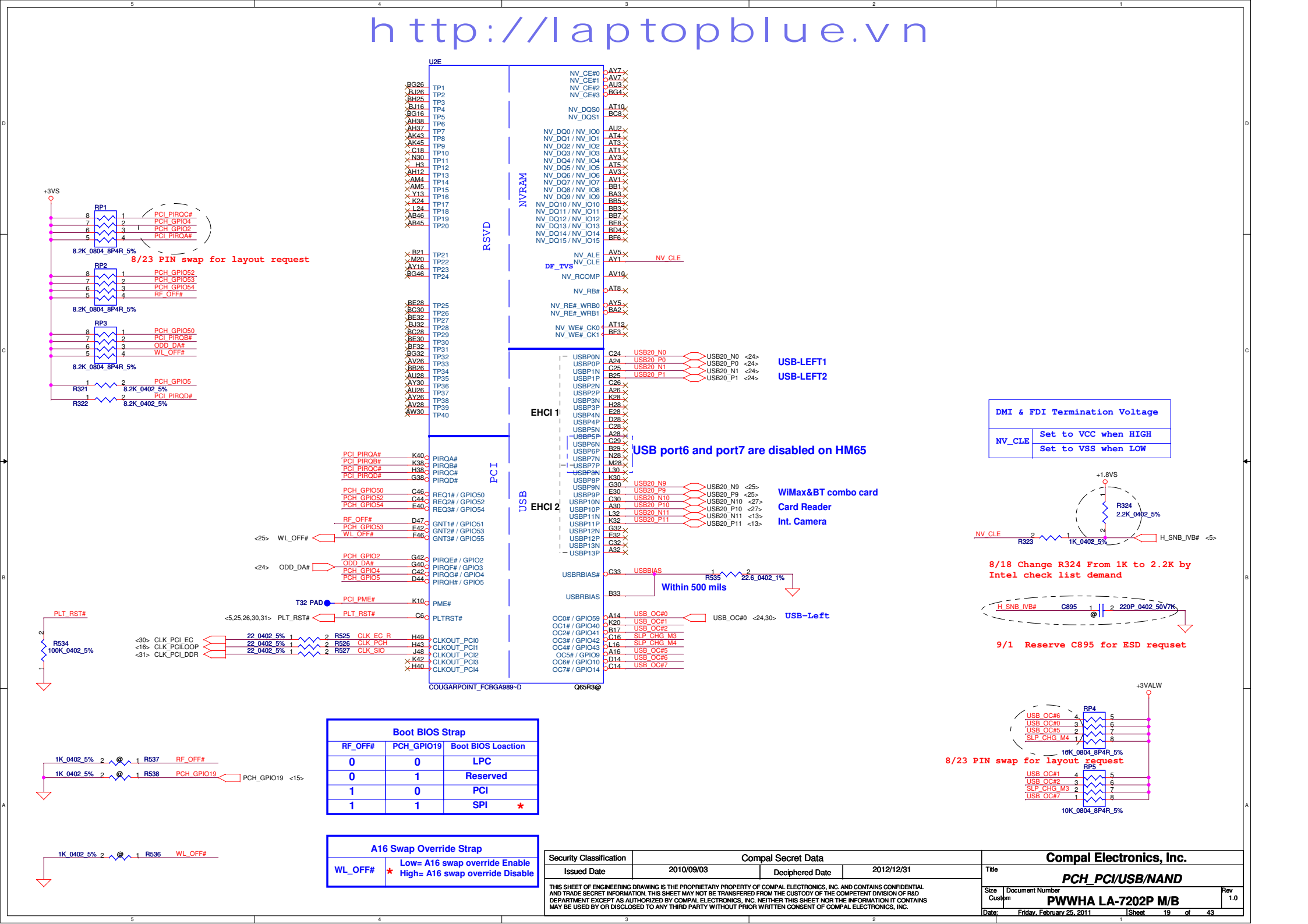
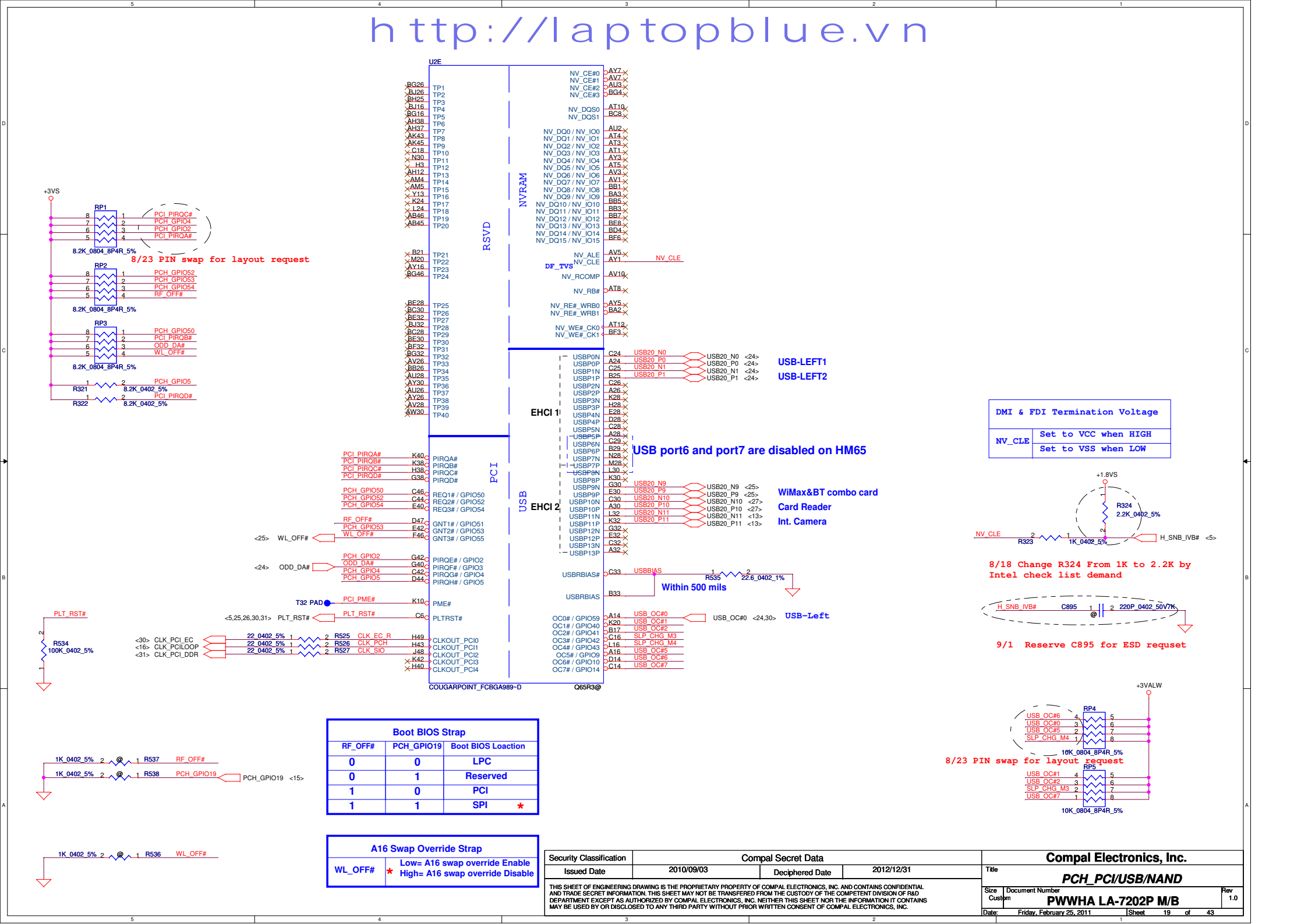
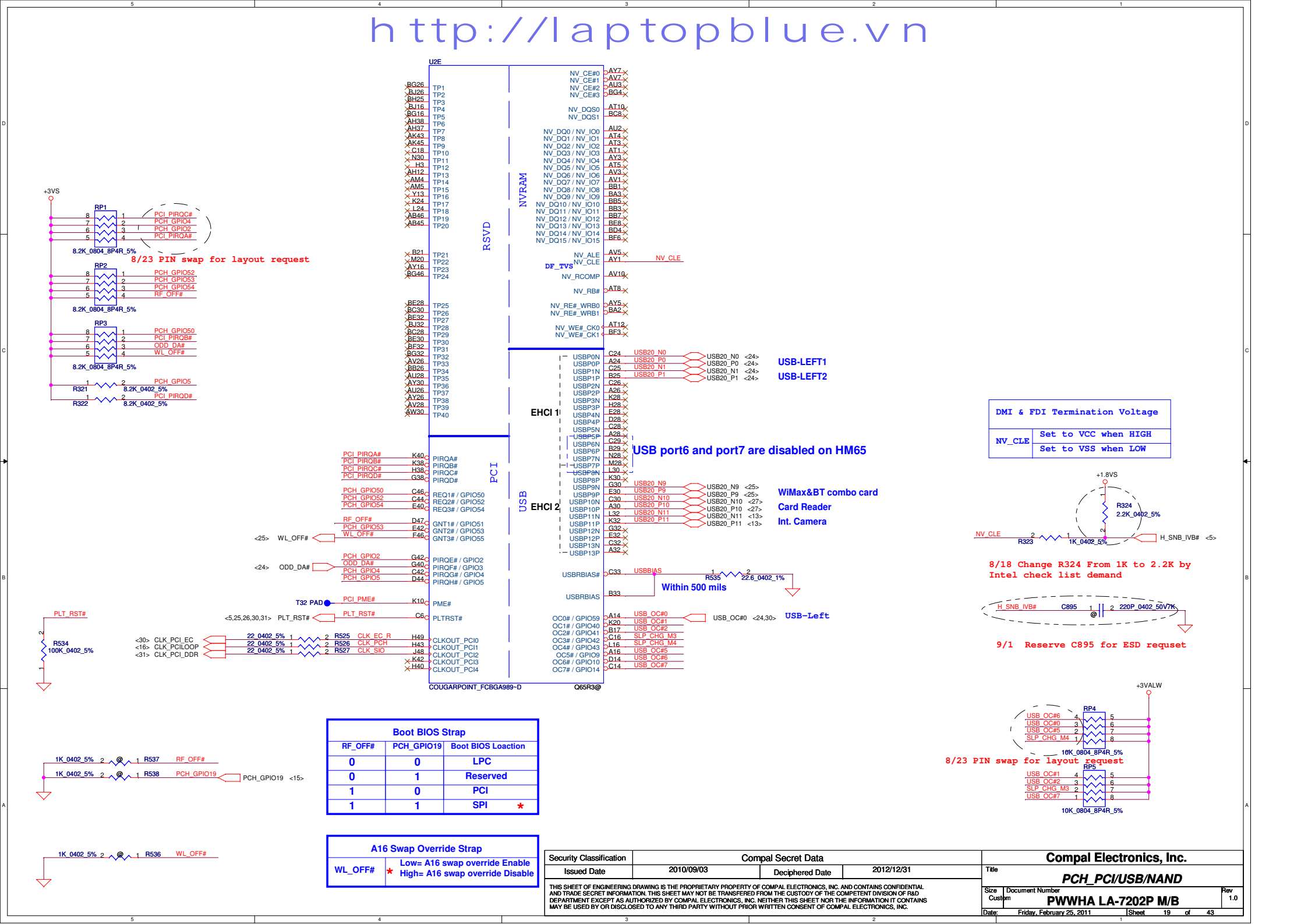


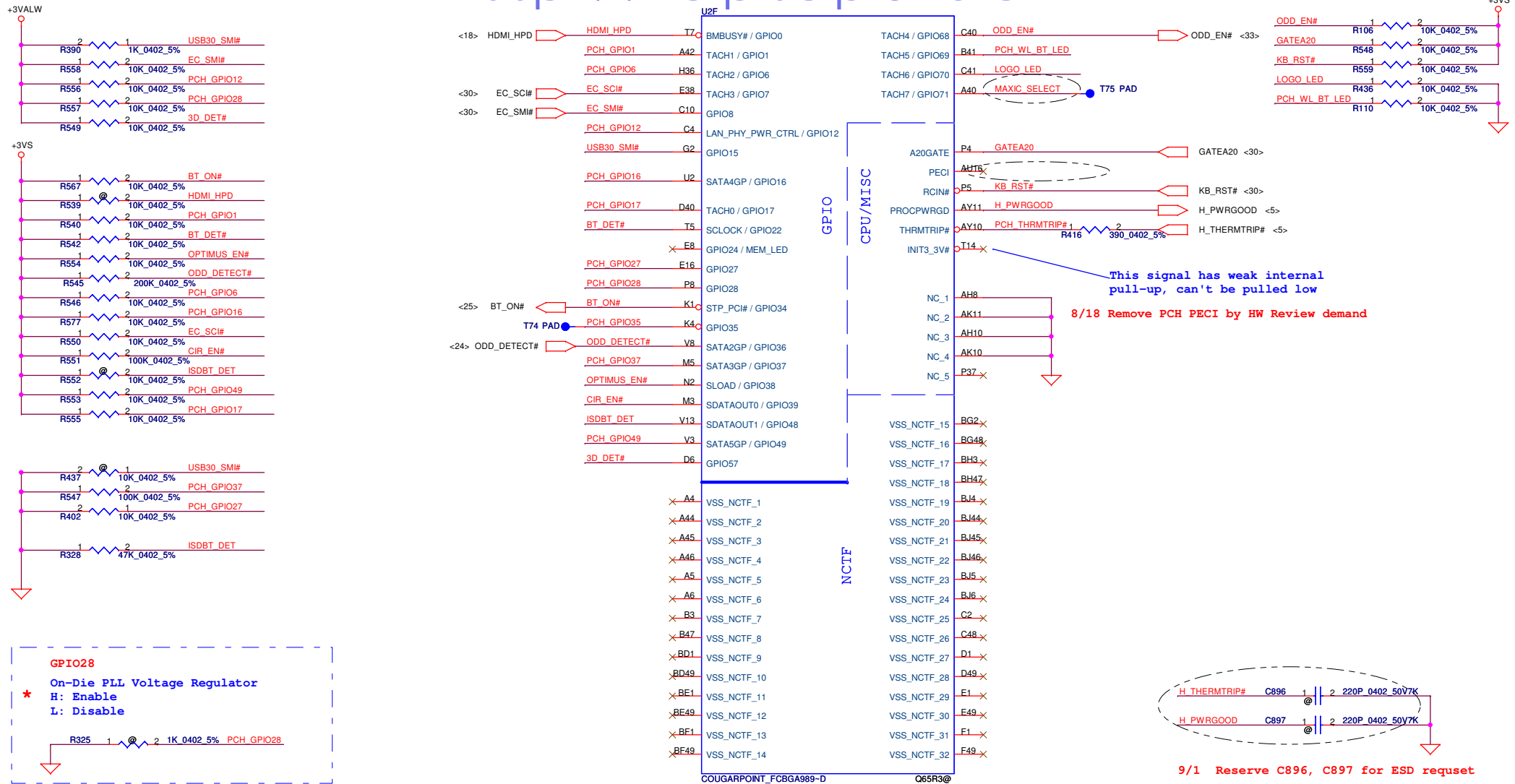
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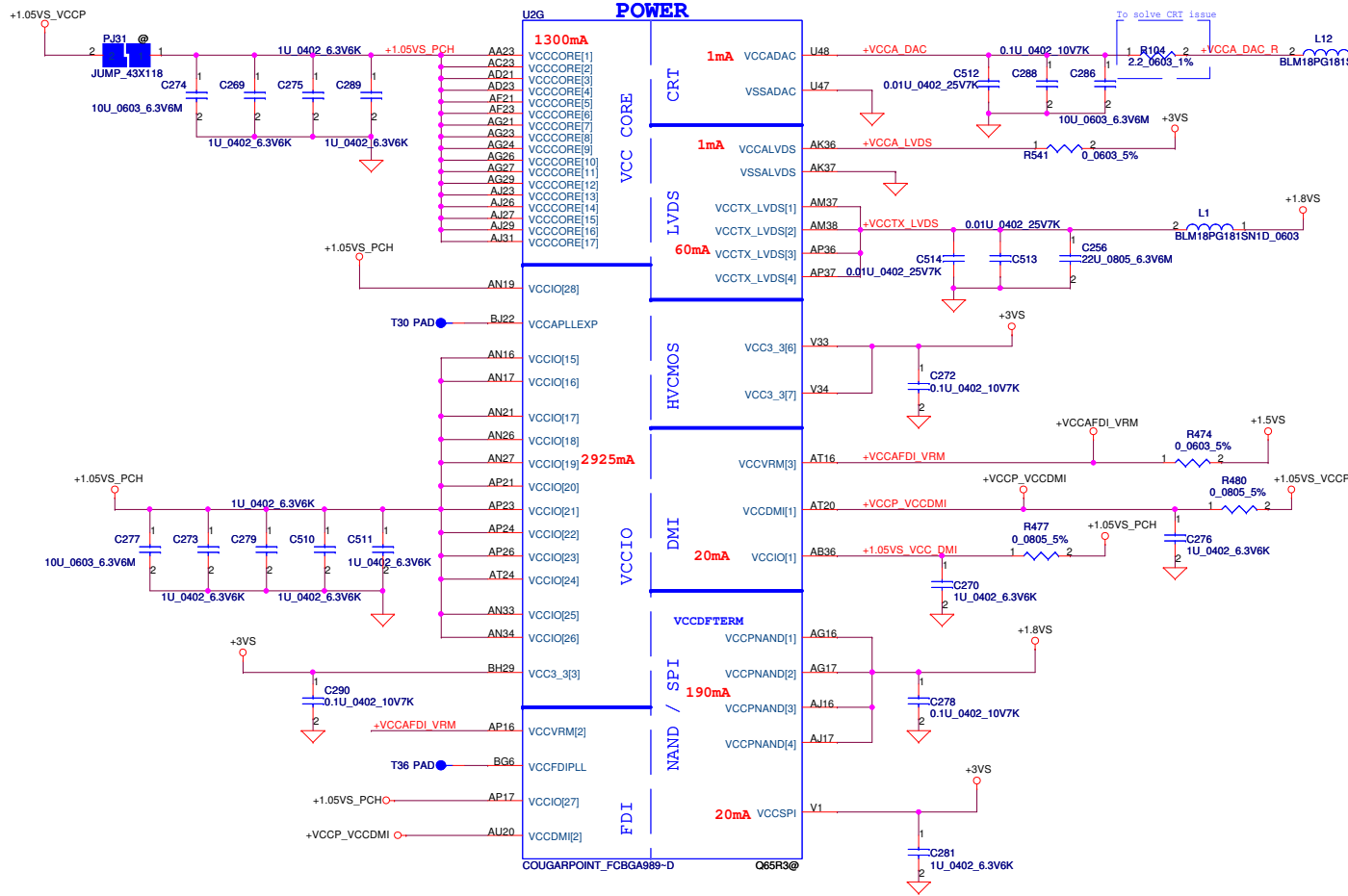
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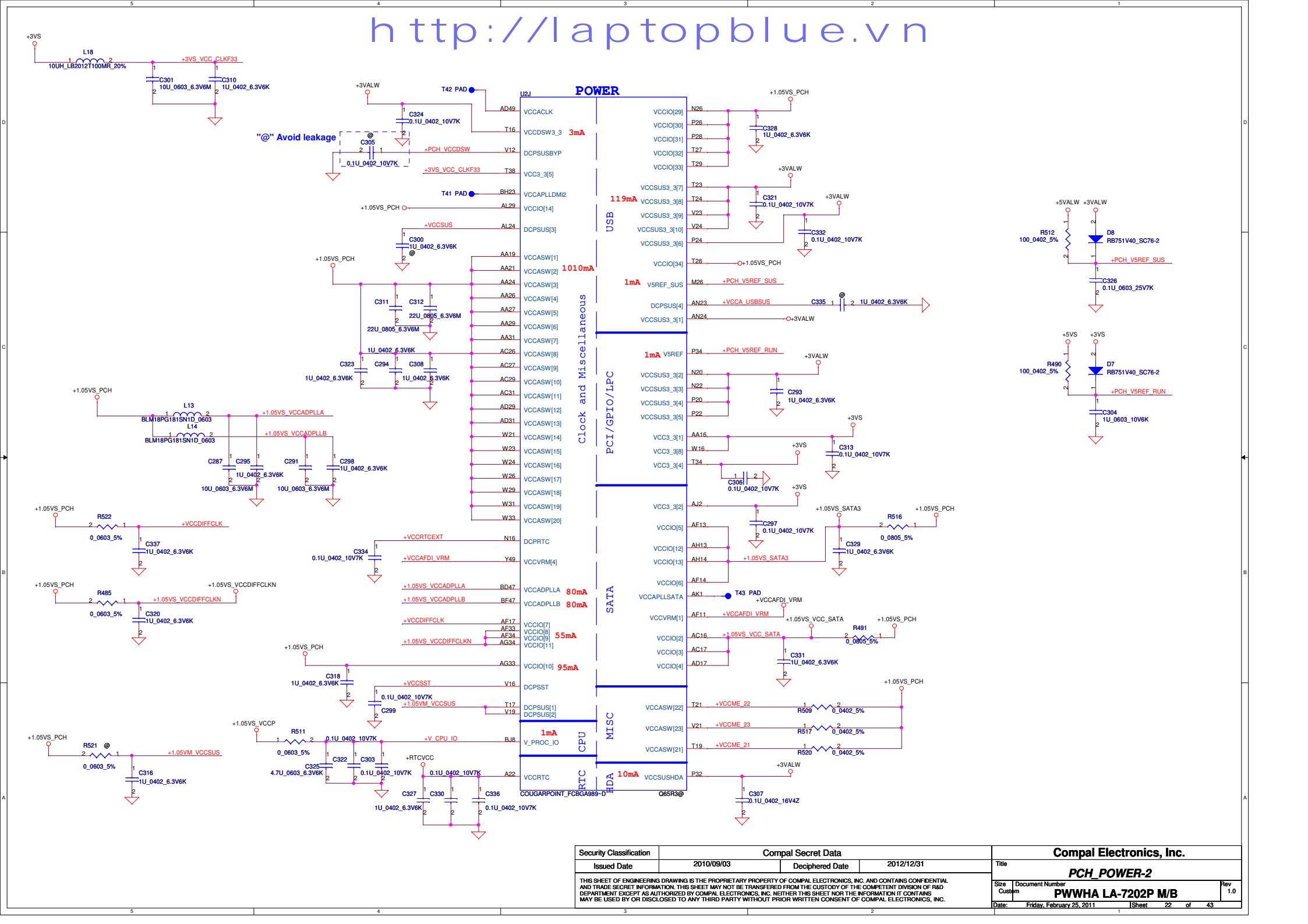
GPIO28
 On-Die PLL Voltage Regulator
 H: Enable
 L: Disable

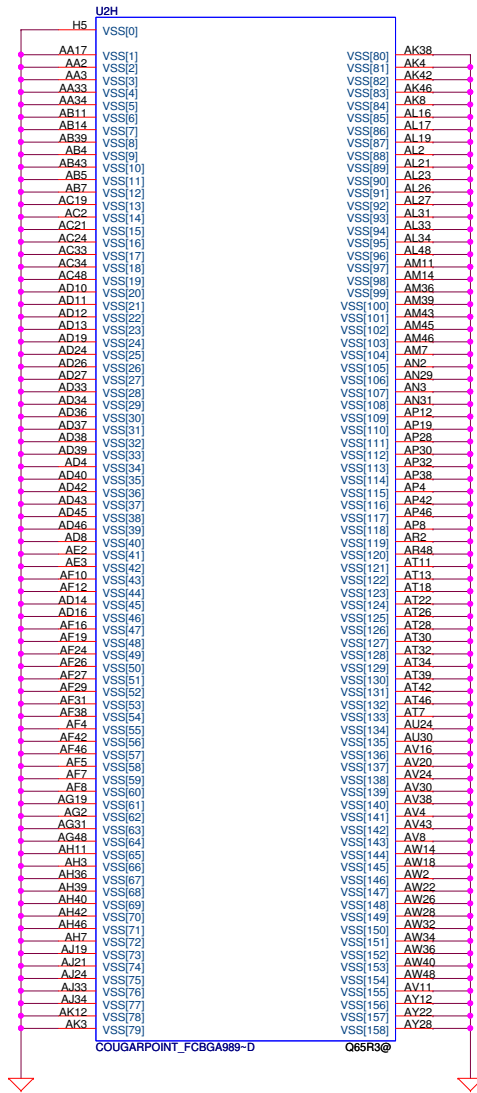
GPIO8
 Integrated Clock Chip Enable (Removed)
 H: Disable
 L: Enable

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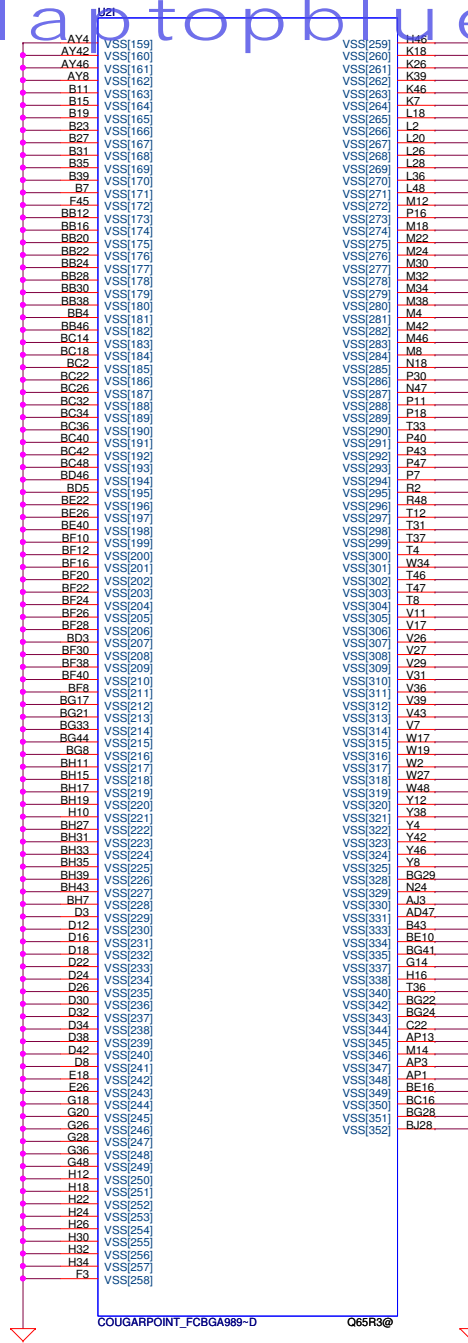
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLL	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

[illegible][illegible]



COUGARPOINT_FCBGA989-D

Q65R3@

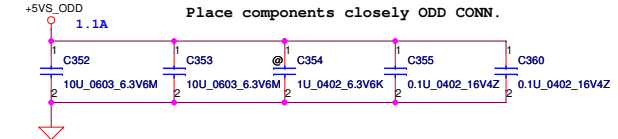
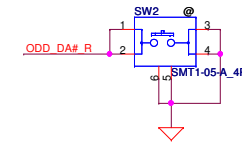
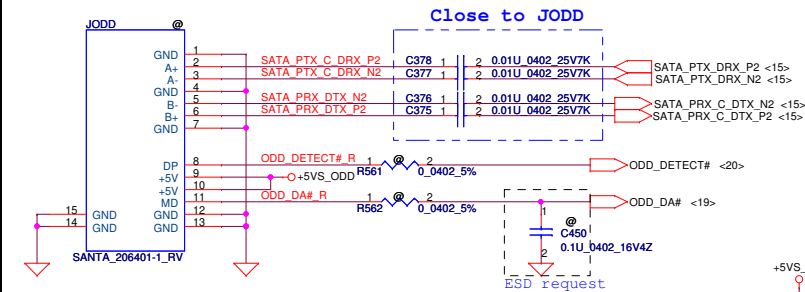


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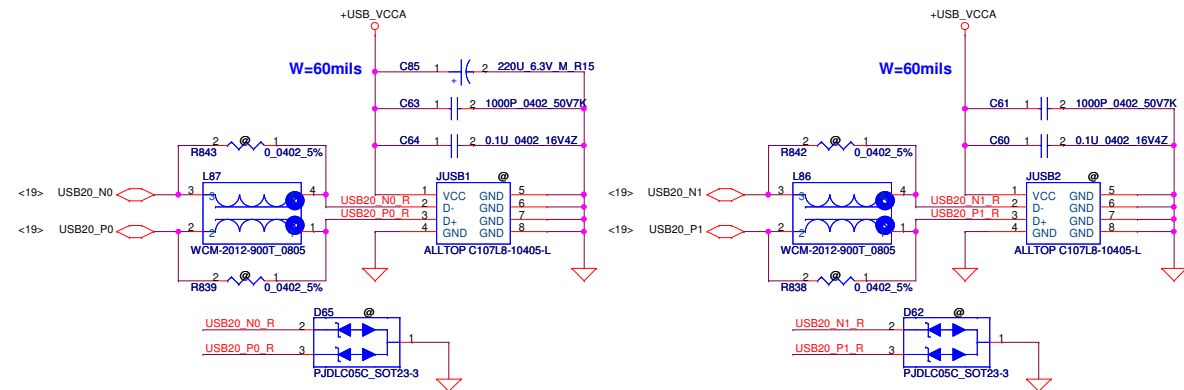
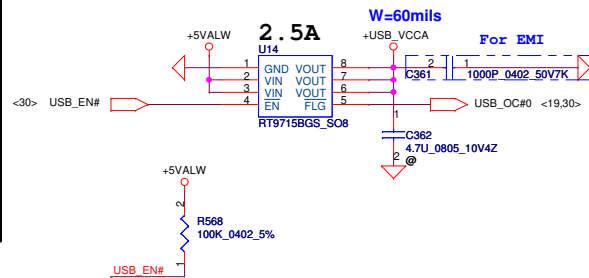
Q65R3@

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Size		Document Number		Rev	
Custom		PWWHA LA-7202P M/B		1.0	
Date:		Friday, February 25, 2011		Sheet 23 of 43	

SATA ODD Conn

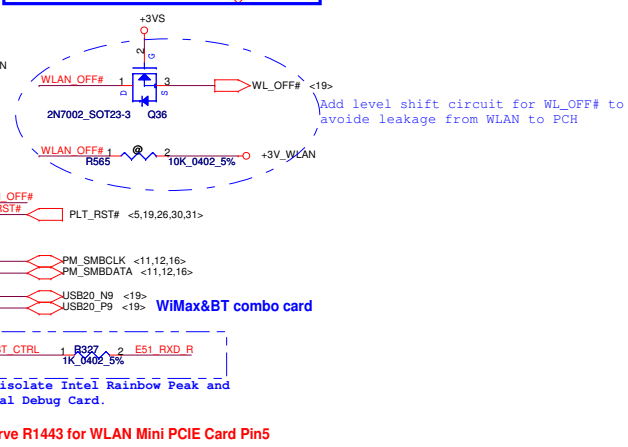
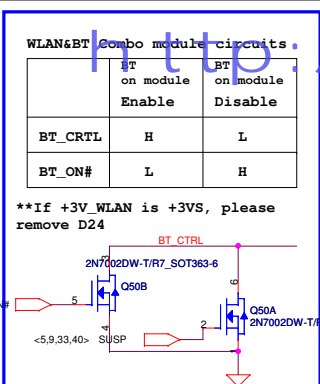


USB Conn. Left Side

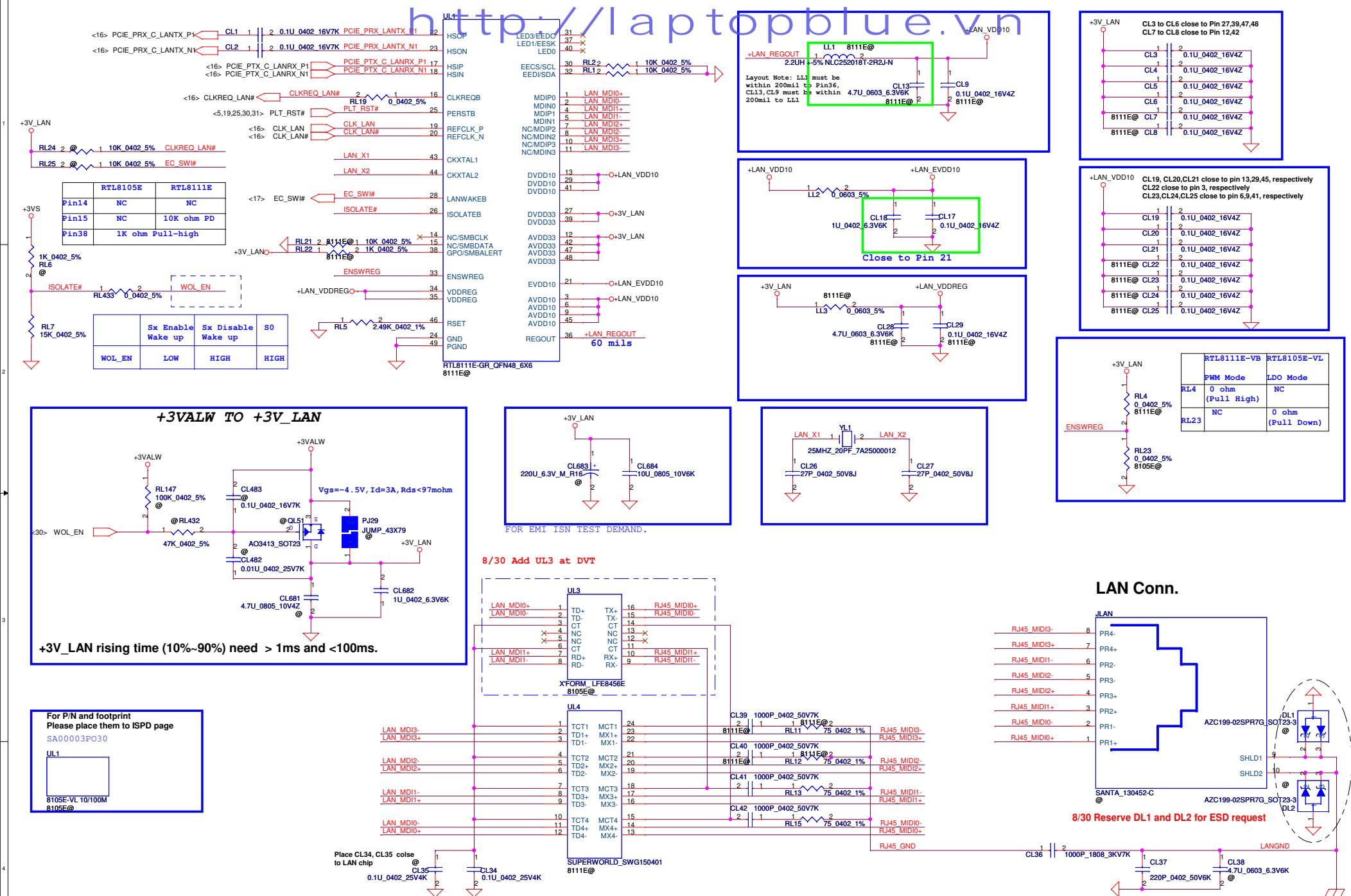


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Size		Document Number		Rev	
		PWWHA LA-7202P M/B		1.0	
Date:		Friday, February 25, 2011		Sheet 24 of 43	

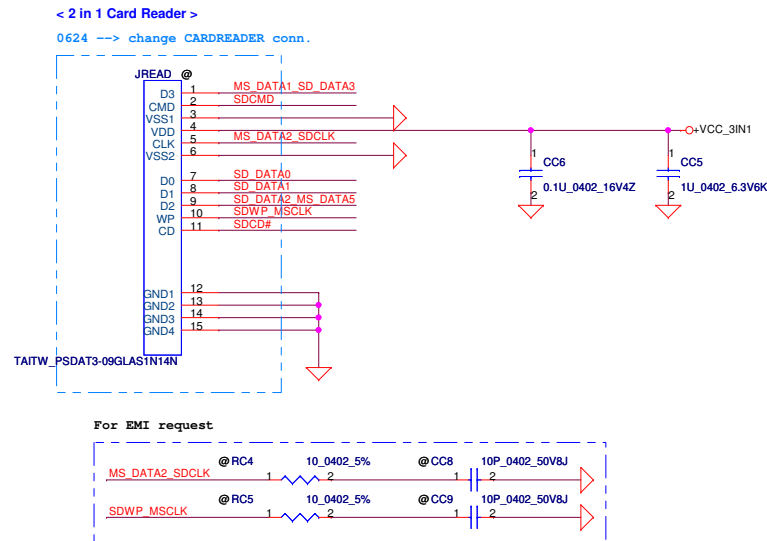
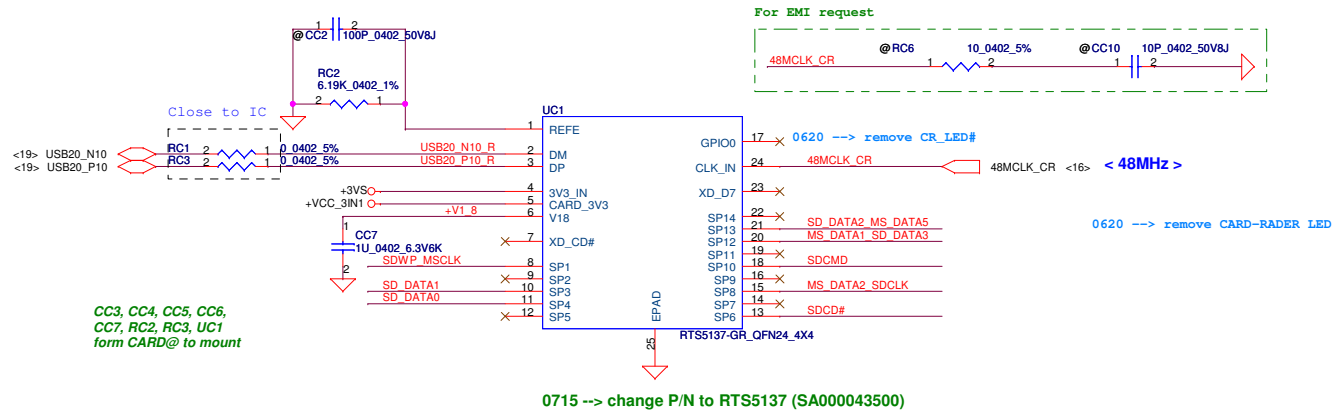
WLAN&BT Combo module circuits.



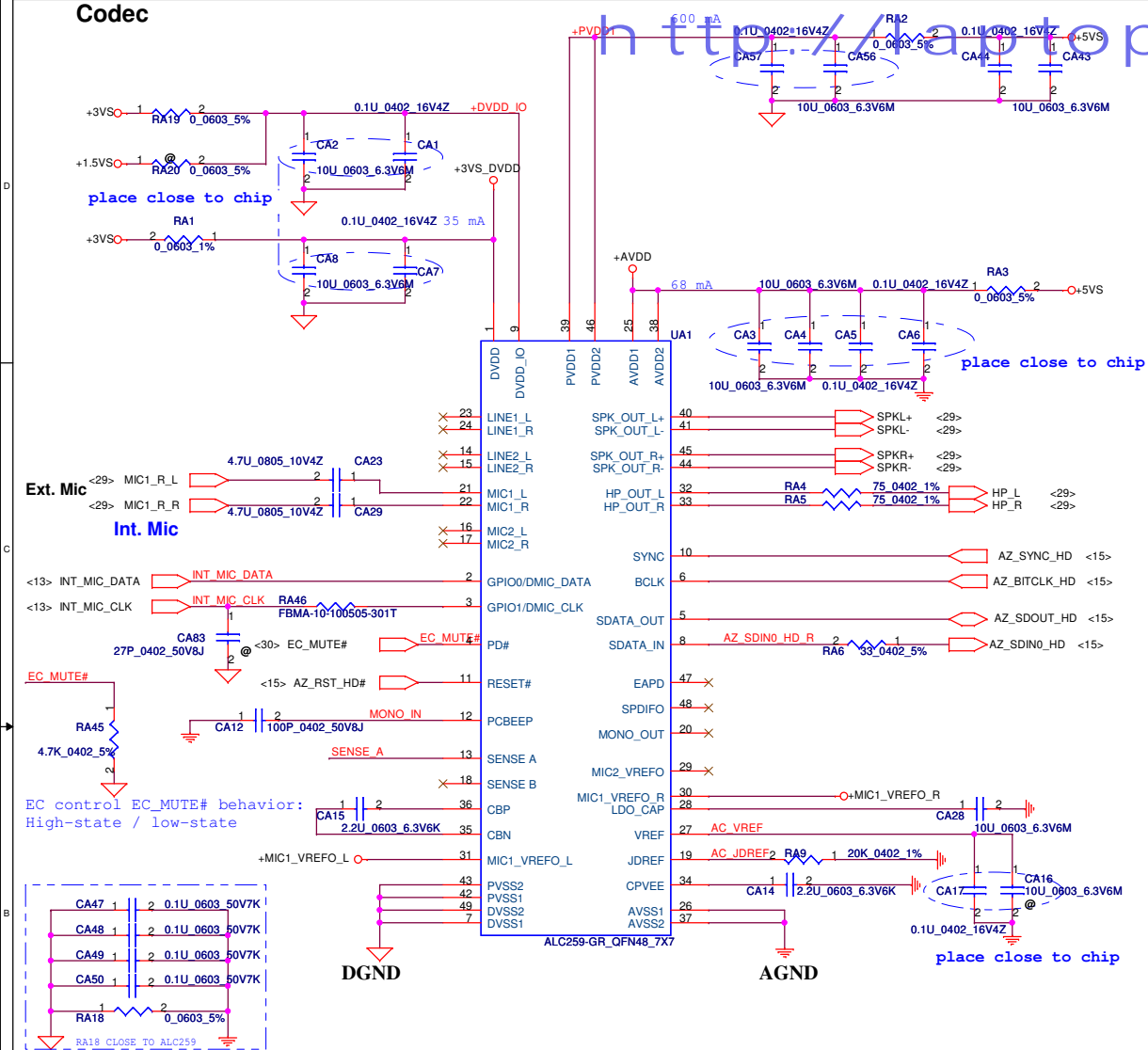
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title		
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				Size	Document Number	Rev
				PWWHA LA-7202P M/B		
Date:	Friday, February 25, 2011	Sheet	25	of	43	



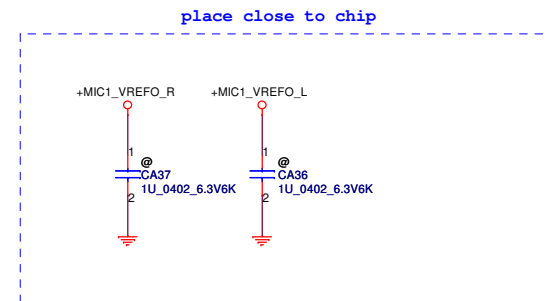
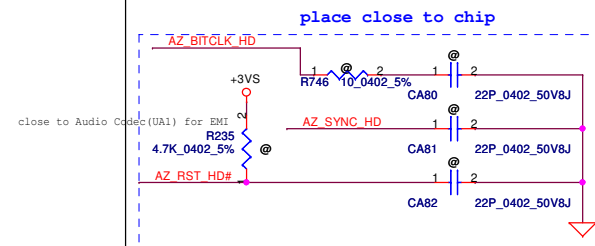
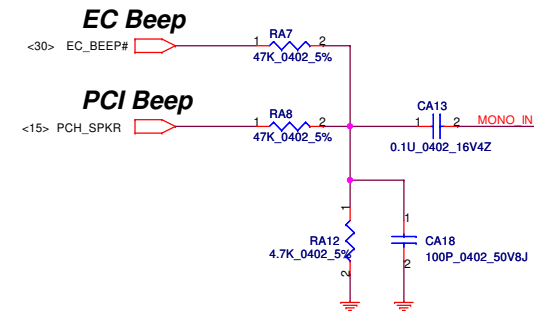
Security Classification		Compal Secret Data		Compal Electronics, Inc. PCle-LAN-RTL8105E/8111E	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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				Document Number	1.0
				PWWHA LA-7202P M/B	
Date:	Friday, February 25, 2011	Sheet	26	of	43



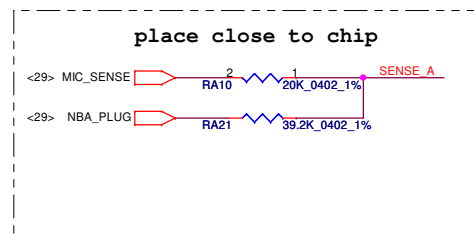
Codec



Beep sound



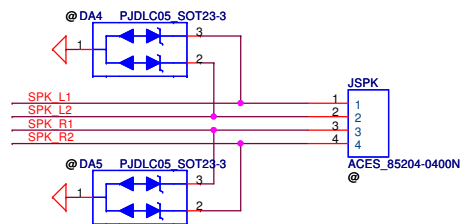
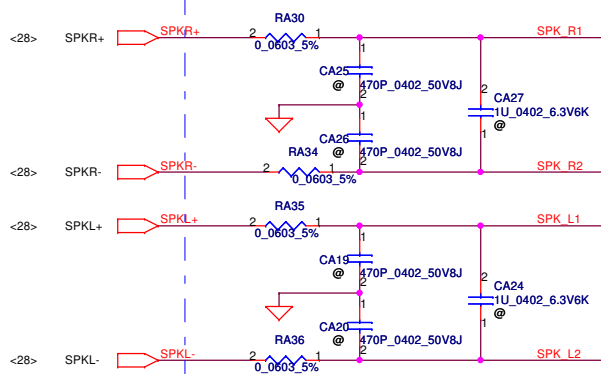
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



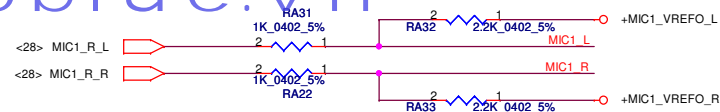
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title HDA-ALC259		
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				PWWHA LA-7202P M/B		
				Date:	Friday, February 25, 2011	[Sheet 28 of 43]

Speaker Connector

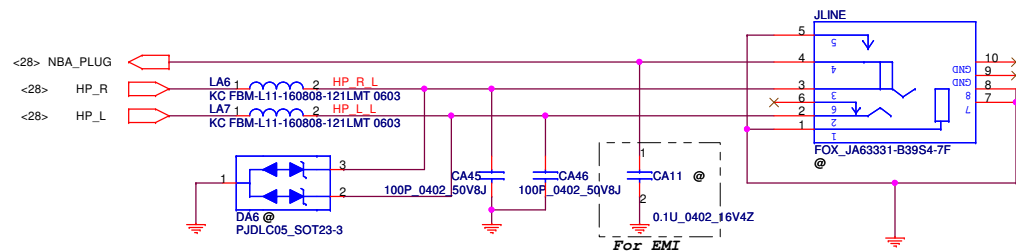
placement near Audio Codec UA1



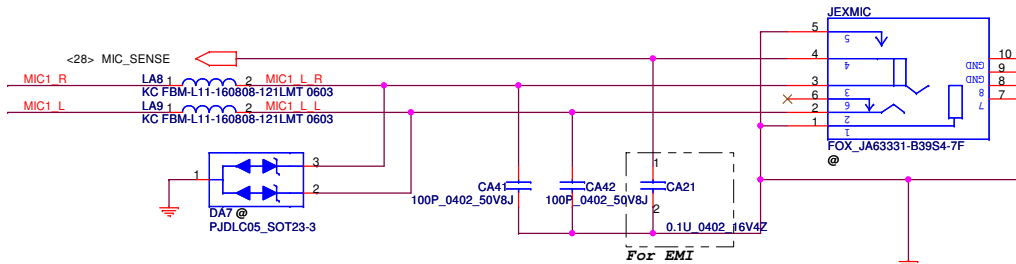
Ext. Mic



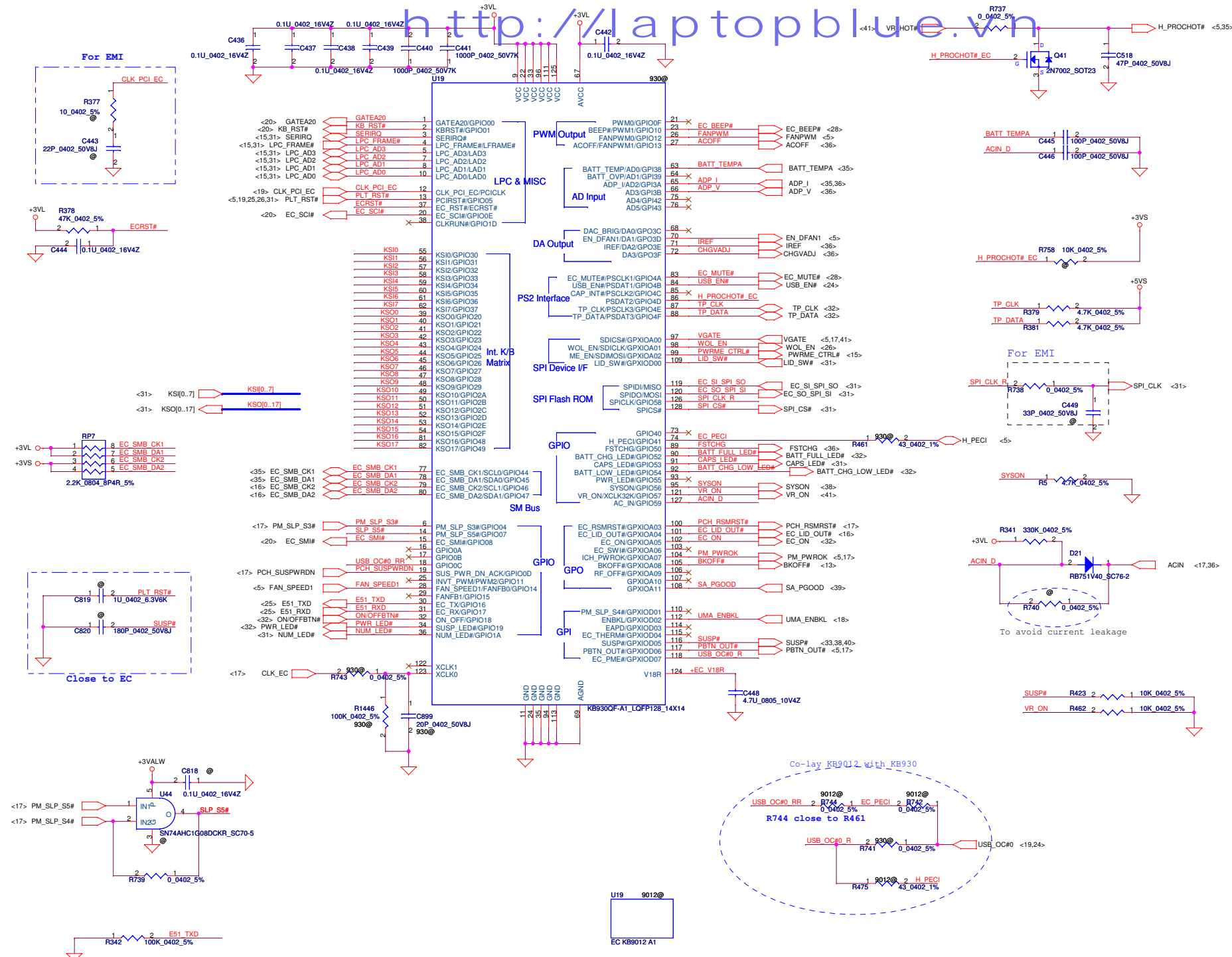
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

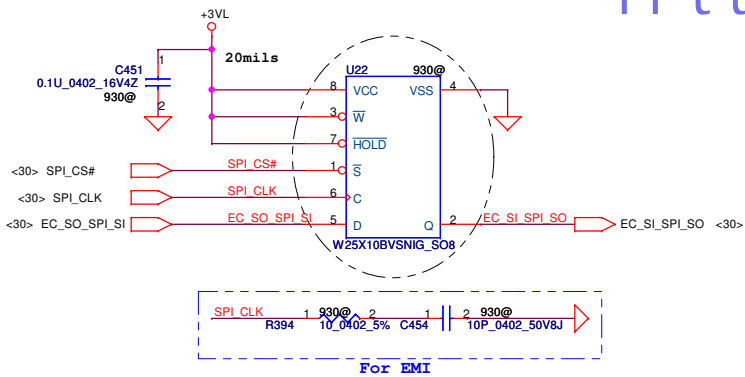


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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title		
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					PWWHA LA-7202P M/B	1.0
				Date:	Friday, February 25, 2011	Sheet 29 of 43

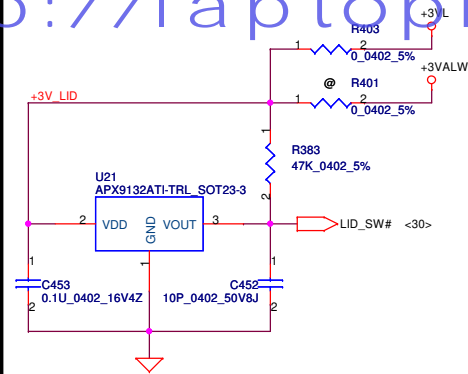


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Issued Date		2010/09/03	Deciphered Date	2012/12/31	Title					
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					Size	Document Number		Rev		
					PWWHA LA-7202P M/B		1.0			
Date:					Friday, February 25, 2011		Sheet	30	of	43

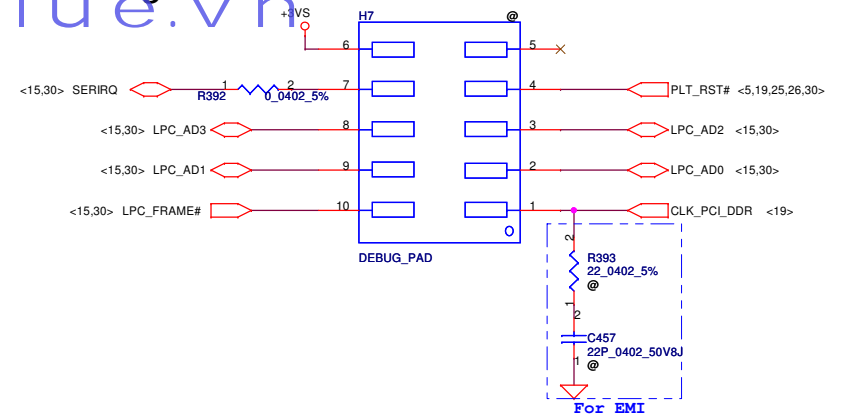
SPI Flash (256KB)



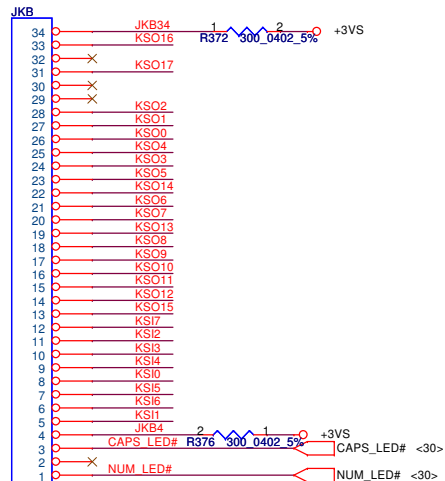
Lid SW



LPC Debug Port

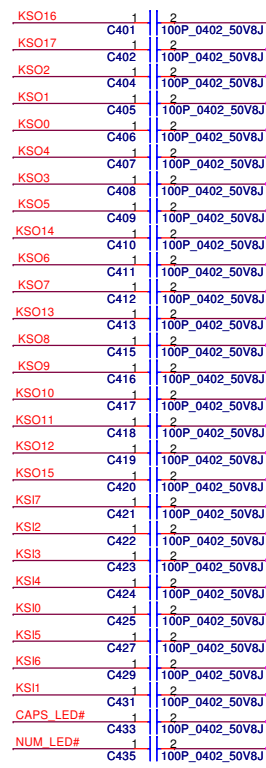


KEYBOARD CONN.



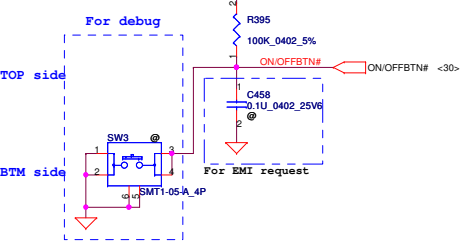
For EMI

Close to JKB



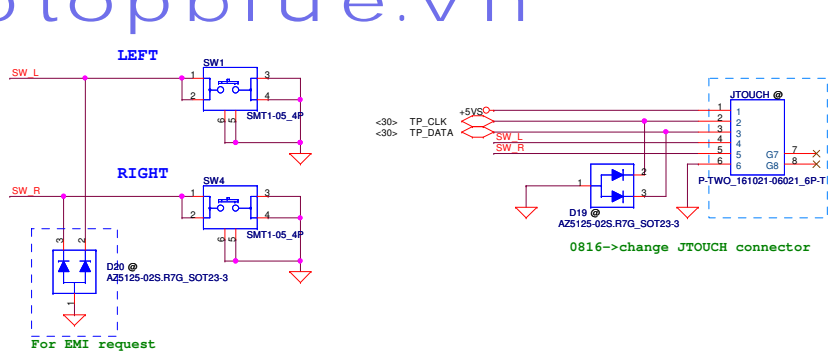
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title
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Size		Document Number		Rev
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Power Button

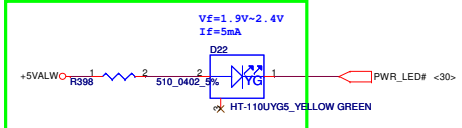


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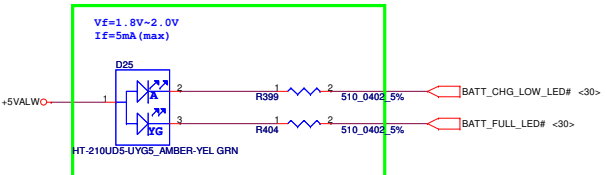
TP Button/Conn.



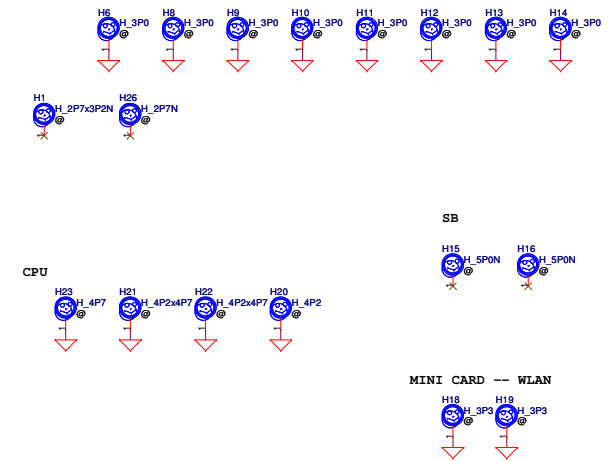
POWER/SUSPEND LED



BATT CHARGE/FULL LED



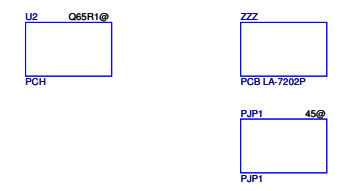
Screw Hole



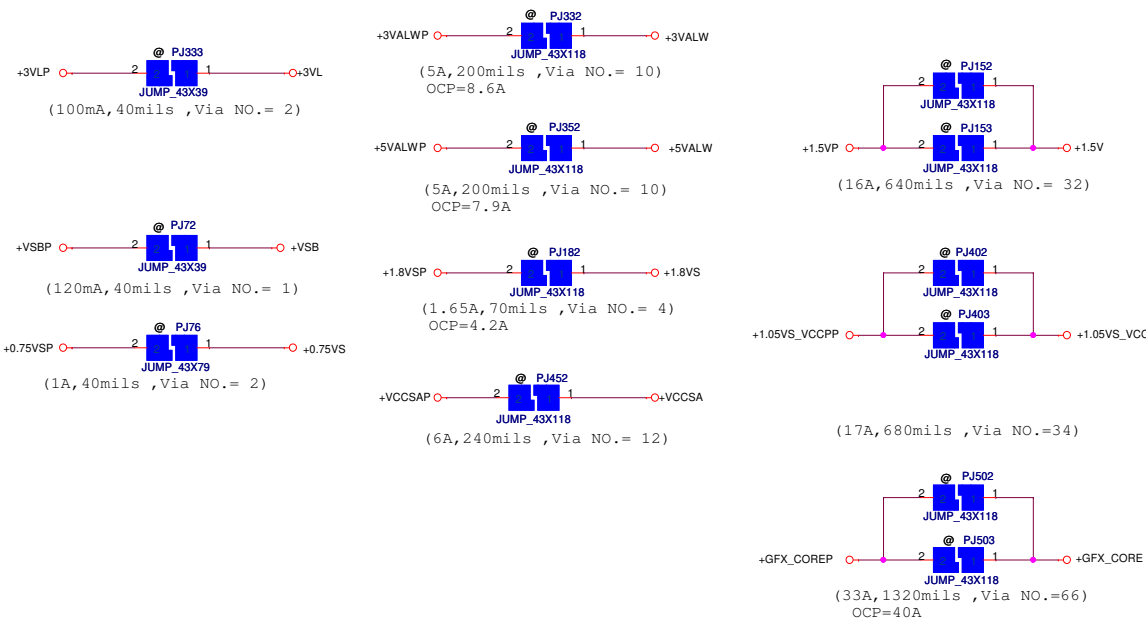
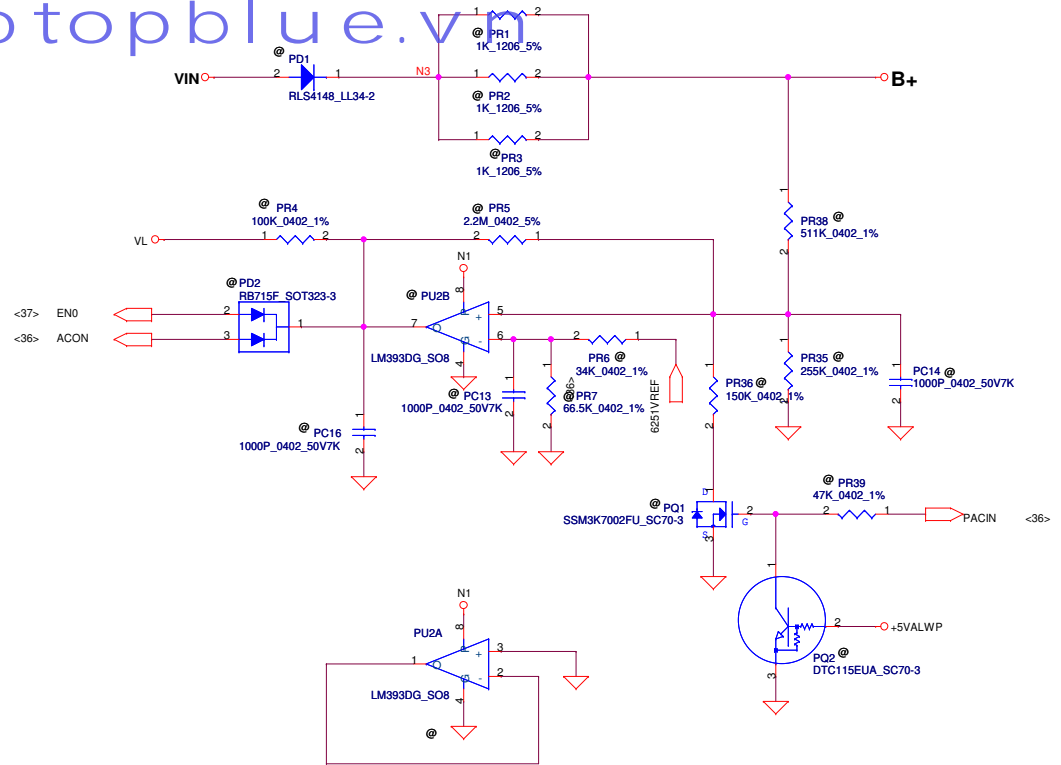
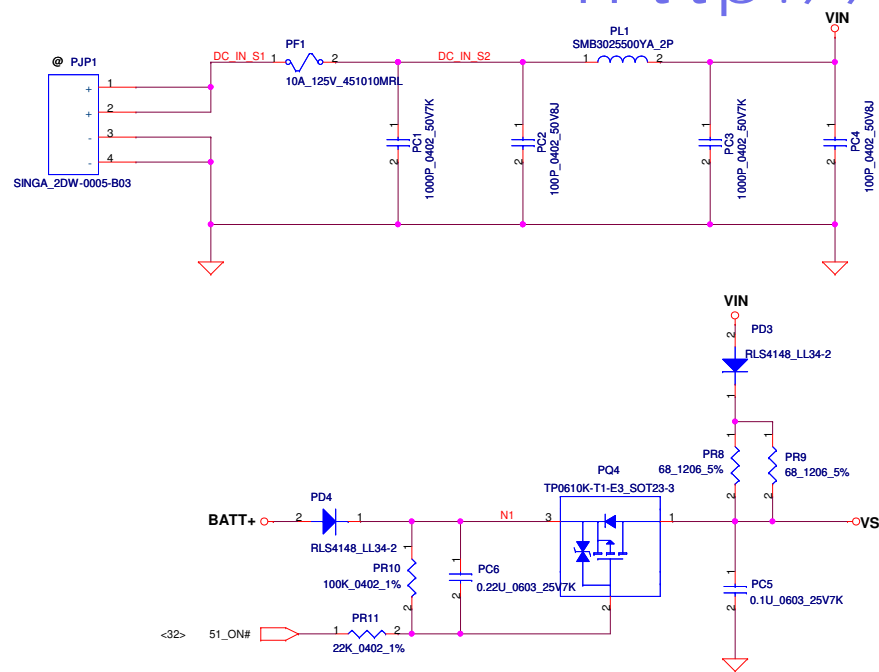
PCB Fedical Mark PAD



ISPD



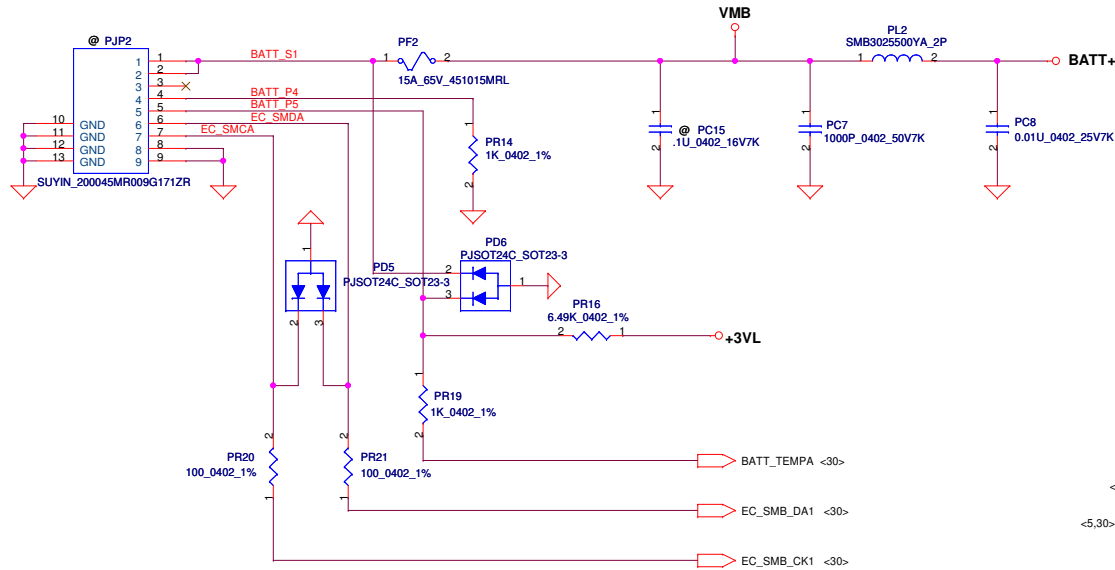
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ACIN			
	Precharge detector		
	Min.	typ.	Max.
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

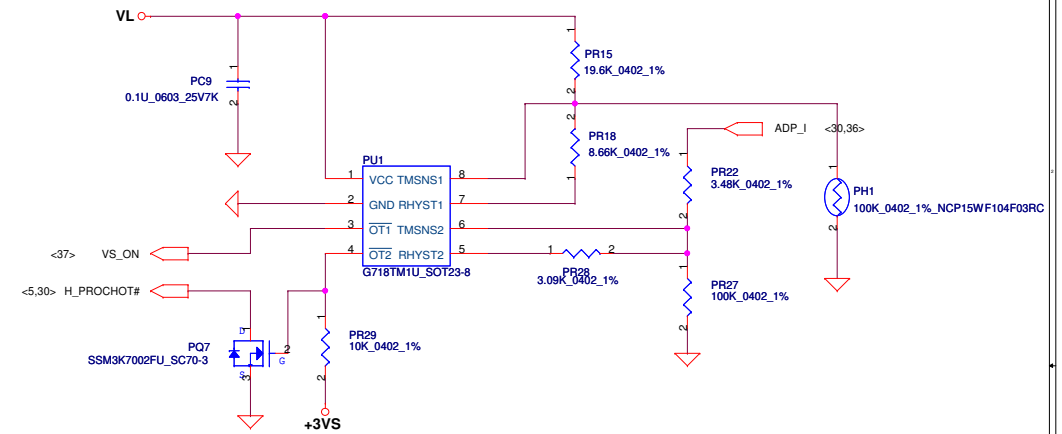
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/09/03				Title			
				Deciphered Date				2012/12/31			
								DCIN/VIN DETECTOR			
								Size			
								Document Number			
								PWWHA LA-7202 M/B			
								Date: Friday, February 25, 2011			
								Sheet 34 of 43			

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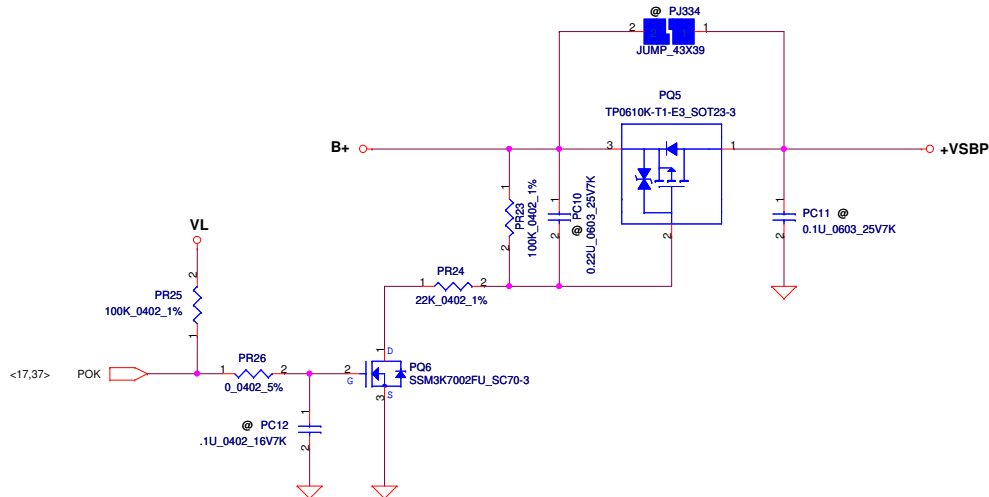


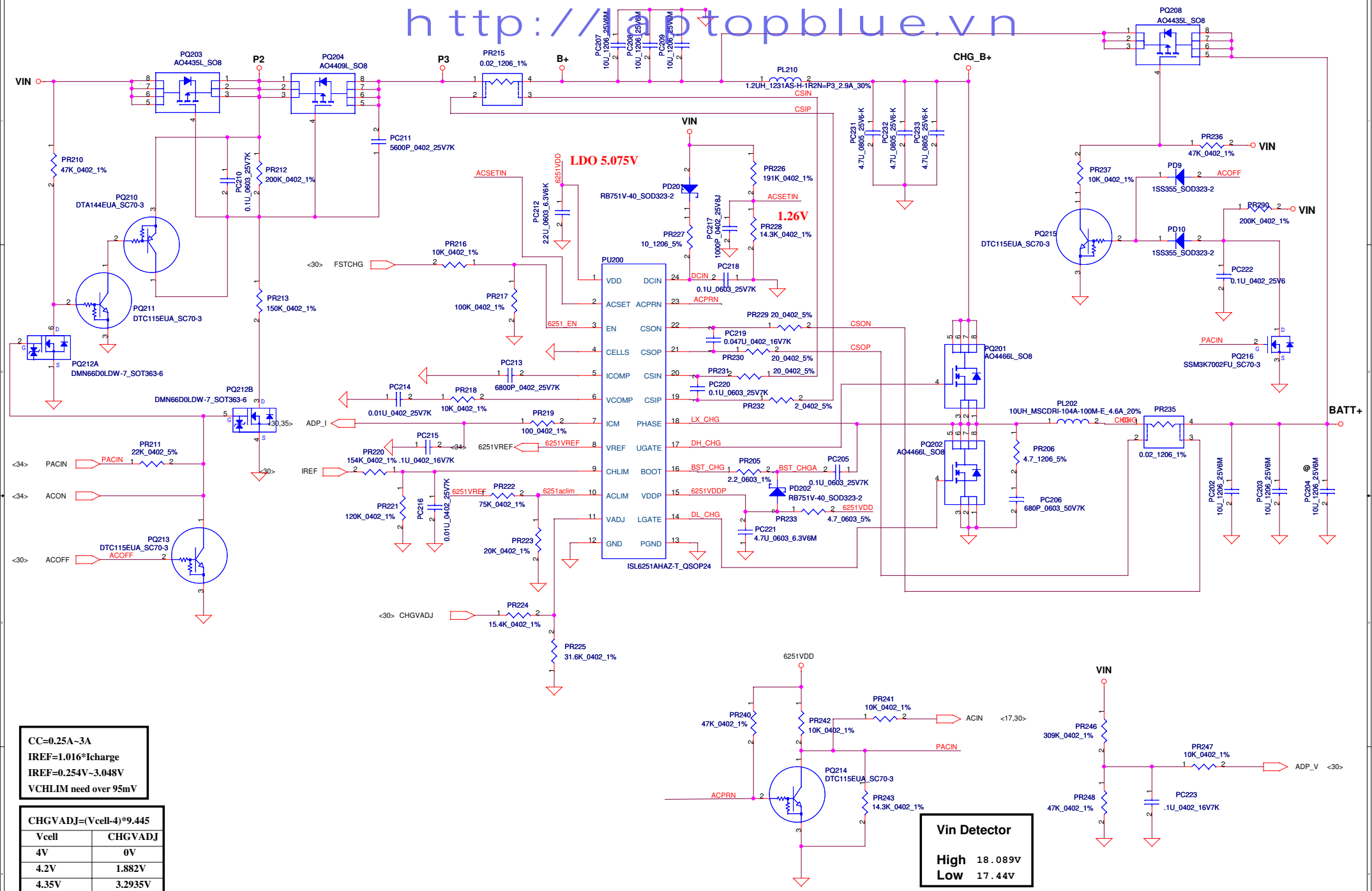
PH1 under CPU botten side :

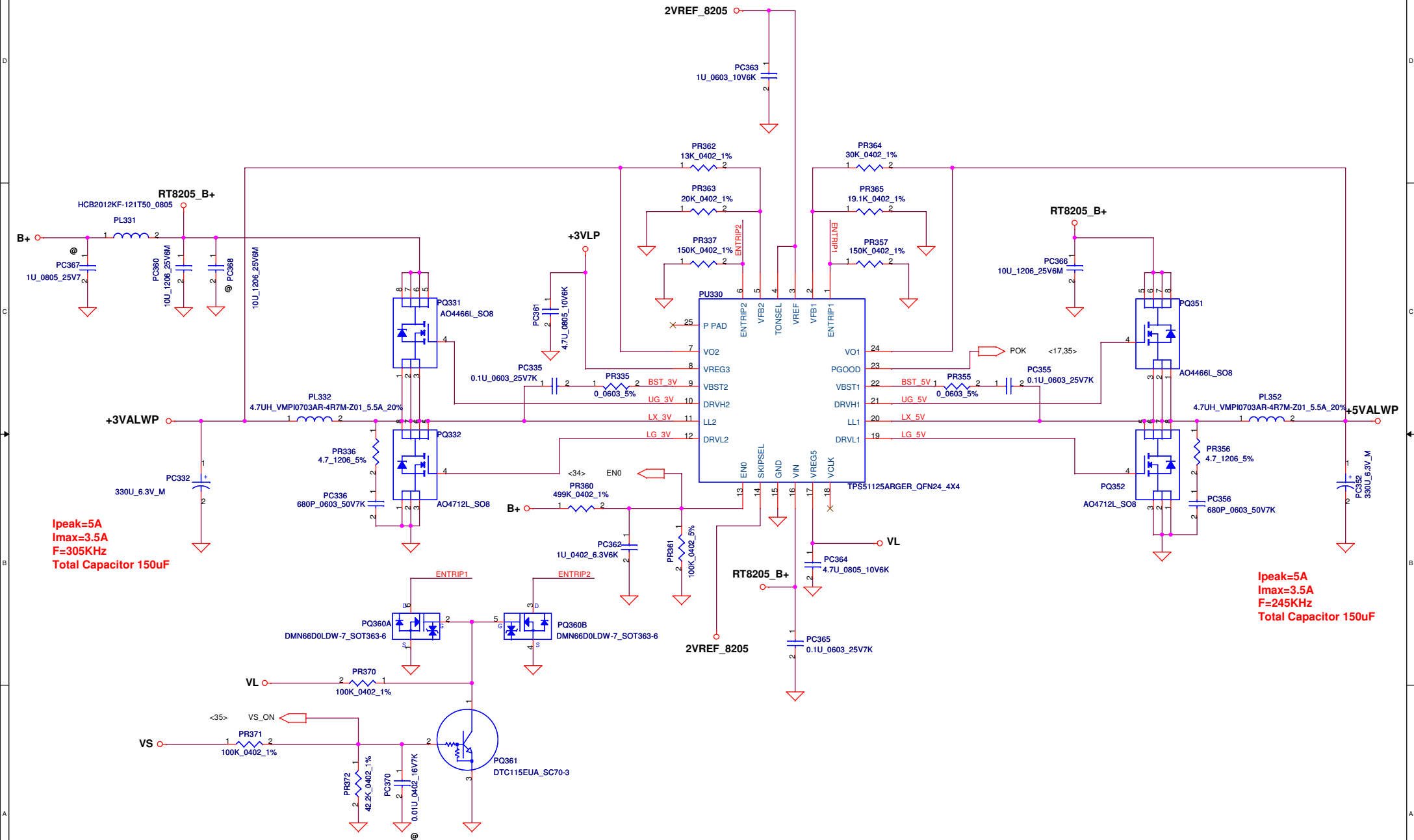
CPU thermal protection at 95 degree C
Recovery at 56 degree C



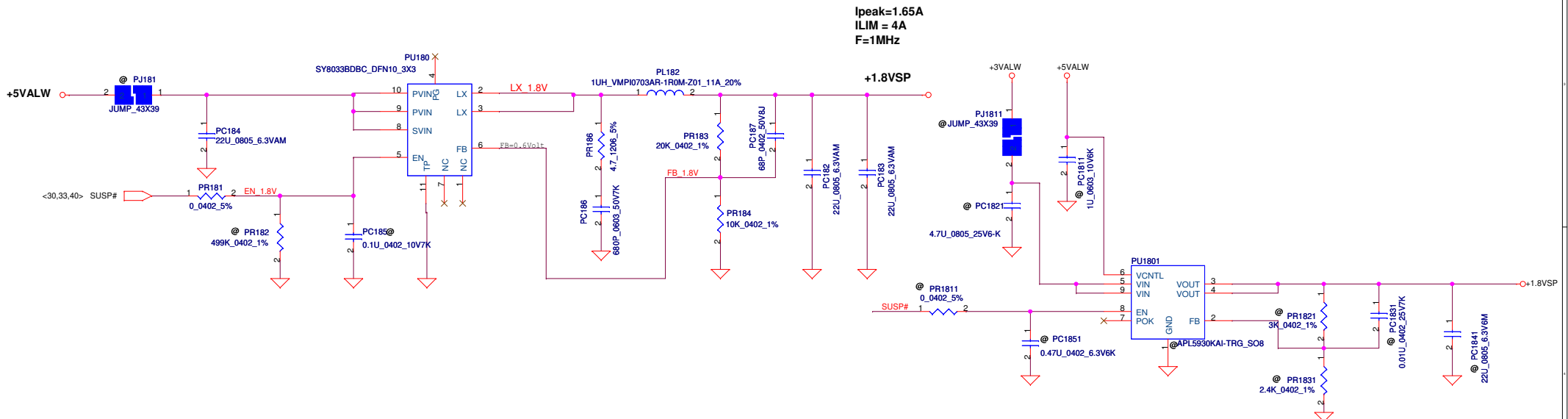
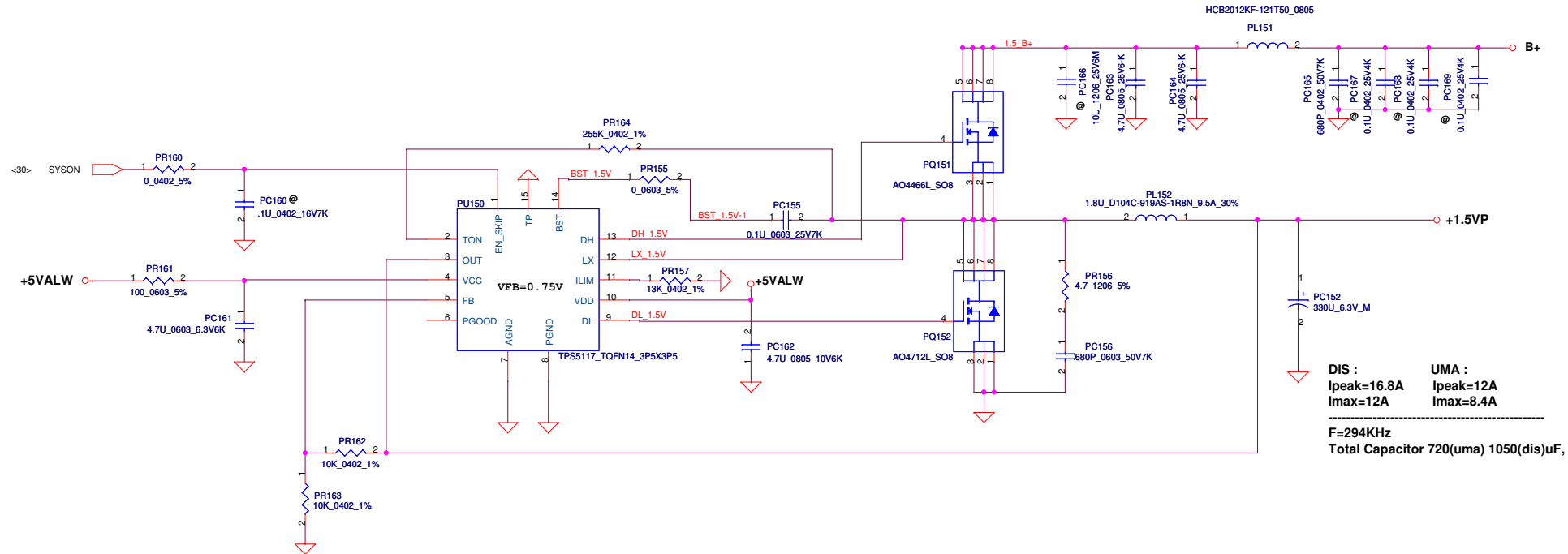
Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V



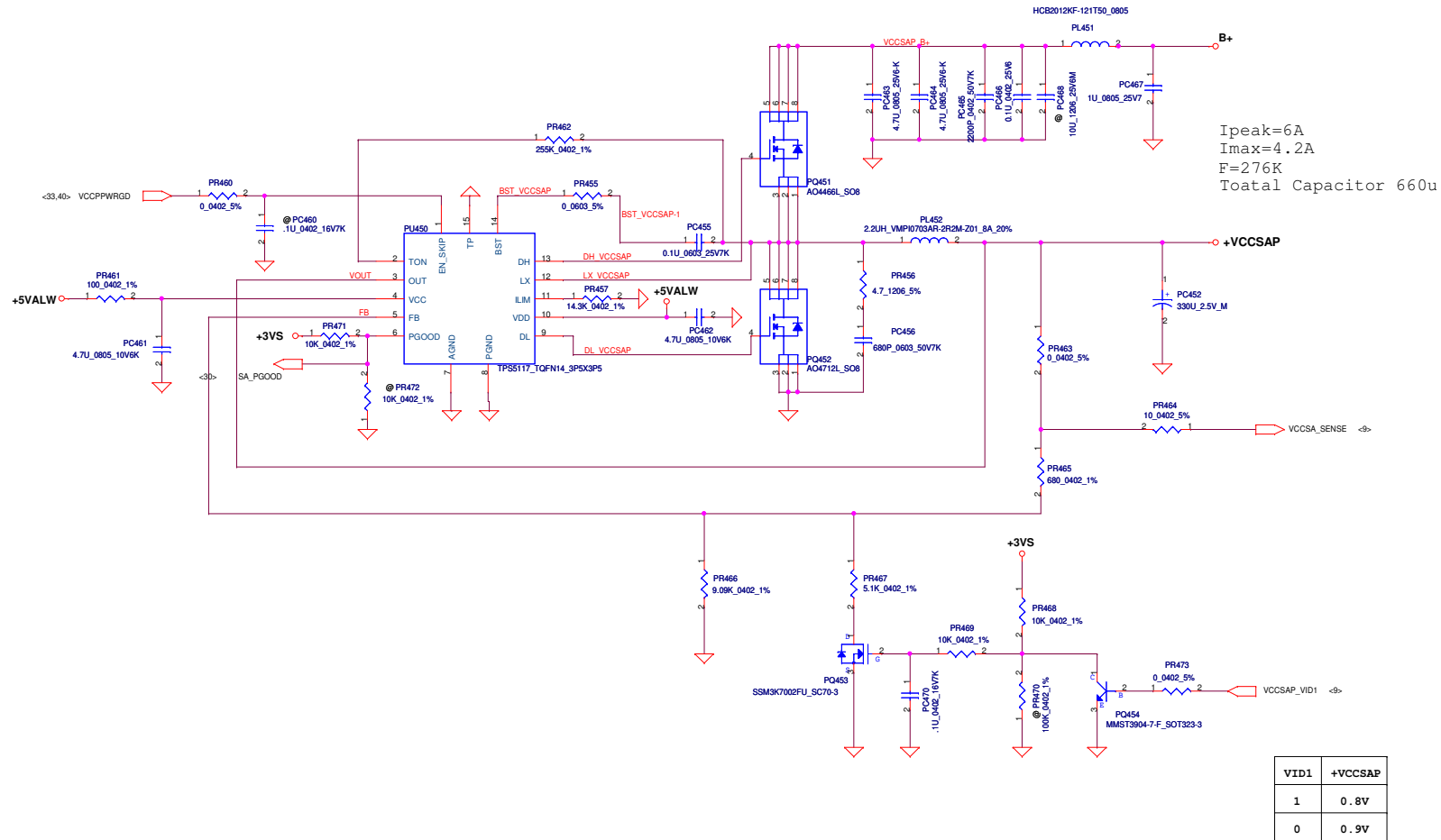


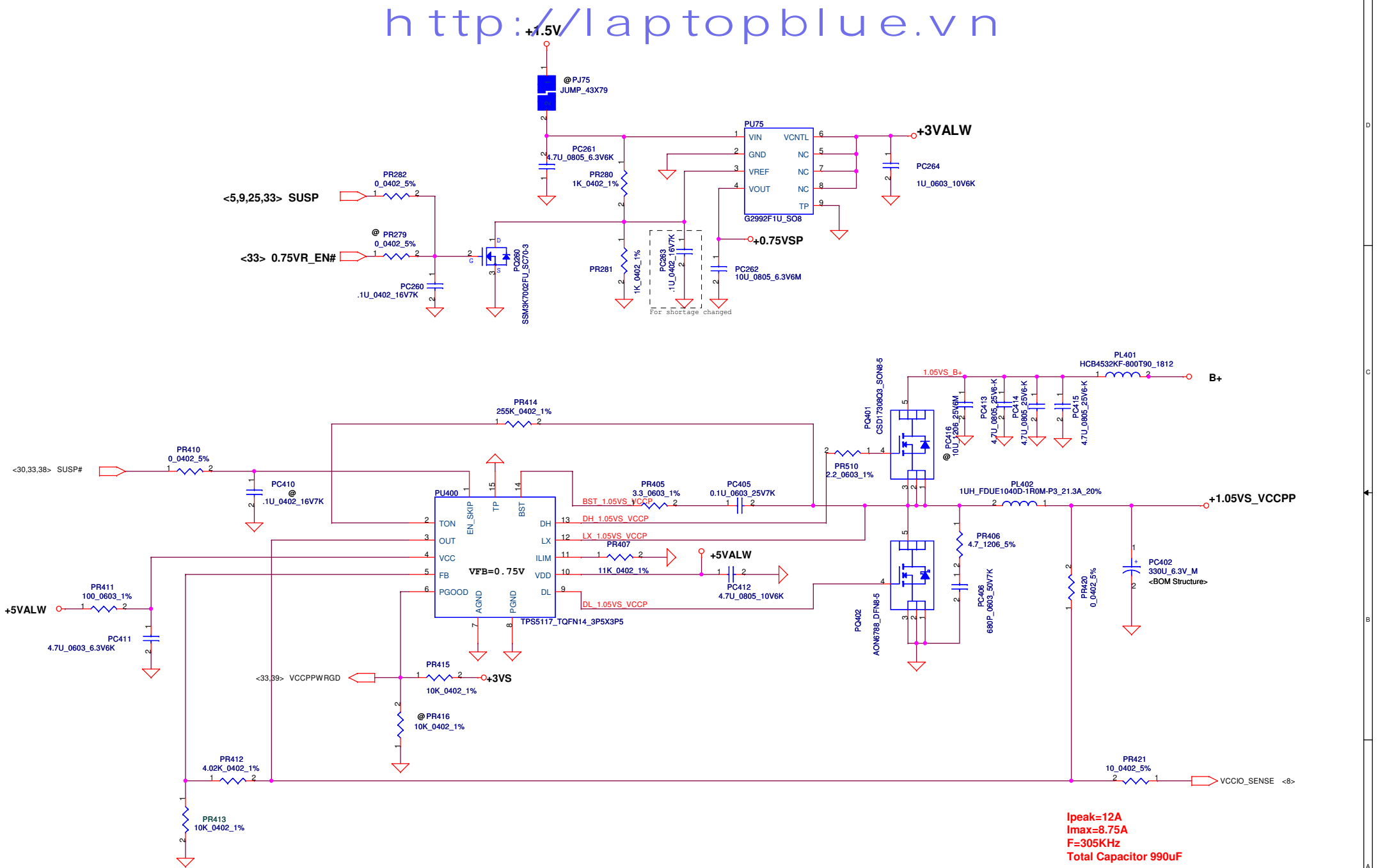


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				PWWHA LA-7202 M/B	



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				PWWHA LA-7202 M/B			1.0
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I_{peak}=12A
I_{max}=8.75A
F=305KHz
Total Capacitor 990uF

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Size	Custom	Document Number	PWWHA LA-7202 M/B		Rev
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Title <Title>			
Size A	Document Number PWWHA LA-7202P M/B		Rev 1.0
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HW PIR (Product Improve Record)

PWWHA LA-7202P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2011/02/18

MODIFICATION LIST				PURPOSE
NO	DATE	PAGE		
1)	01/24	05	modify FAN with BTO item PWM and RPM	For HW BTO item
2)	01/24	05	modify RPM FAN connector pin define	Request from thermal team
3)	02/14	30	co-lay KB9012	For BTO item
4)	02/15	24	Add C450	For ESD request

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Title		HW-PIR			
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