

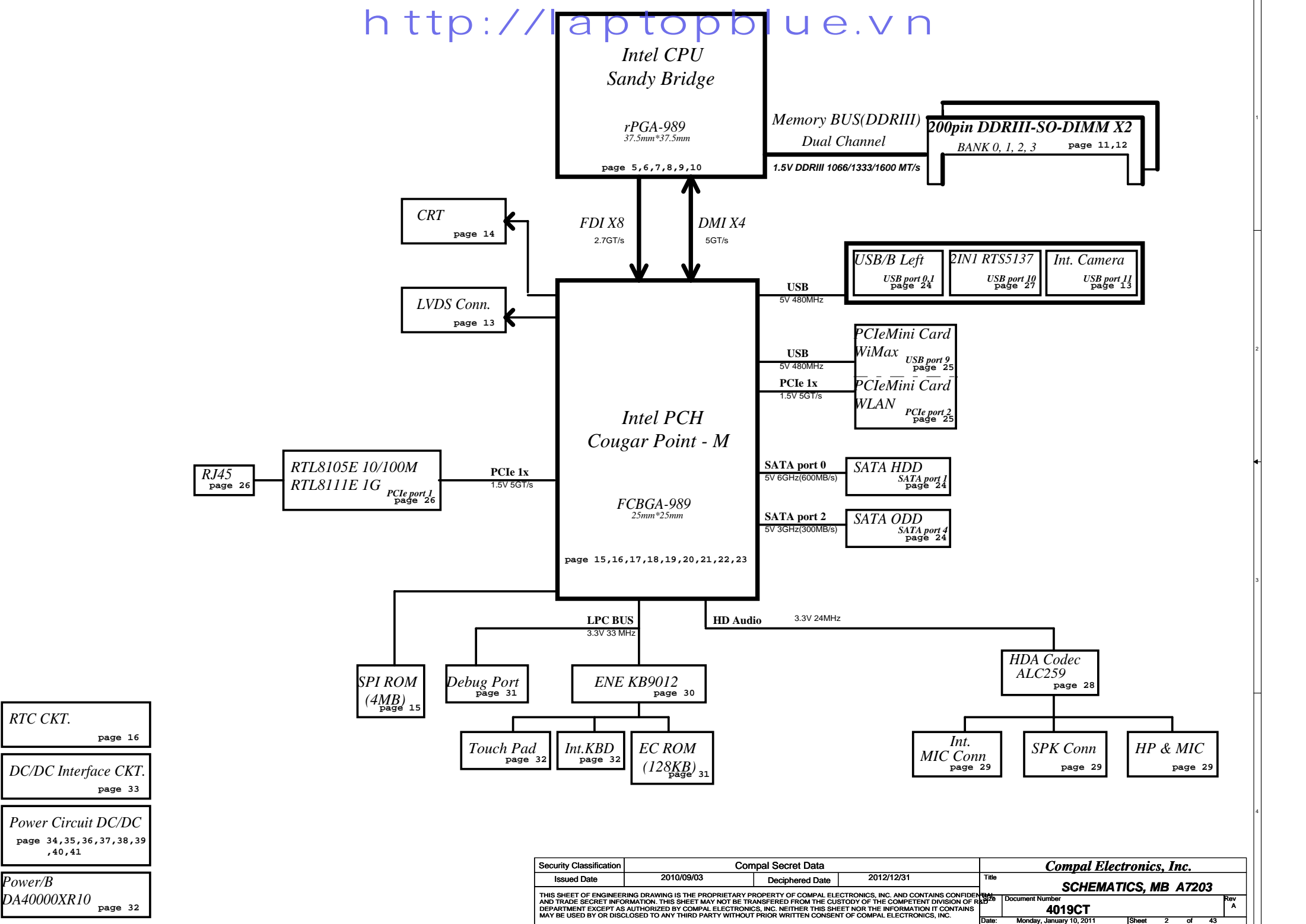
# *PWWHA*

## *TaiDi1 Plus*

# LA-7203P REV 0.1 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)  
2010-12-27 Rev 0.1

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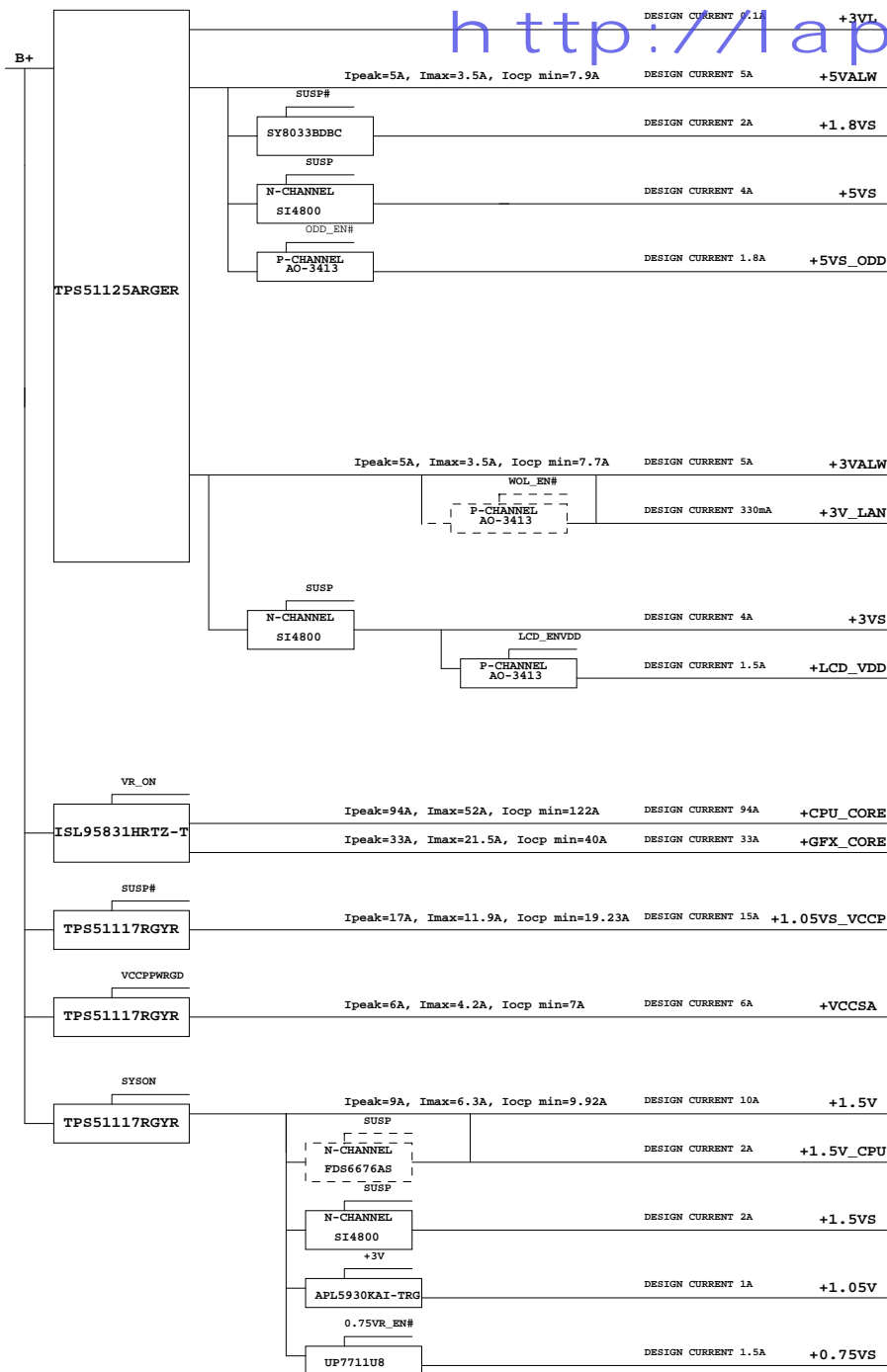
RTC CKT.  
page 16

DC/DC Interface CKT.  
page 33

Power Circuit DC/DC  
page 34,35,36,37,38,39,40,41

Power/B  
DA40000XR10  
page 32

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## Voltage Rails

( O MEANS ON X MEANS OFF )

<http://laptopblue.vn>

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
	S0	O	O	O	O	O
	S1	O	O	O	O	O
	S3	O	O	O	O	X
	S5 S4/AC	O	O	O	X	X
	S5 S4/ Battery only	O	O	O	X	X
	S5 S4/AC & Battery don't exist	O	X	X	X	X

## BTO Option Table

Function	MINI PCI-E SLOT	LAN		Camera & Mic		
description	SLOT1	LAN		Camera & Mic		
explain	WIMAX	10/100M	Giga	Camera & Mic		
BTO	WIMAX@	8105E@	8111E@	CAM@		

## PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

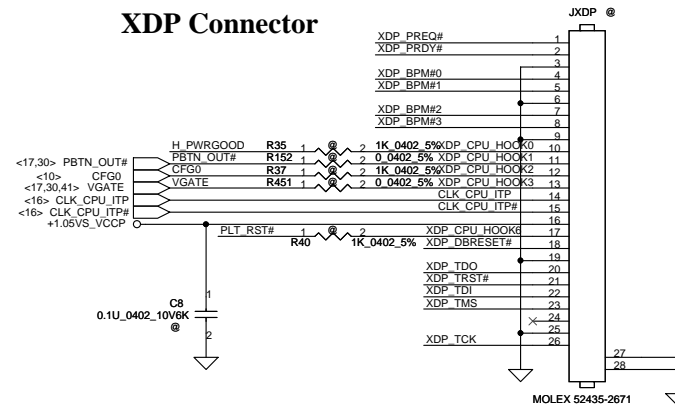
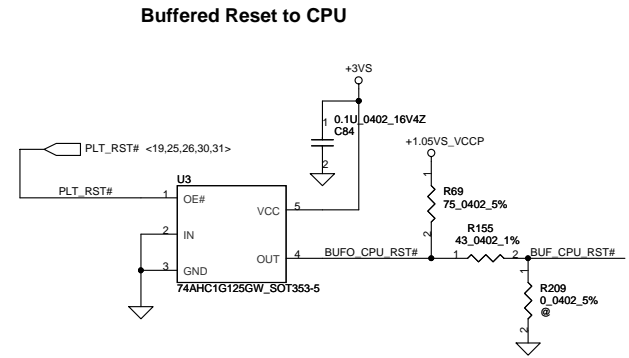
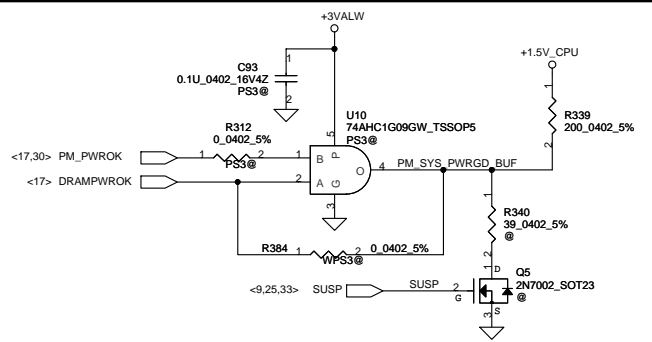
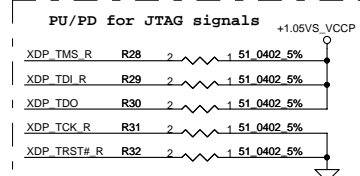
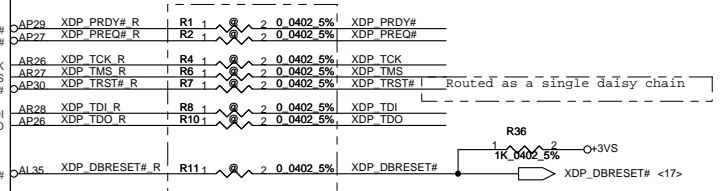
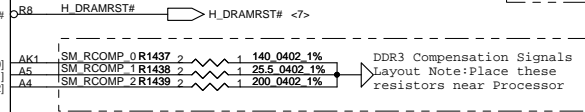
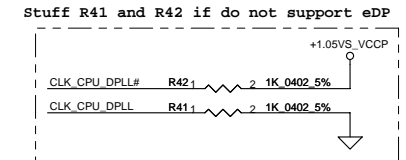
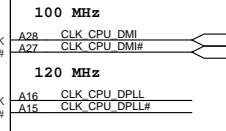
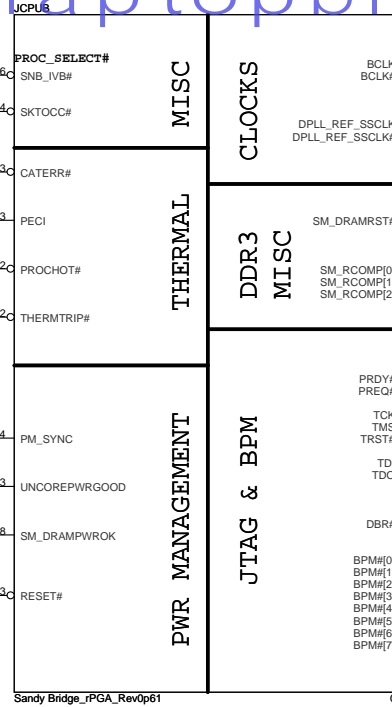
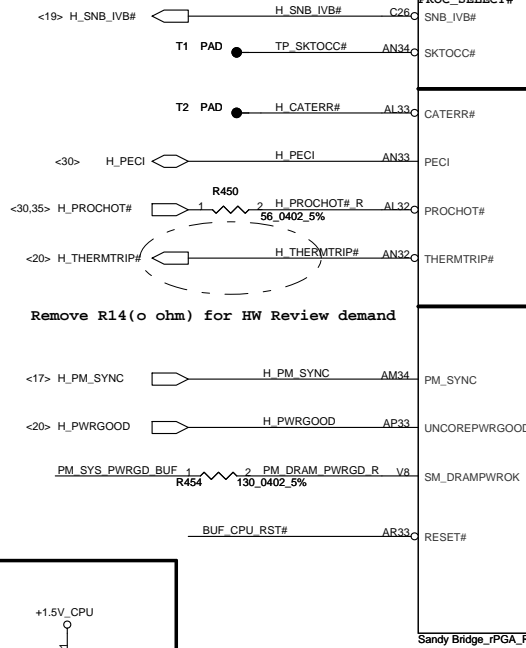
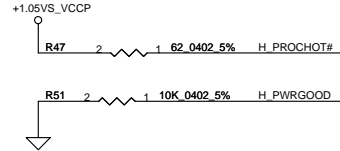
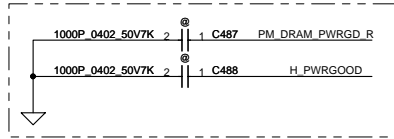
## EC SM Bus1 Address

## EC SM Bus2 Address

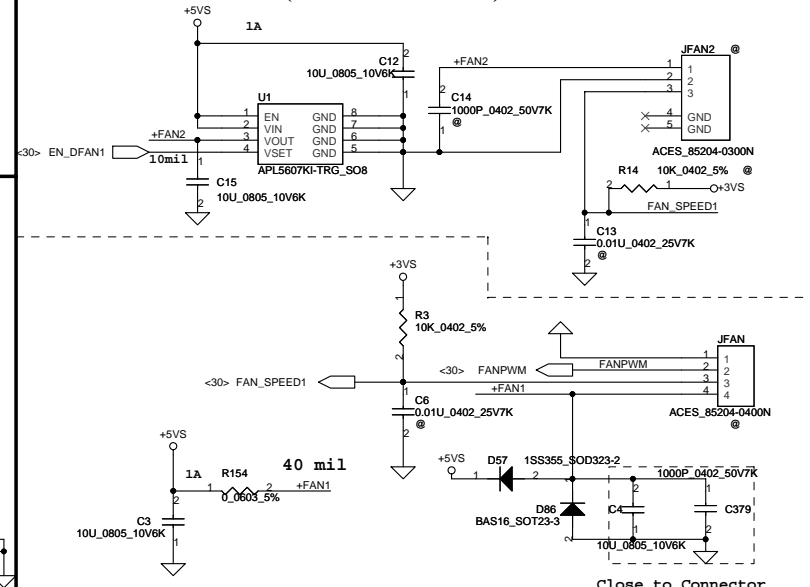
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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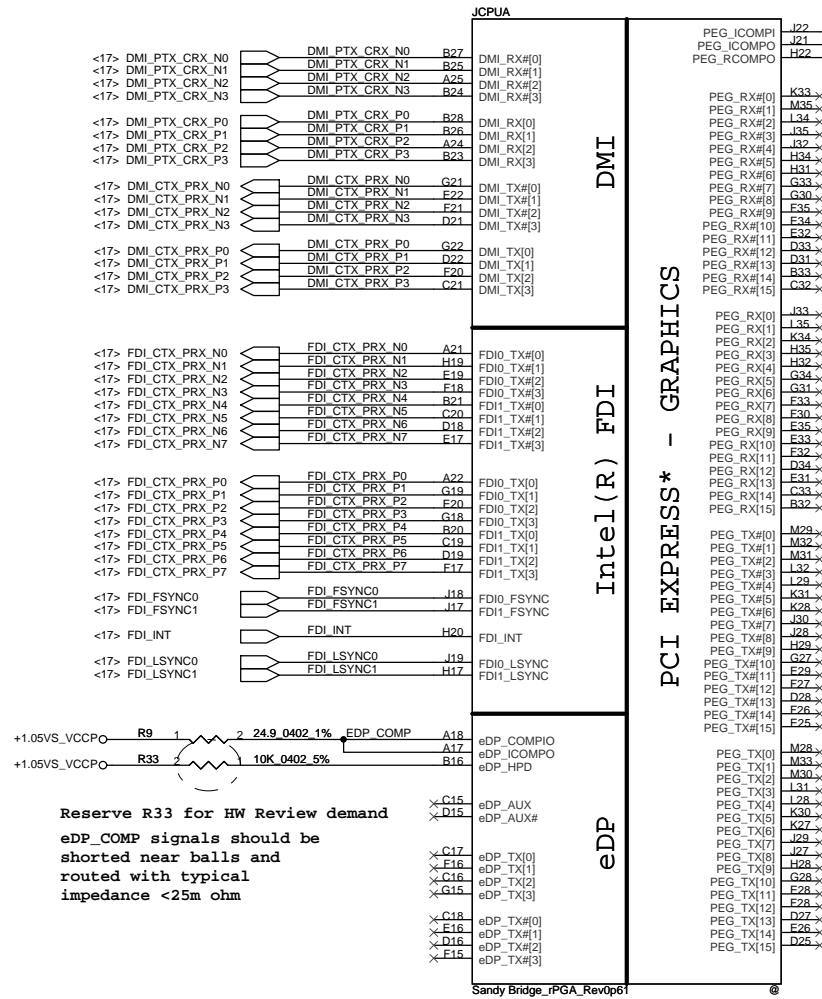


## FAN Control Circuit (RPM and PWM)

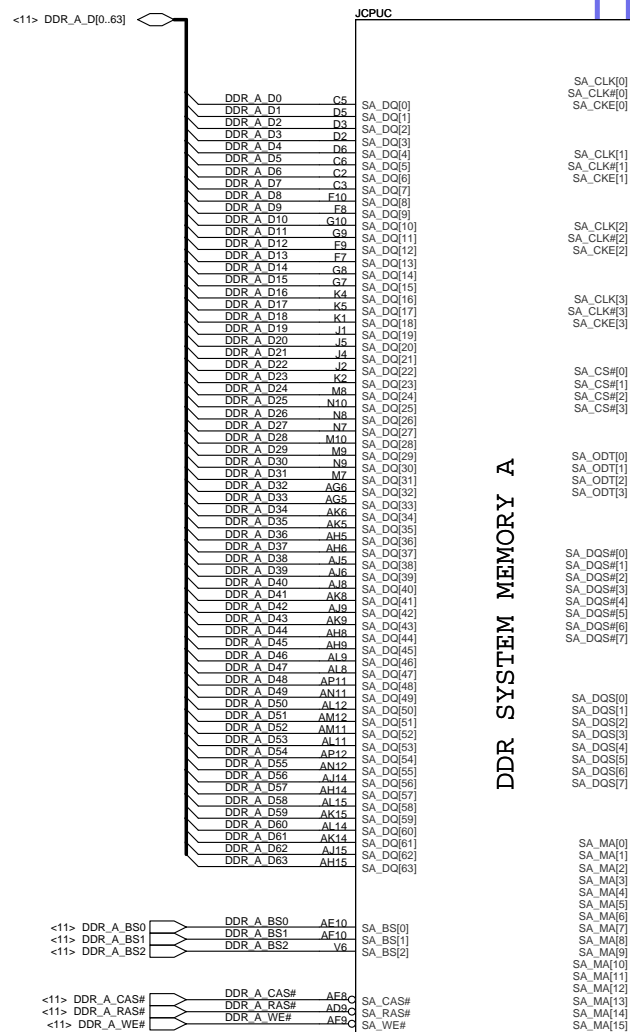


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PEG\_ICOMPI and RCOMPO signals should be  
shorted and routed  
with - max length = 500 mils - typical  
impedance = 43 m ohm (4 mils)  
PEG\_ICOMPO signals should be routed with -  
max length = 500 mils  
- typical impedance = 14.5 m ohm (12 mils)

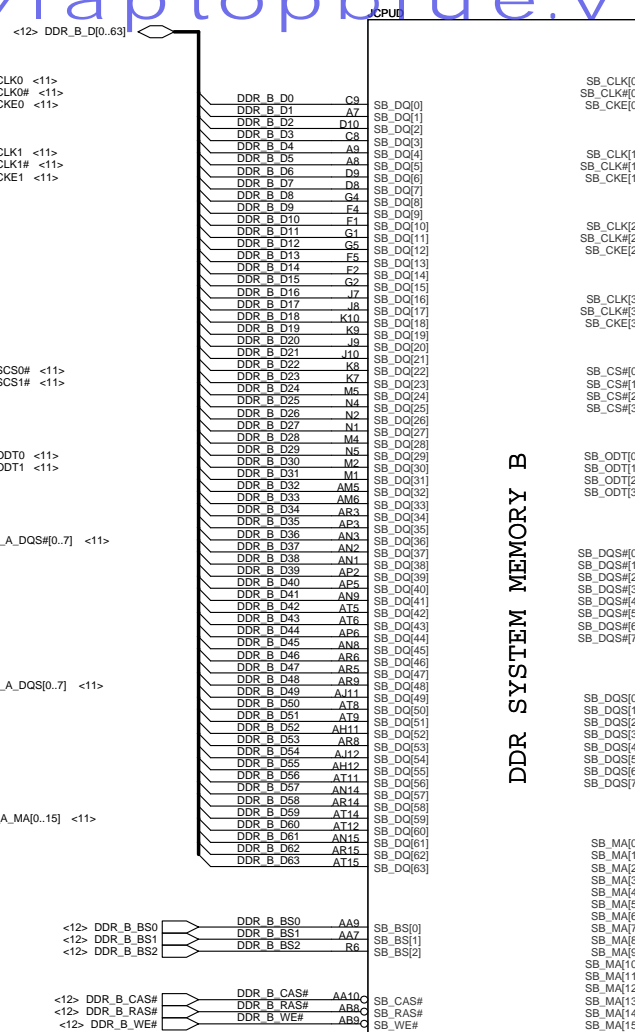


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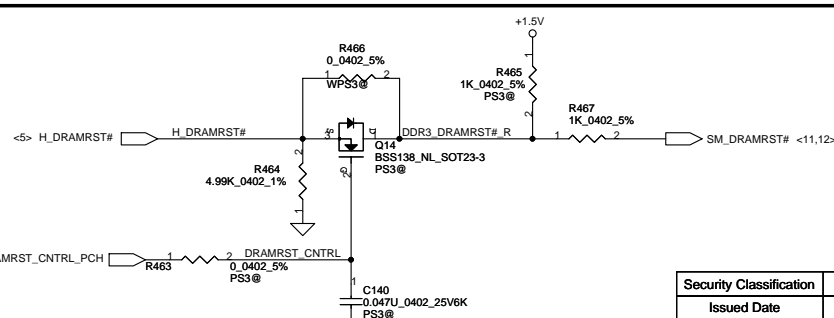
DDR SYSTEM MEMORY A

Sandy Bridge\_rPGA\_Rev0p61

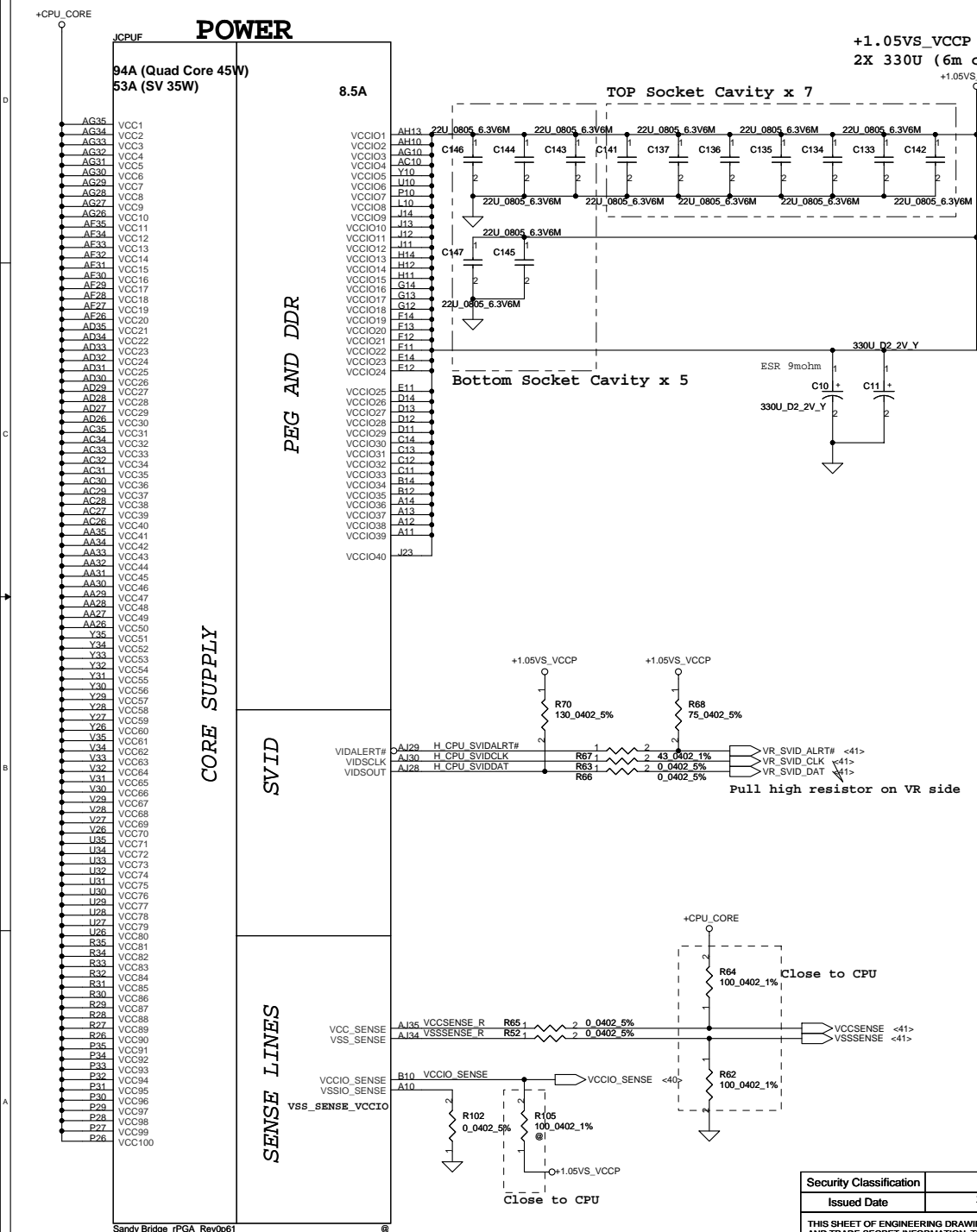


DDR SYSTEM MEMORY B

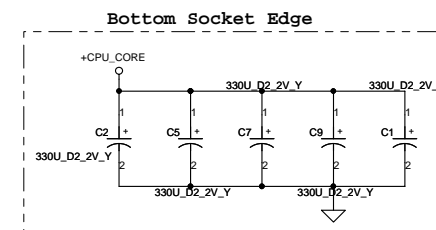
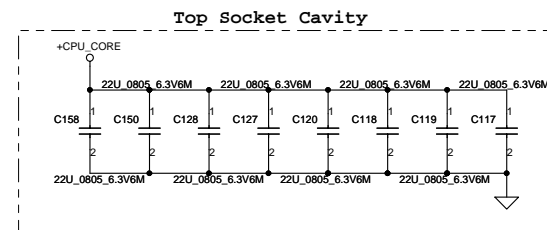
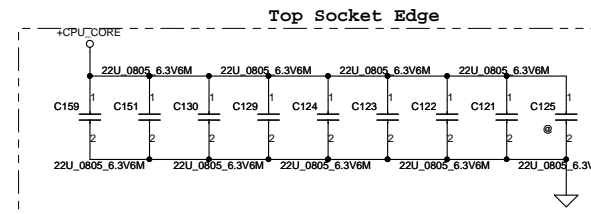
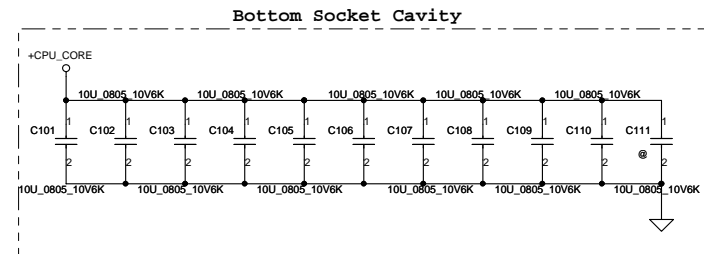
Sandy Bridge\_rPGA\_Rev0p61



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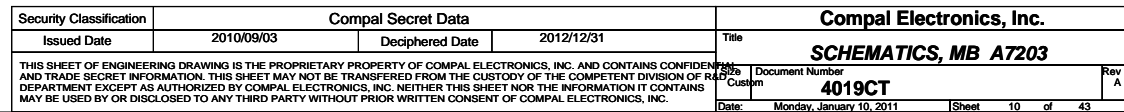
+CPU\_CORE Decoupling:  
4X 470U (4m ohm), 16X 22U, 10X 10U

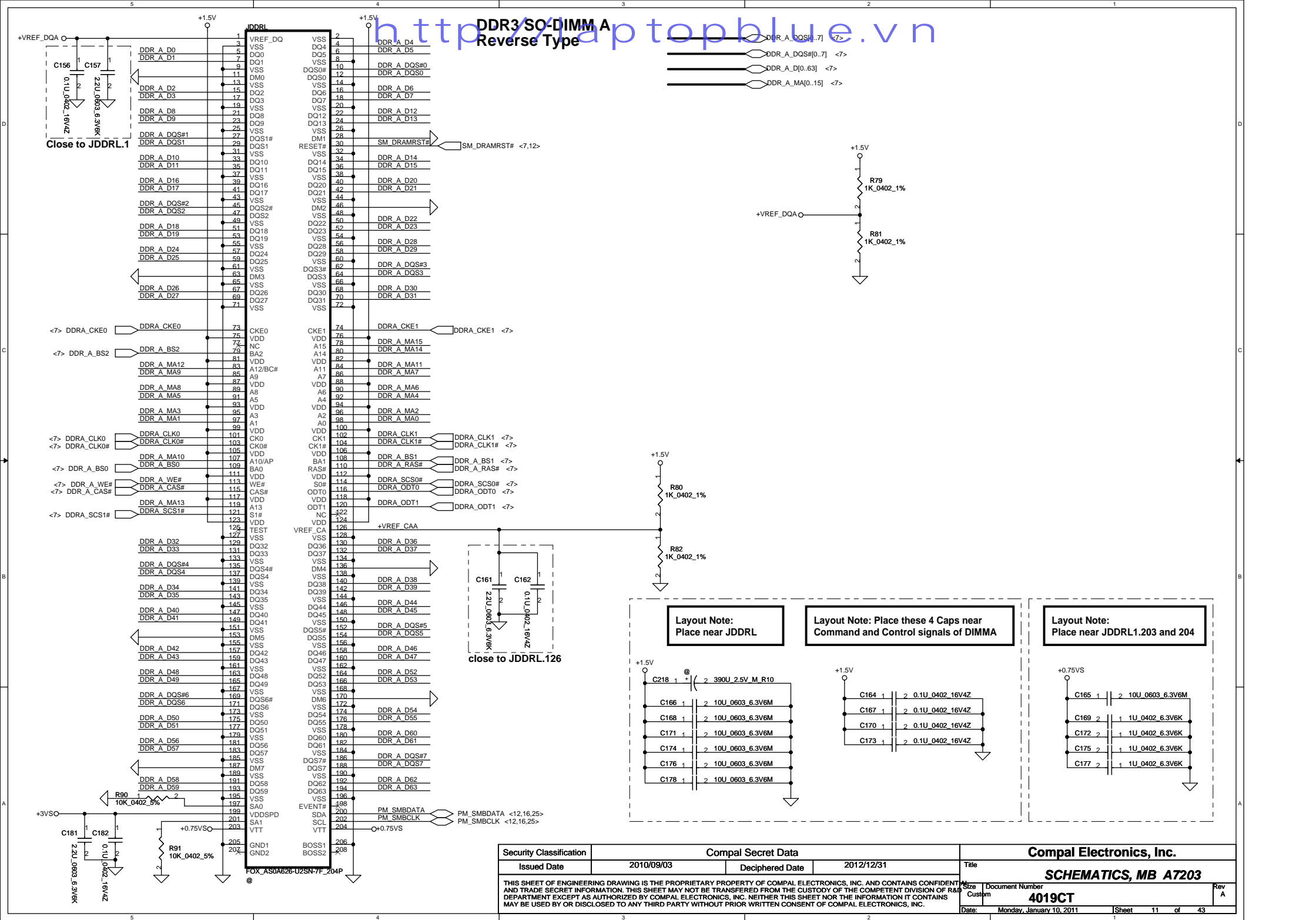


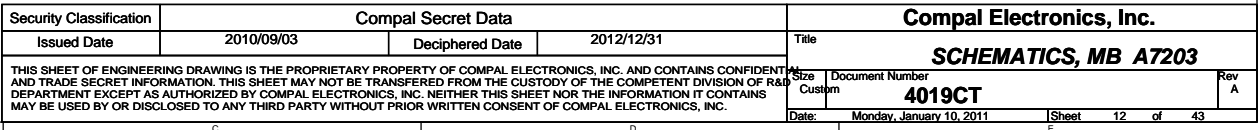
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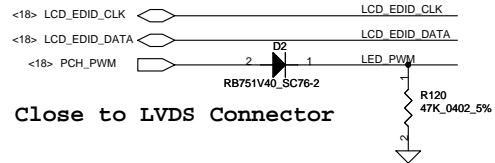




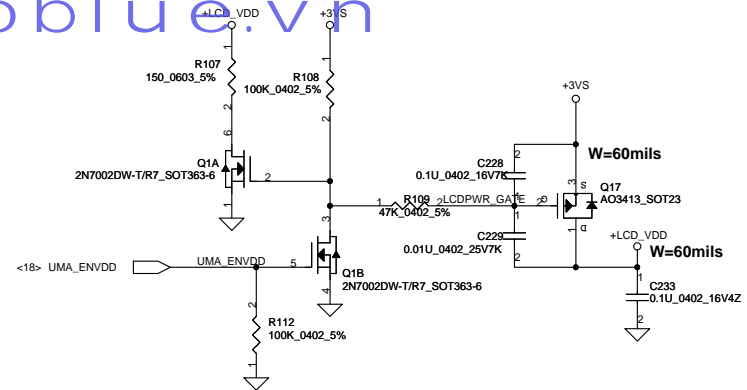
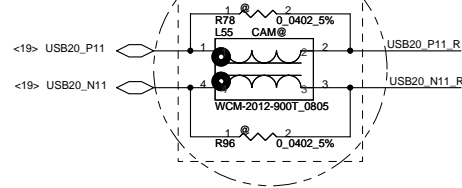




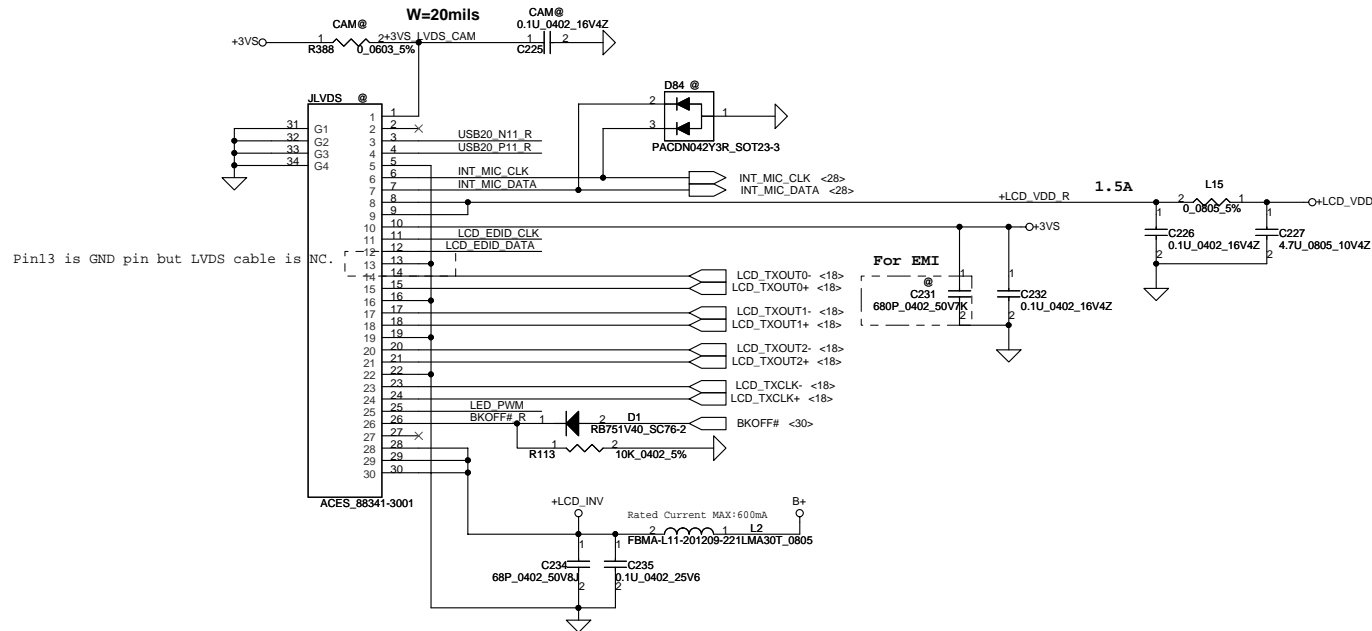




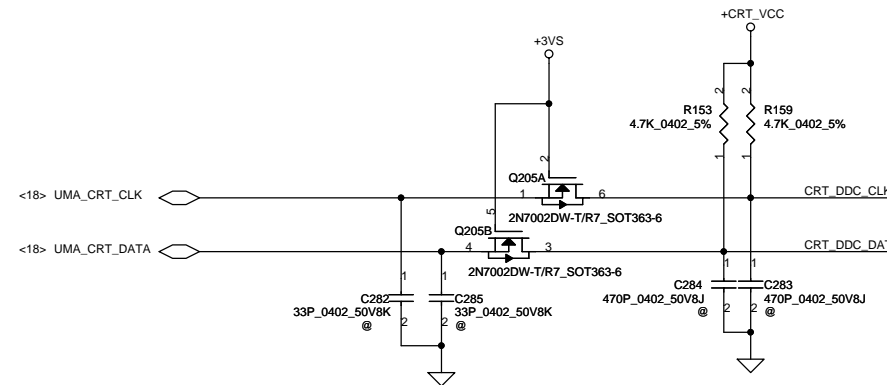
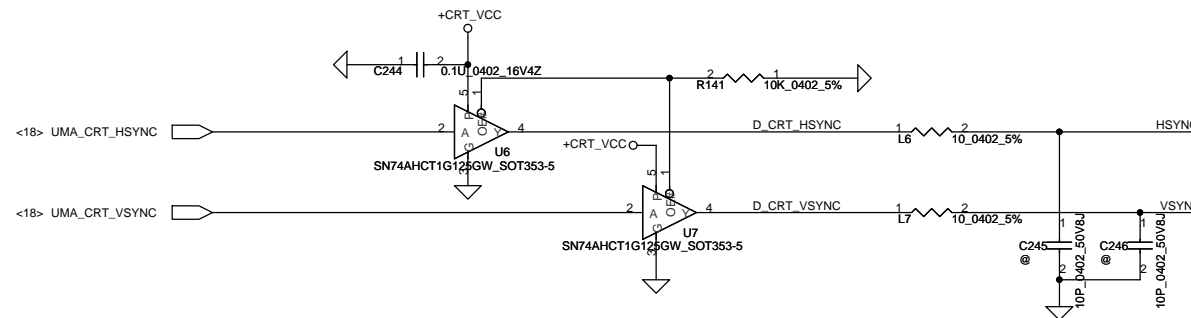
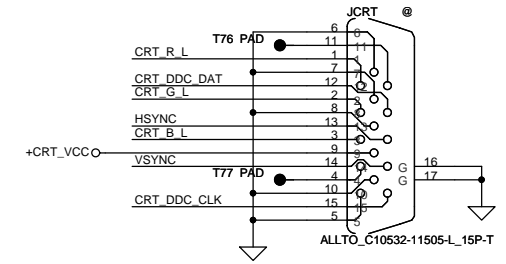
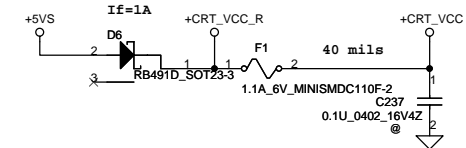
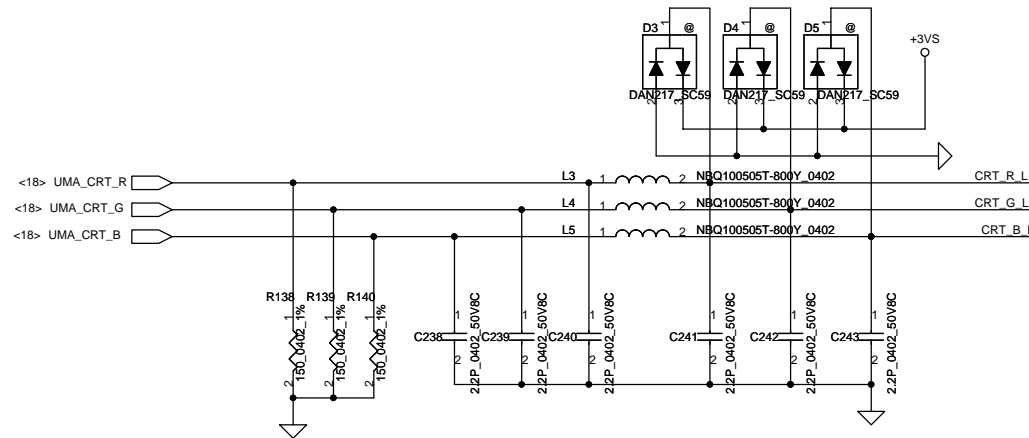
Reserve for EMI request



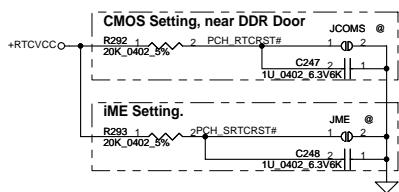
## LCD/PANEL BD. Conn.



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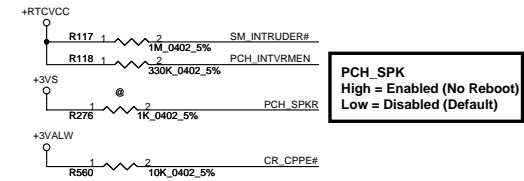


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**Integrated SUS 1.05V VRM Enable**

PCH\_INTVRMEN High - Enable Internal VRs (must be always pulled high)



**HDA\_SDO**

ME debug mode, this signal has a weak internal pull down

\*Low = Disable (default)

High = Enable (flash descriptor security override)

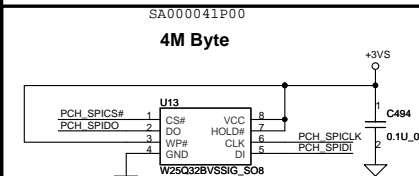
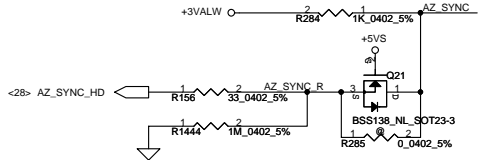
**HDA\_SYNC**

\*This signal has a weak internal pull down

H=>On Die PLL is supplied by 1.5V

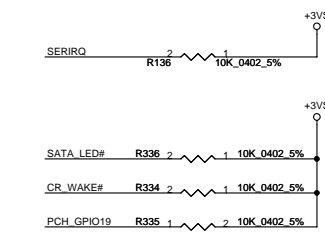
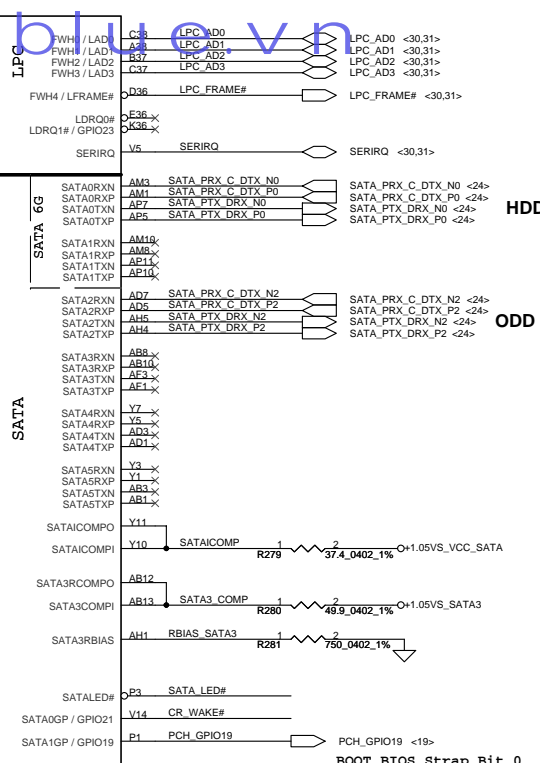
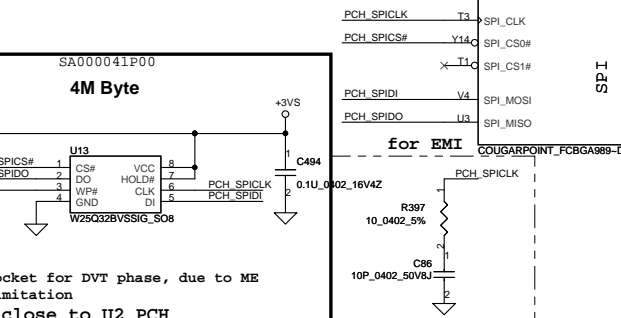
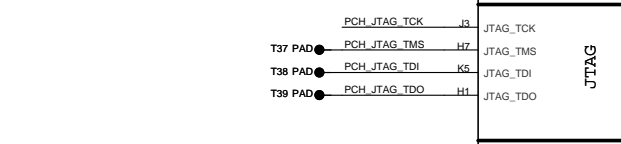
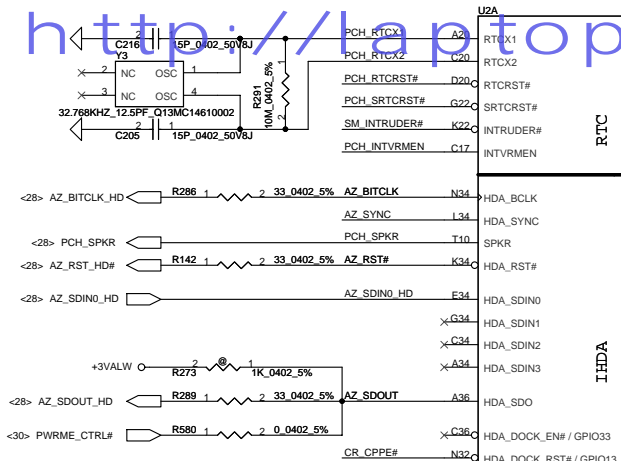
L=>On Die PLL is supplied by 1.8V

Need to pull high for Huron River platform

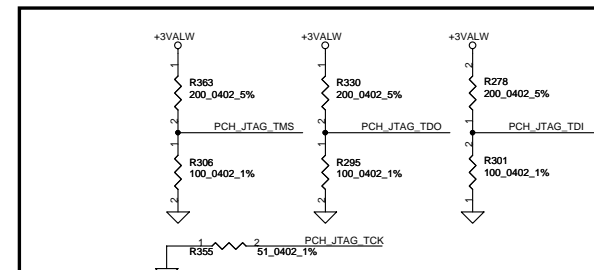
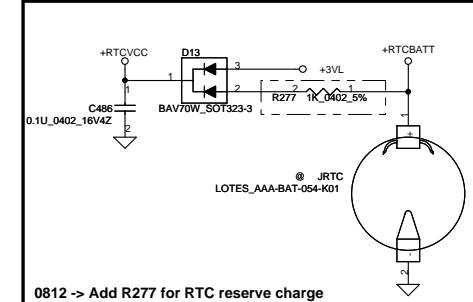


remove socket for DVT phase, due to ME height limitation

Please close to U2 PCH

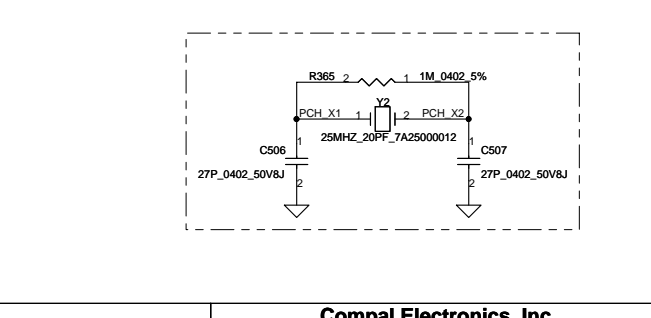
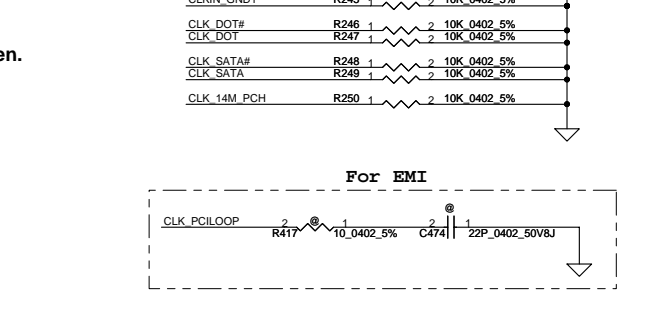
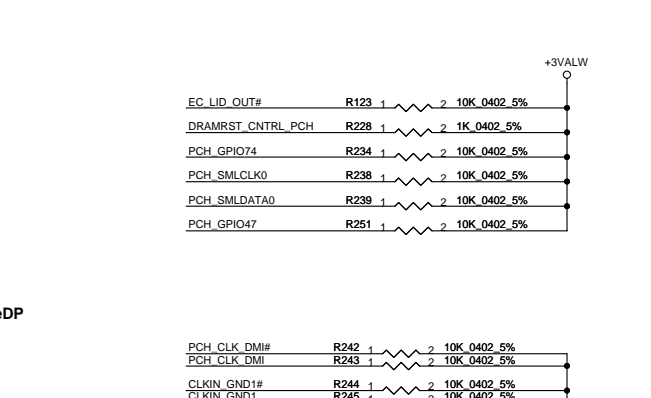


RTC schematic for non-chargeable



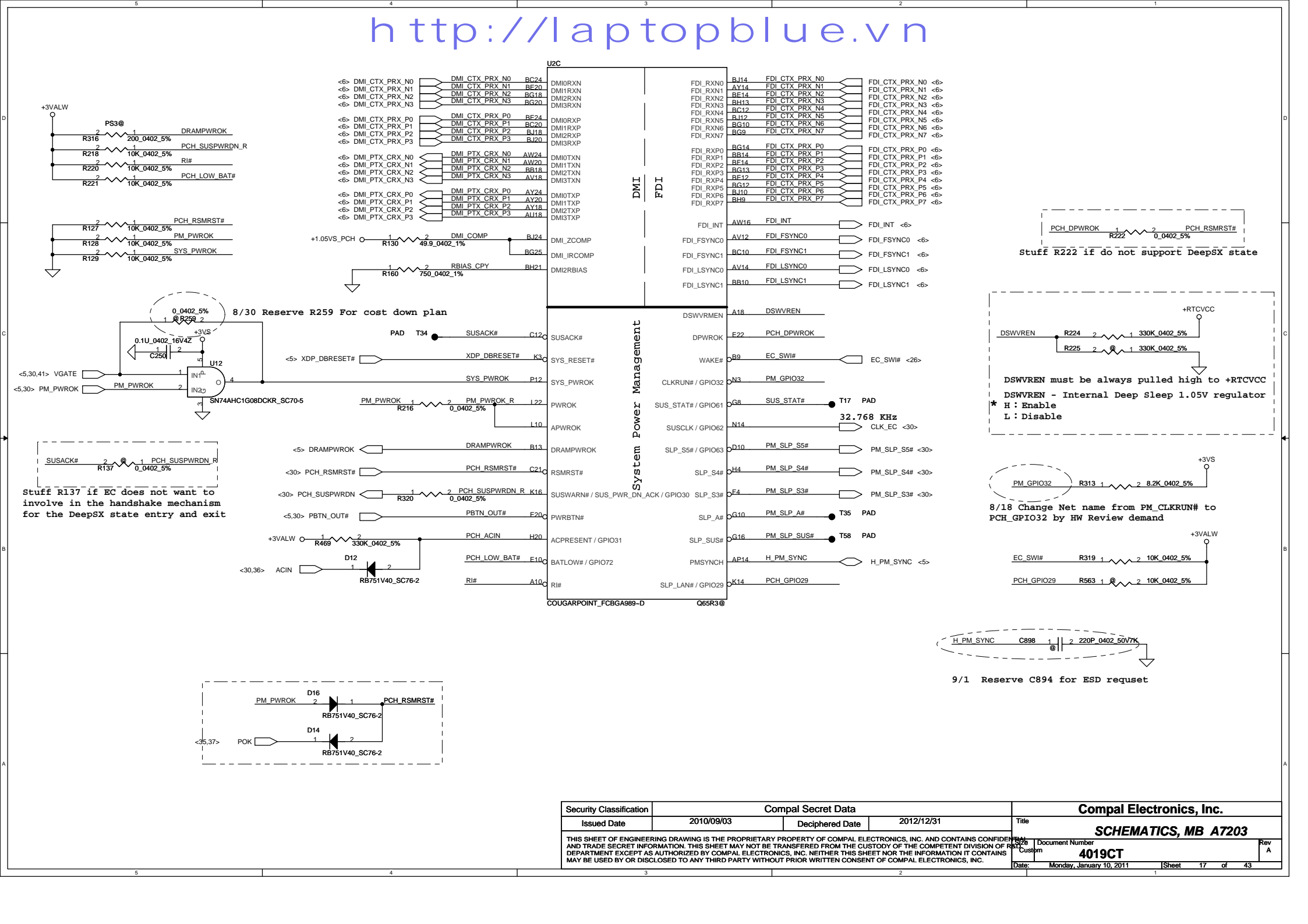
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**8/30 Reserve R259 For cost down plan**

**Stuff R137 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit**

**8/18 Change Net name from PM\_CLKRUN# to PCH\_GPIO32 by HW Review demand**

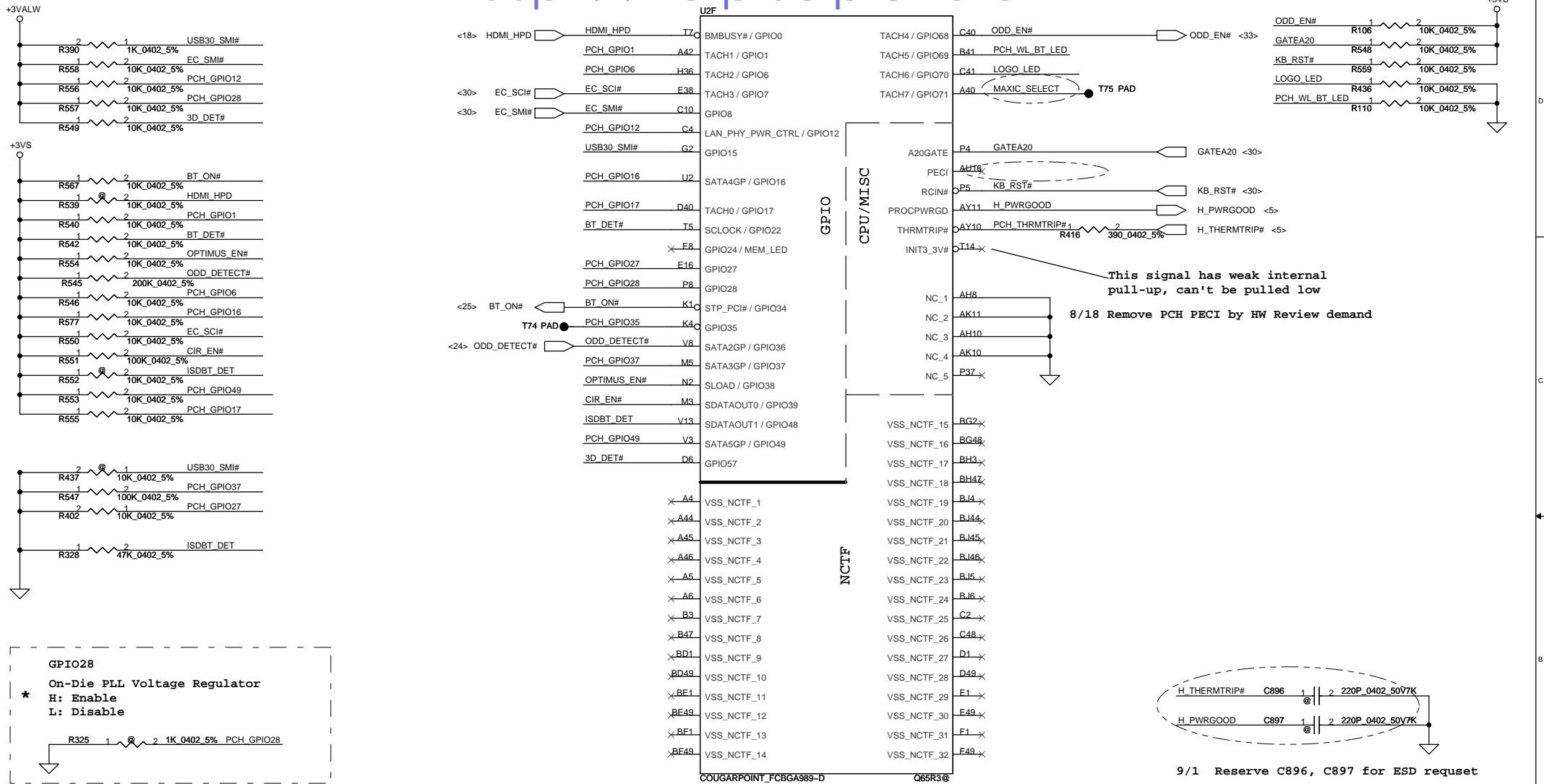
**9/1 Reserve C894 for ESD request**

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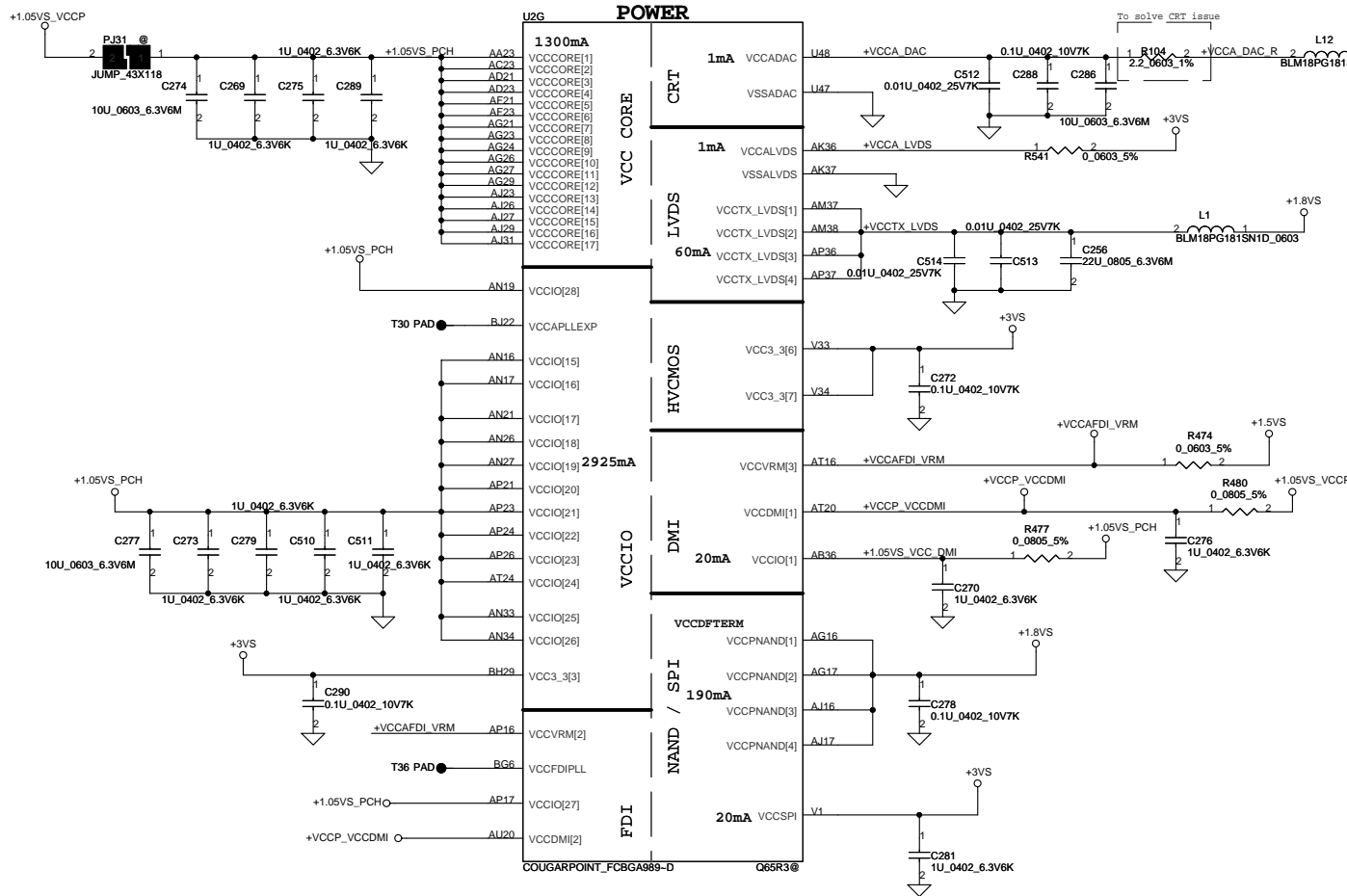
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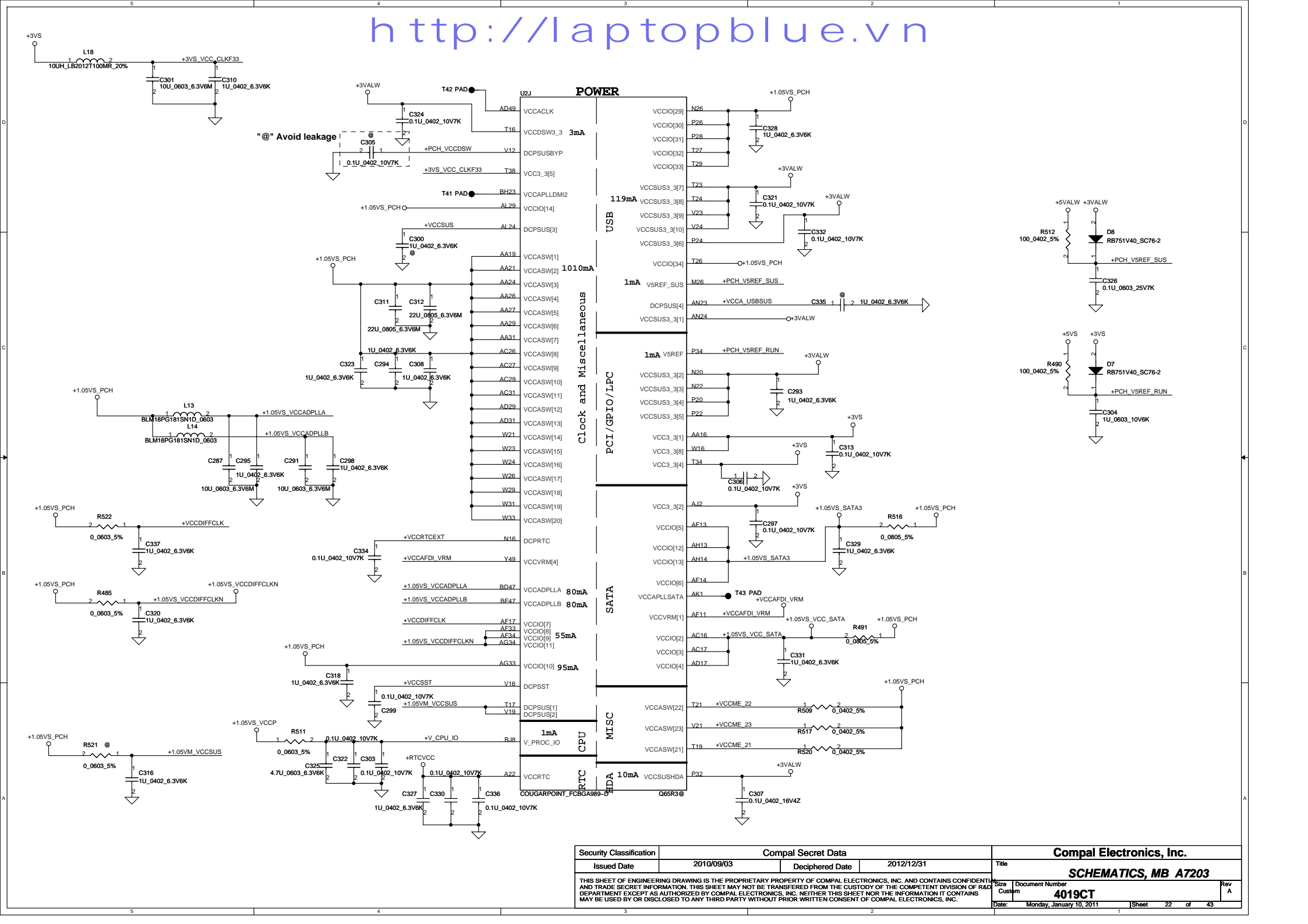


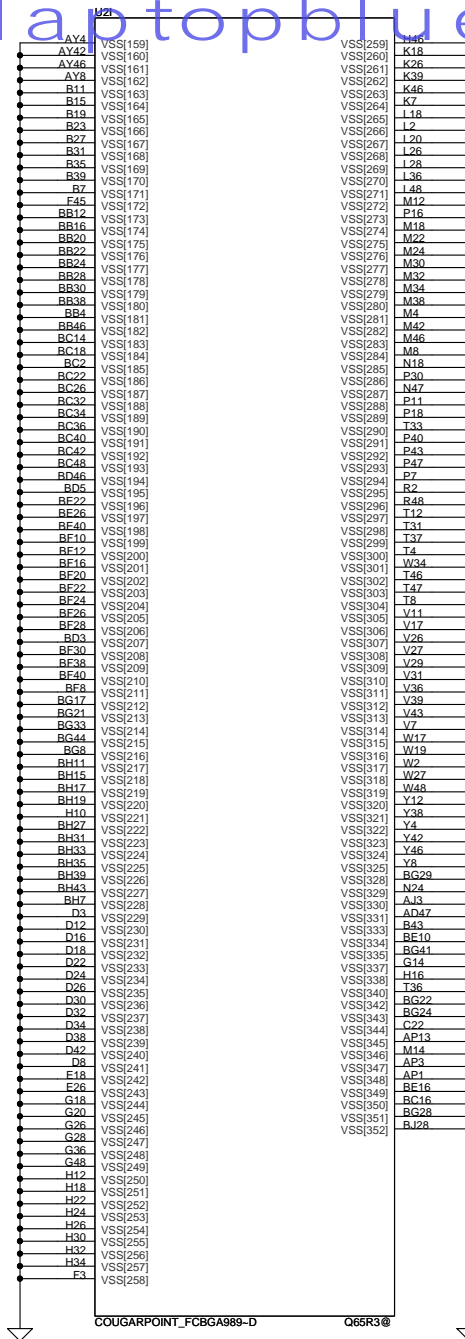
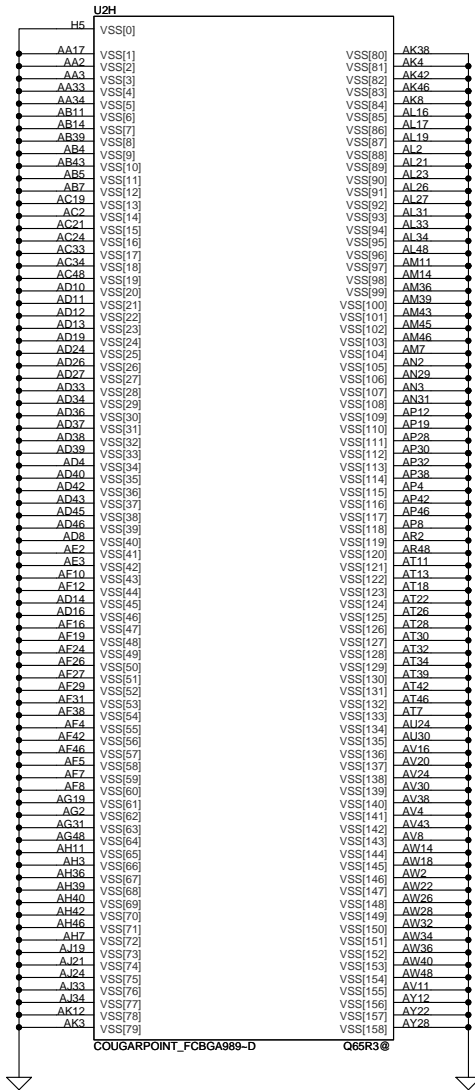


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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCDAC	3.3	0.001
VCCADPLL	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTerm	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

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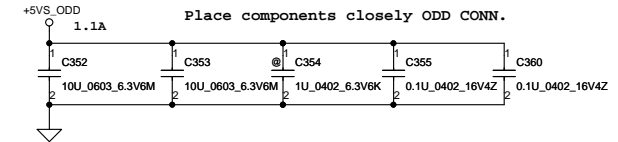


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**Place closely JHDD SATA CONN.**

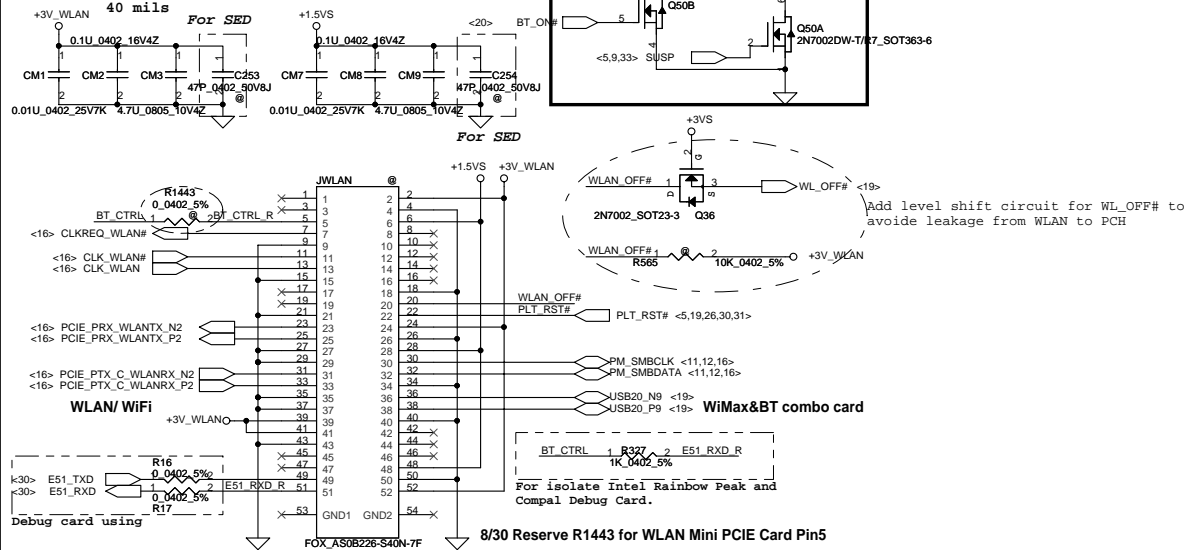
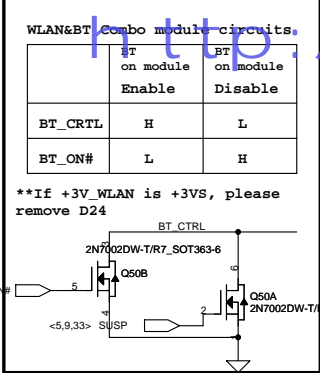
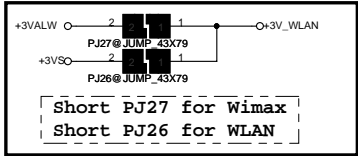
Diagram illustrating the power supply section of the JHDD SATA connector. The circuit includes a +5VS input, a 1.2A current source, and four capacitors (C356, C357, C358, C359) connected in series between the +5VS line and ground. The capacitors are labeled with their values: C356 (10U\_0603\_6.3V6M), C357 (0.1U\_0402\_16V4Z), C358 (0.1U\_0402\_16V4Z), and C359 (0.1U\_0402\_16V4Z).



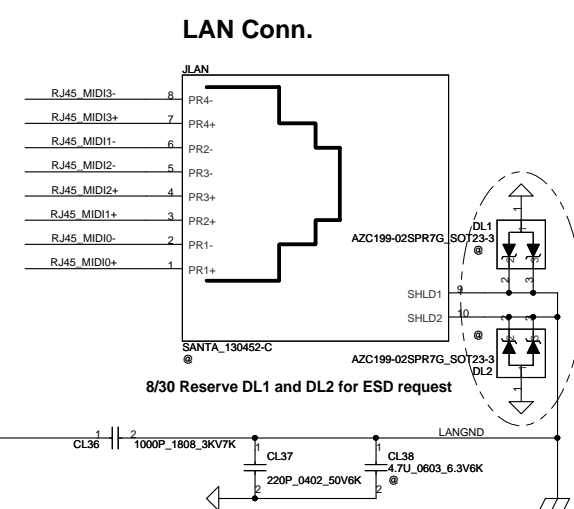
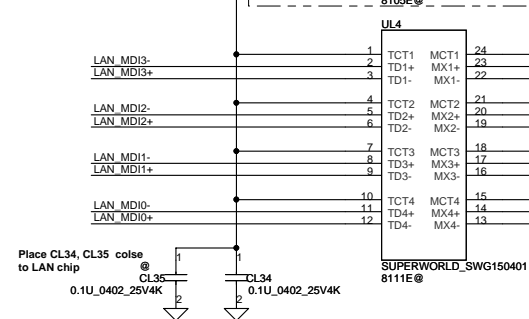
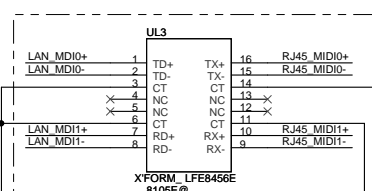
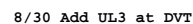
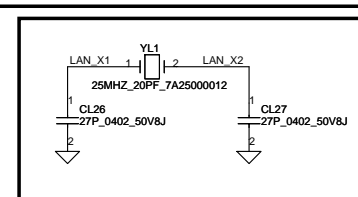
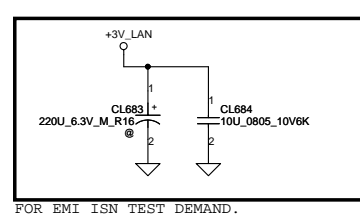
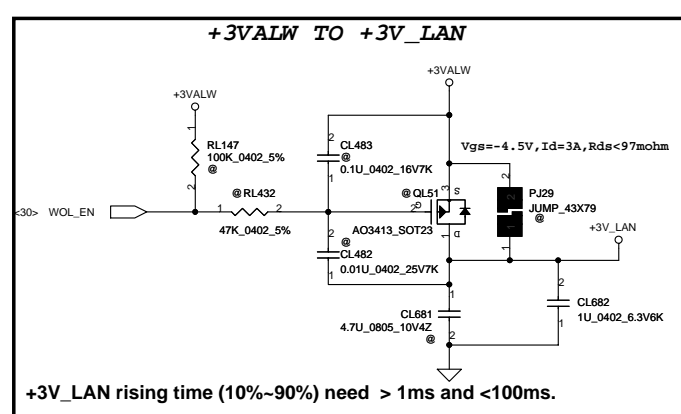
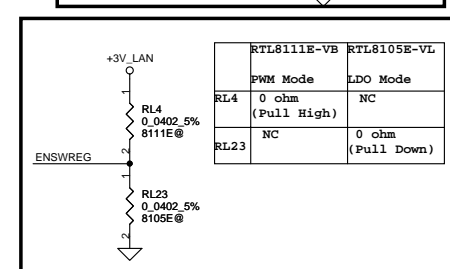
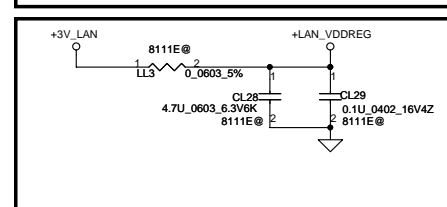
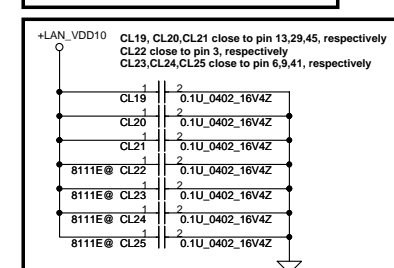
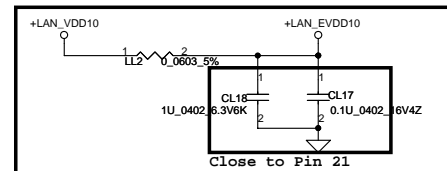
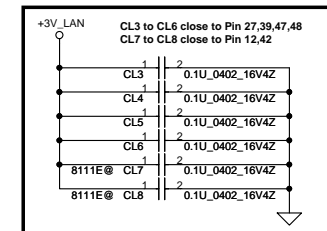
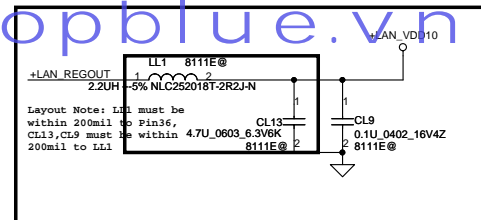
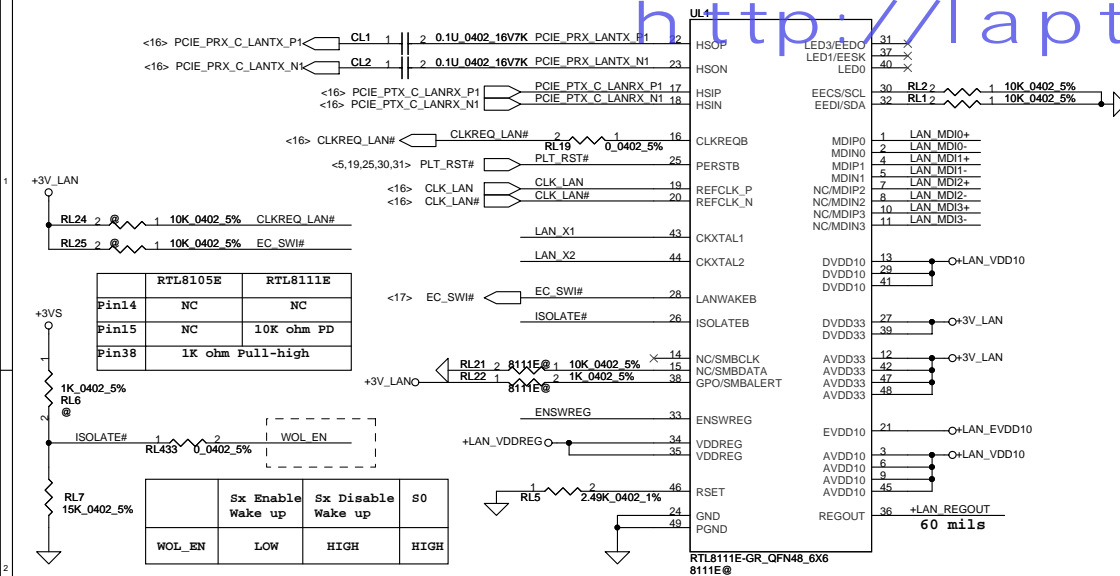
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax



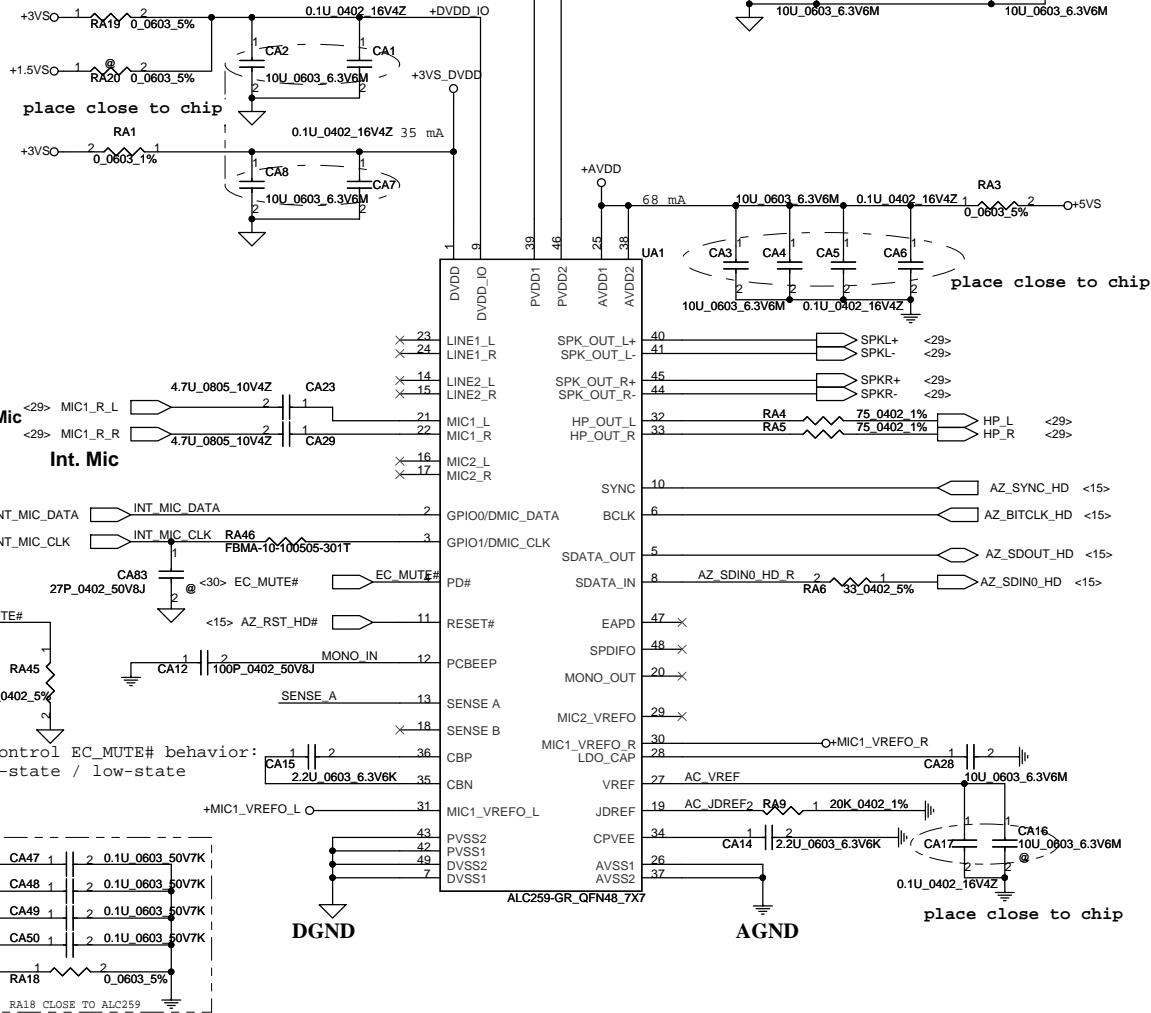
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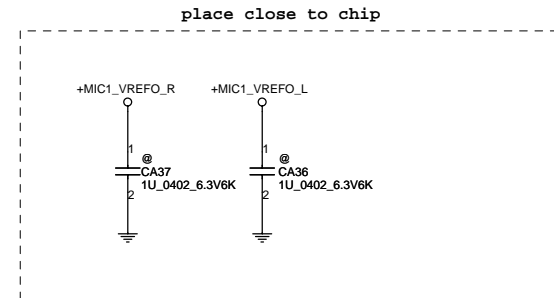
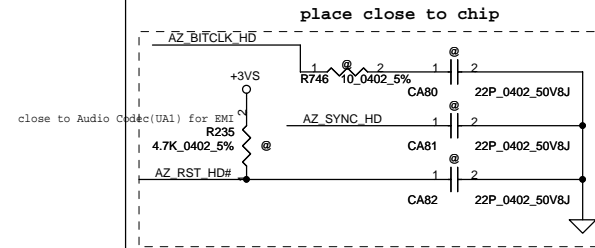
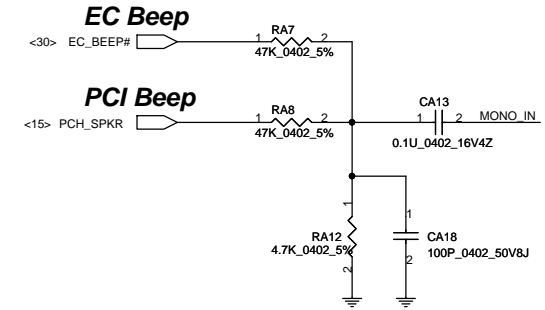
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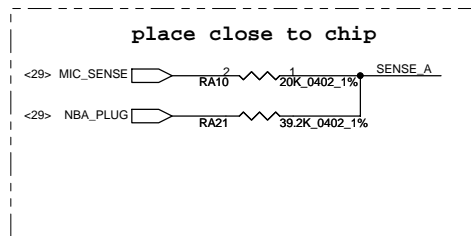
# Codec



# Beep sound

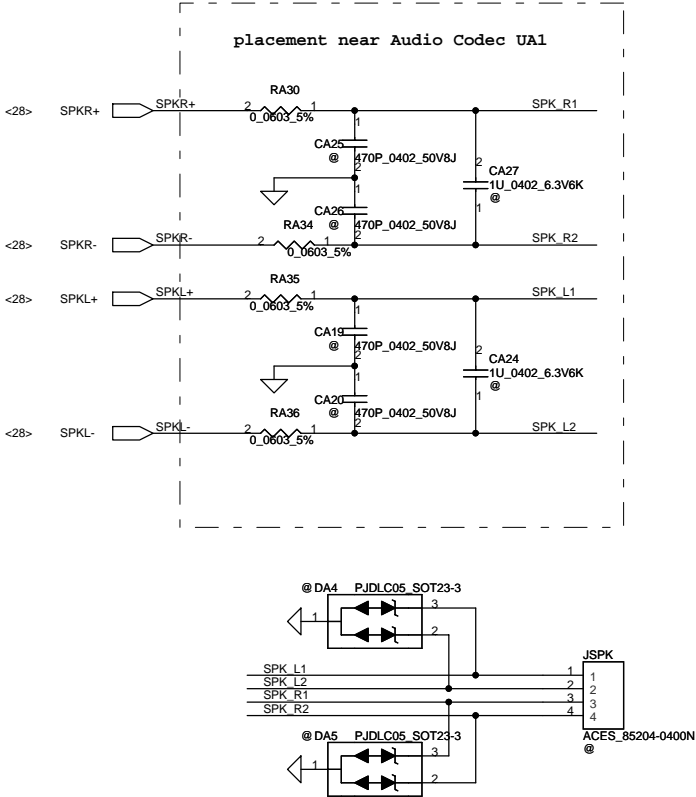


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	

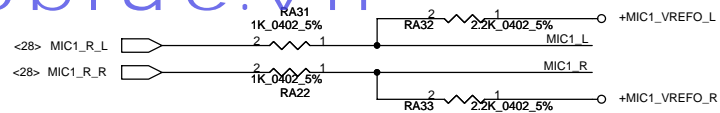


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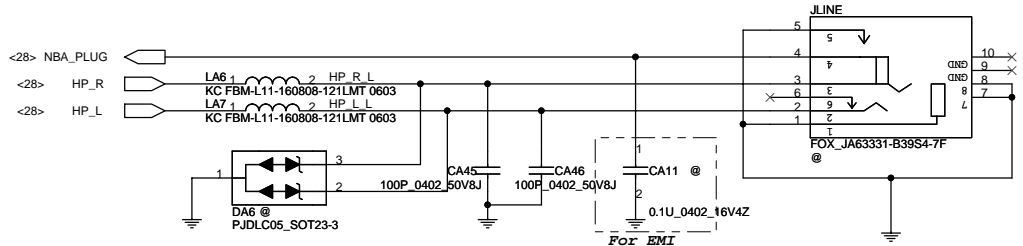
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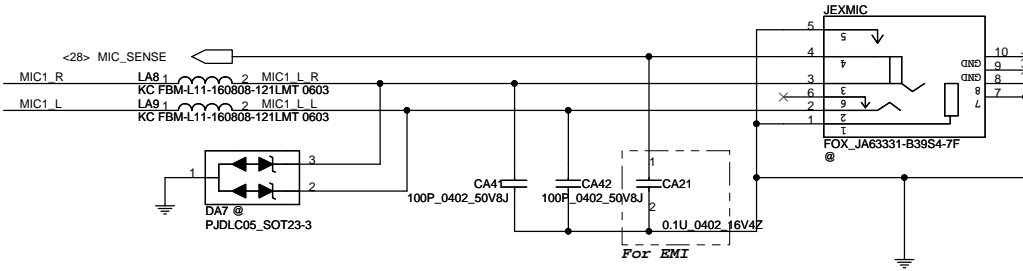
Ext. Mic



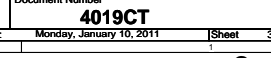
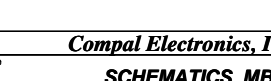
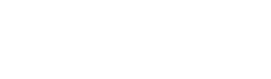
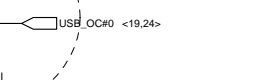
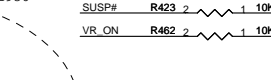
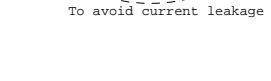
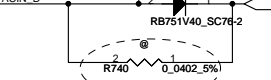
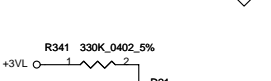
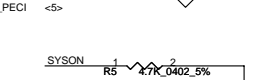
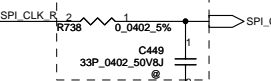
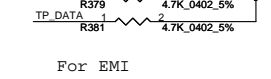
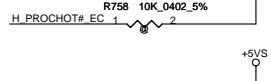
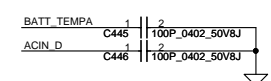
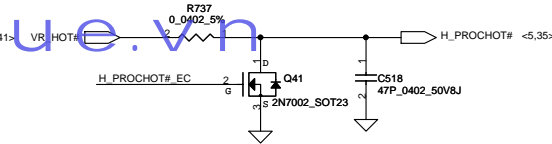
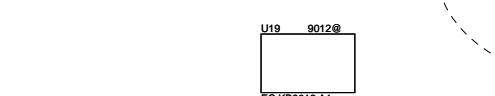
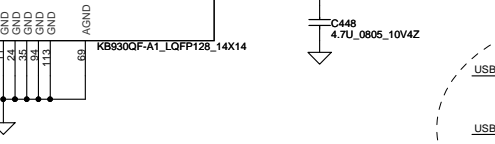
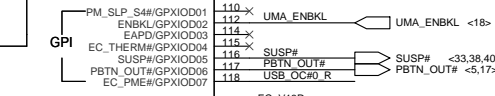
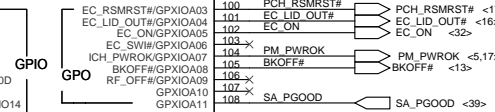
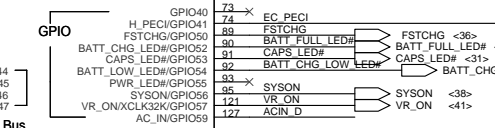
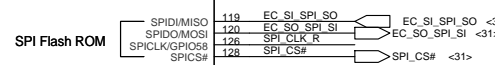
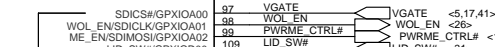
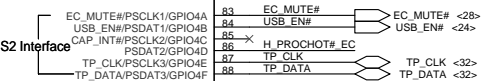
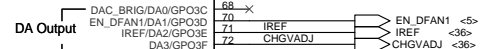
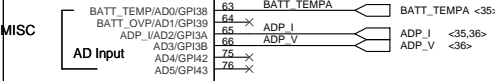
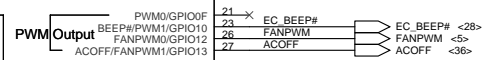
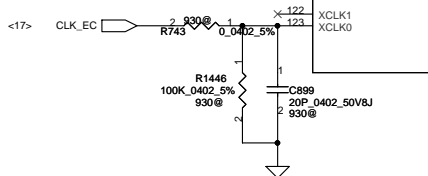
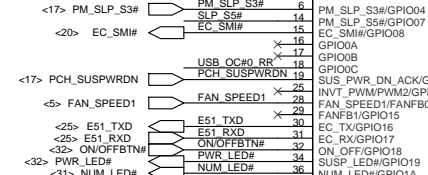
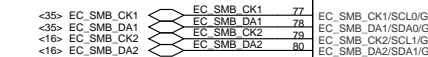
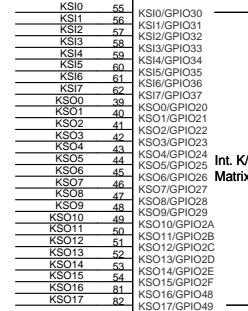
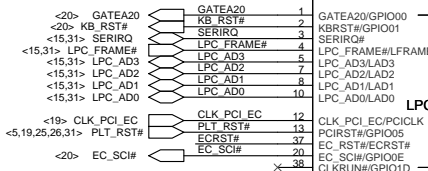
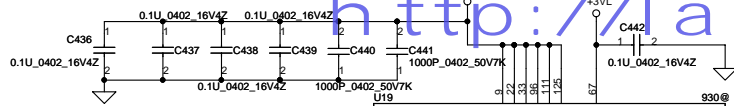
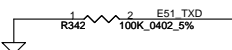
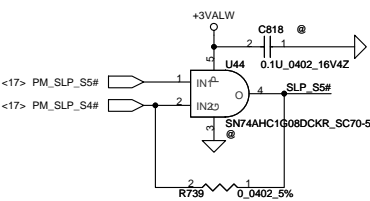
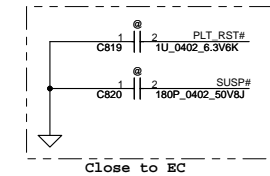
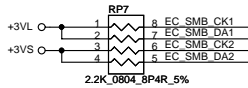
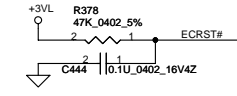
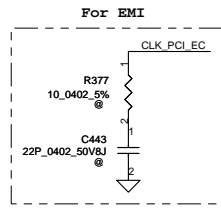
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

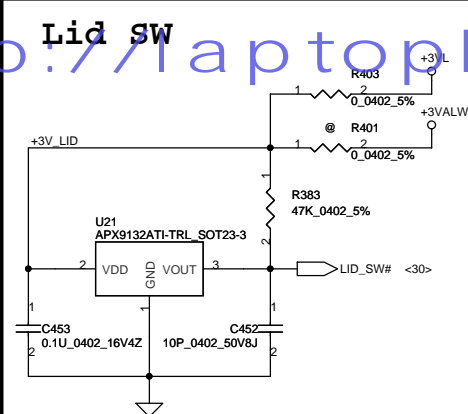


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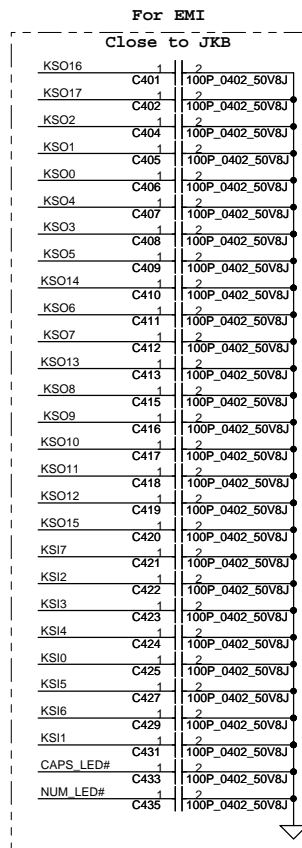
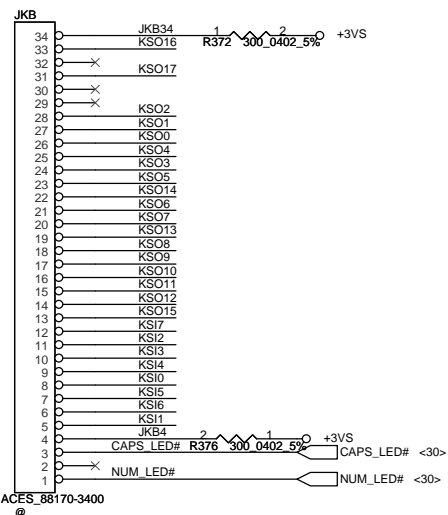
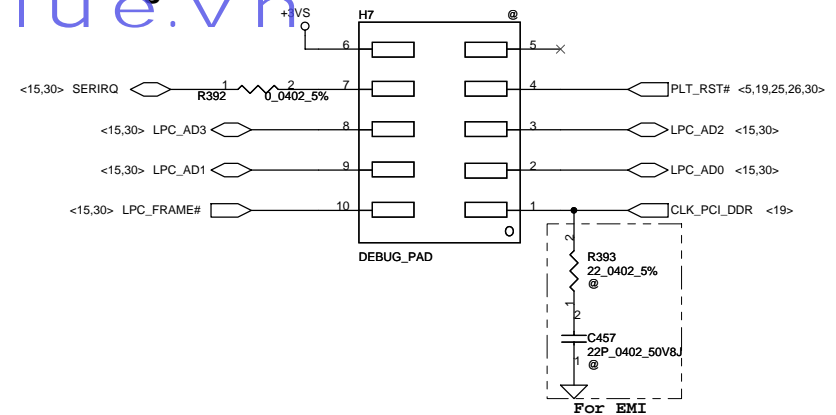


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				Date	Monday, January 10, 2011
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h t t p : / / l a p t o p b l u e . v n

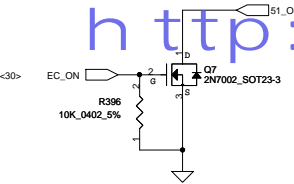
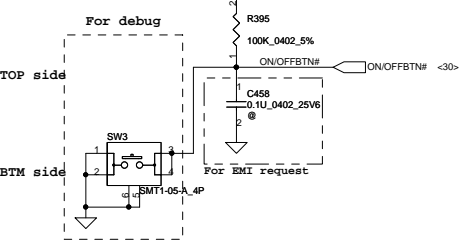


Place the PAD under DDR DIMM.

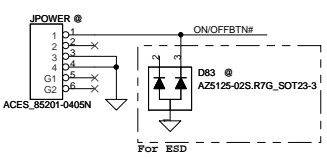


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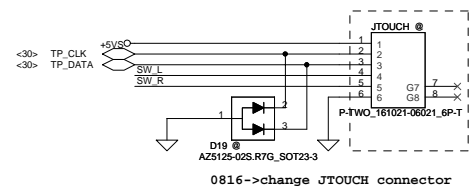
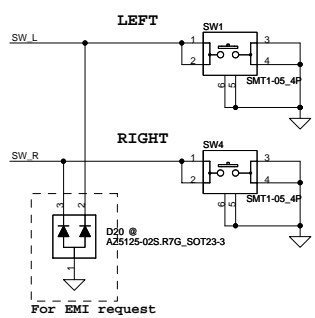
Power Button



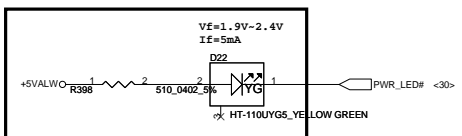
PWR/B to MB Conn.



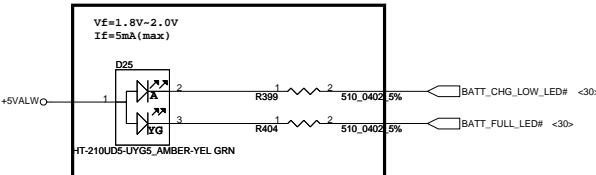
TP Button/Conn.



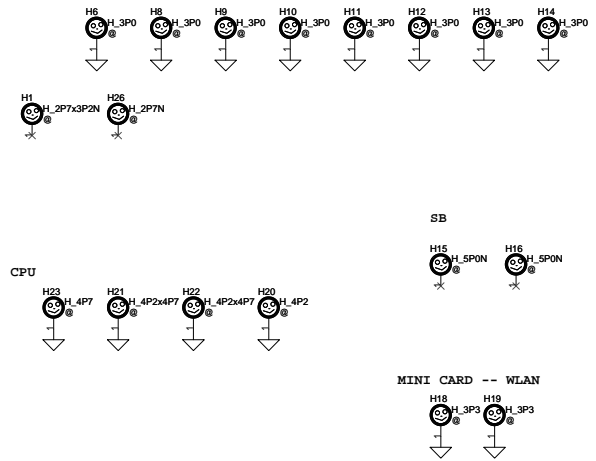
POWER/SUSPEND LED



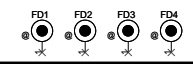
BATT CHARGE/FULL LED



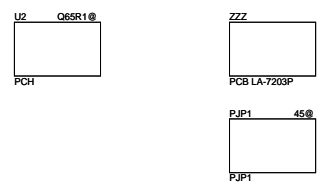
Screw Hole



PCB Fedical Mark PAD



ISPD

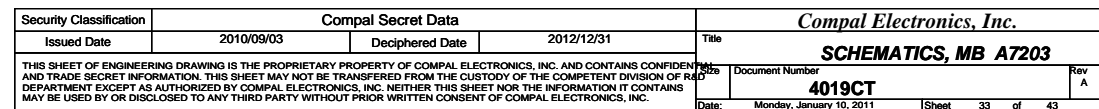
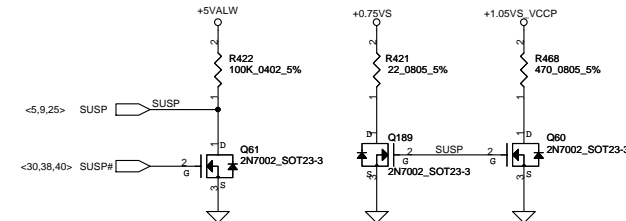
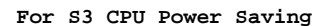
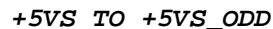
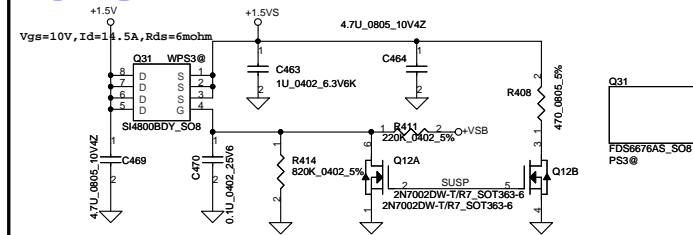


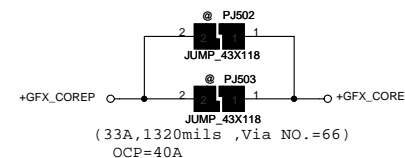
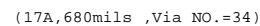
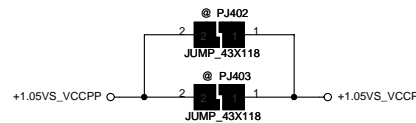
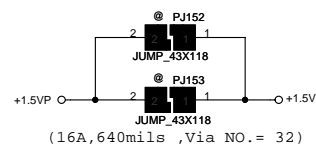
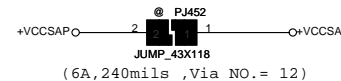
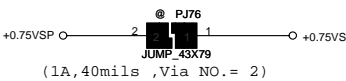
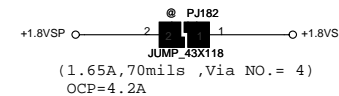
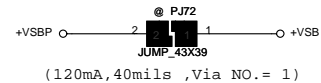
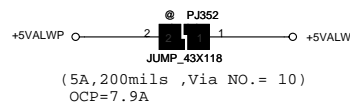
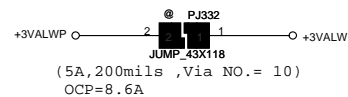
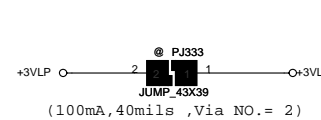
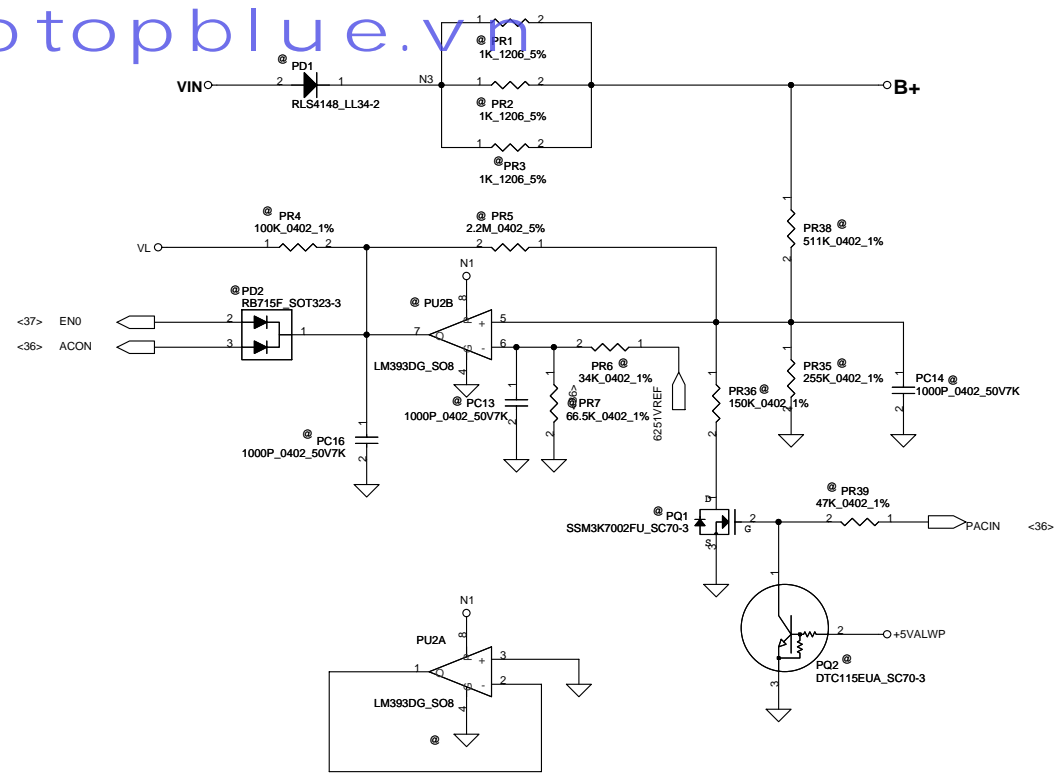
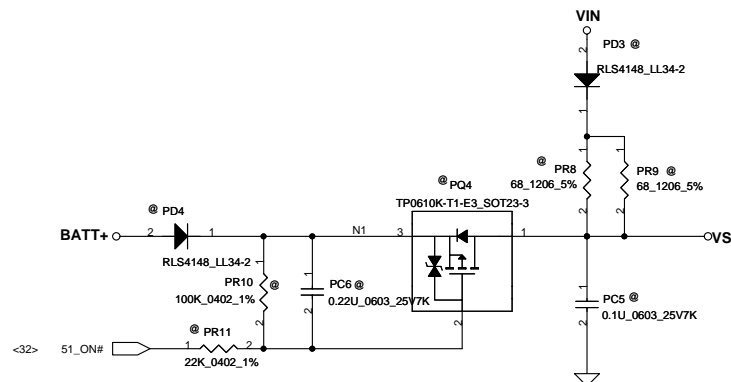
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$b_{+} + b_{-} + 5V_{ALW} \rightarrow 5V_S$

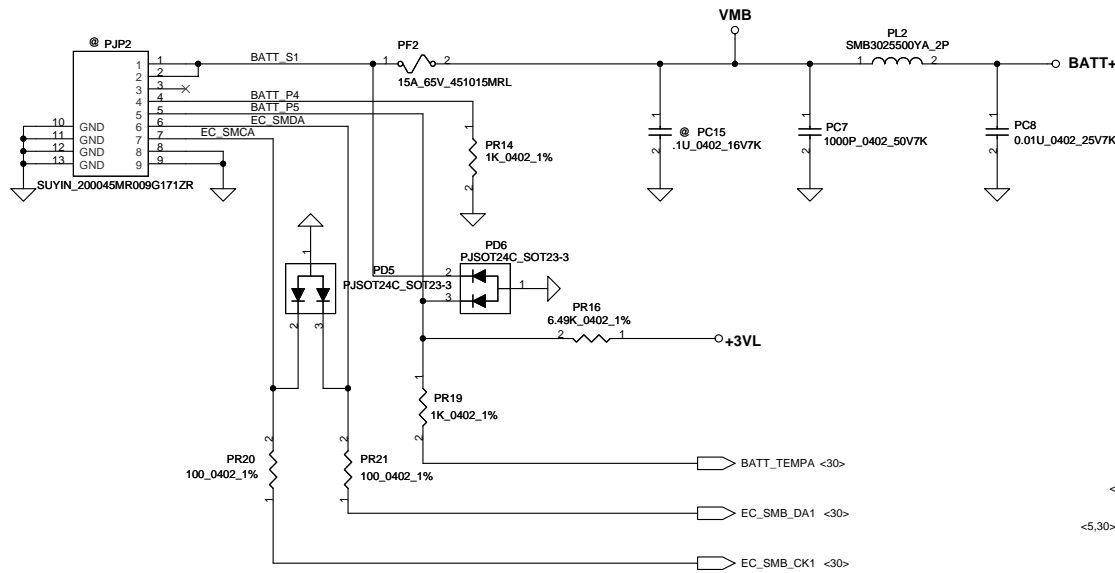
**+5VALW TO +5VS** **+1.5V t**



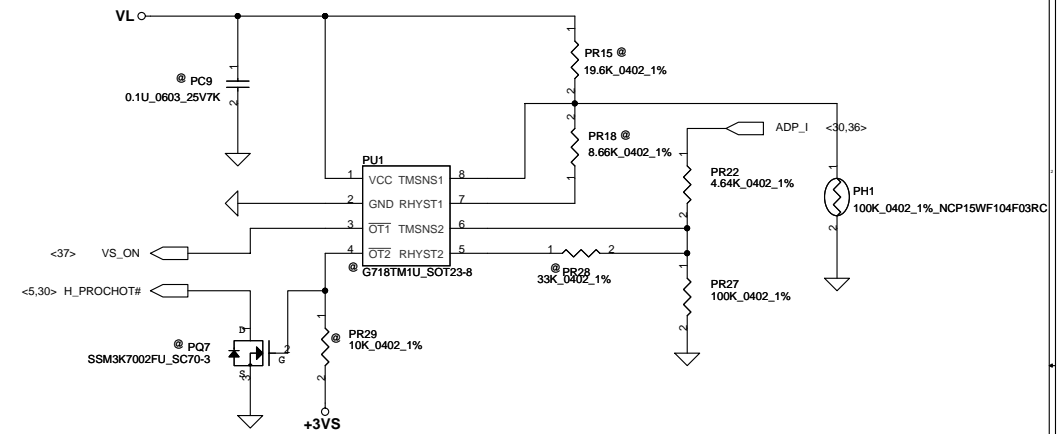


ACIN			
	Precharge detector		
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

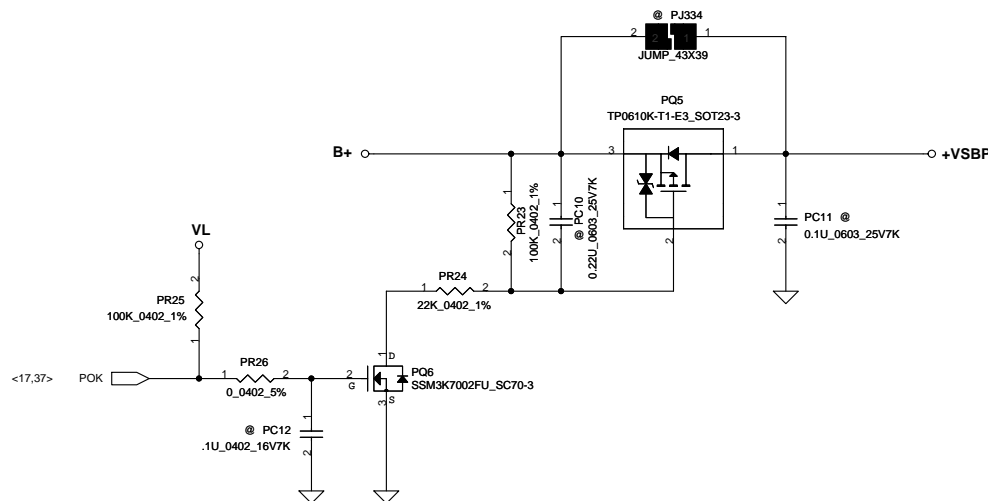
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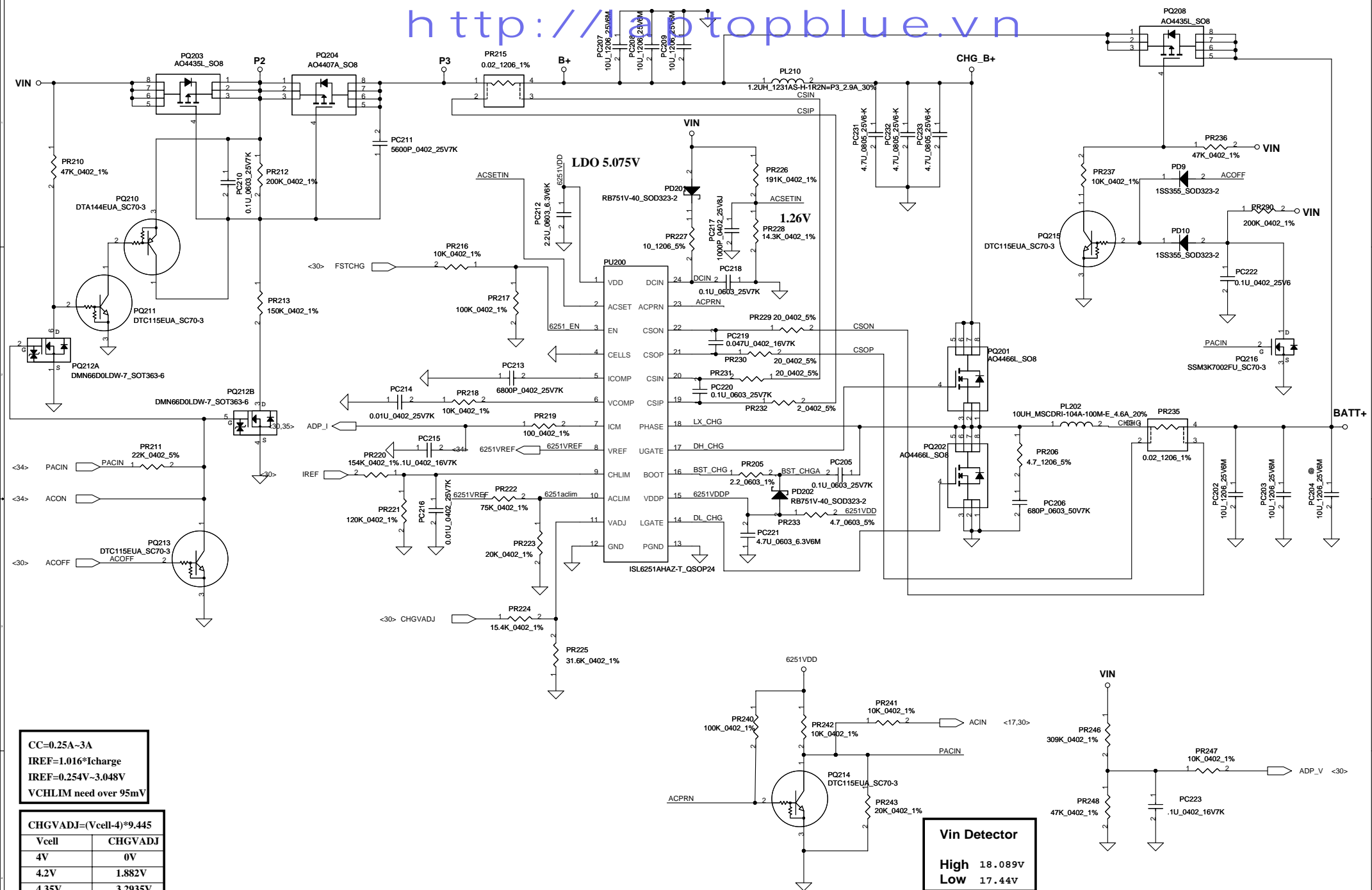


PH1 under CPU botten side :  
CPU thermal protection at 95 degree C  
Recovery at 56 degree C



Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V

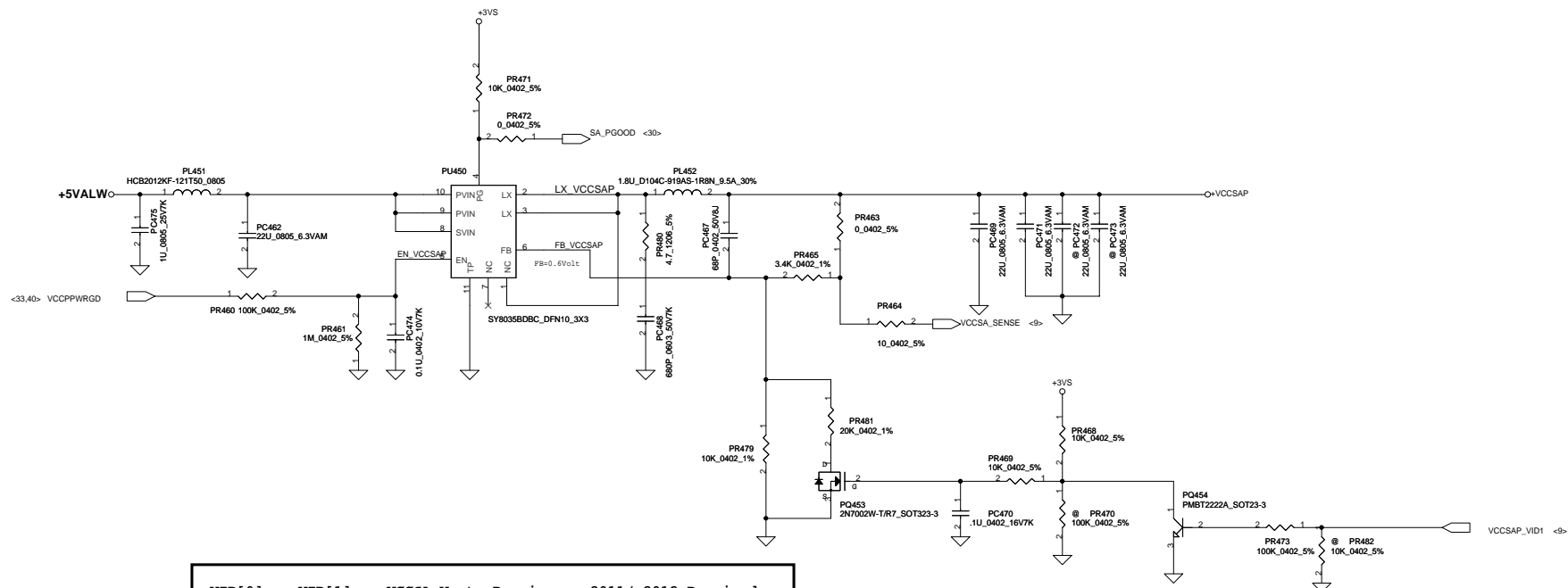



$$1.26 / 14.3 * 205.3 = 18.089V$$

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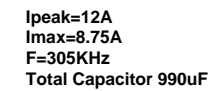






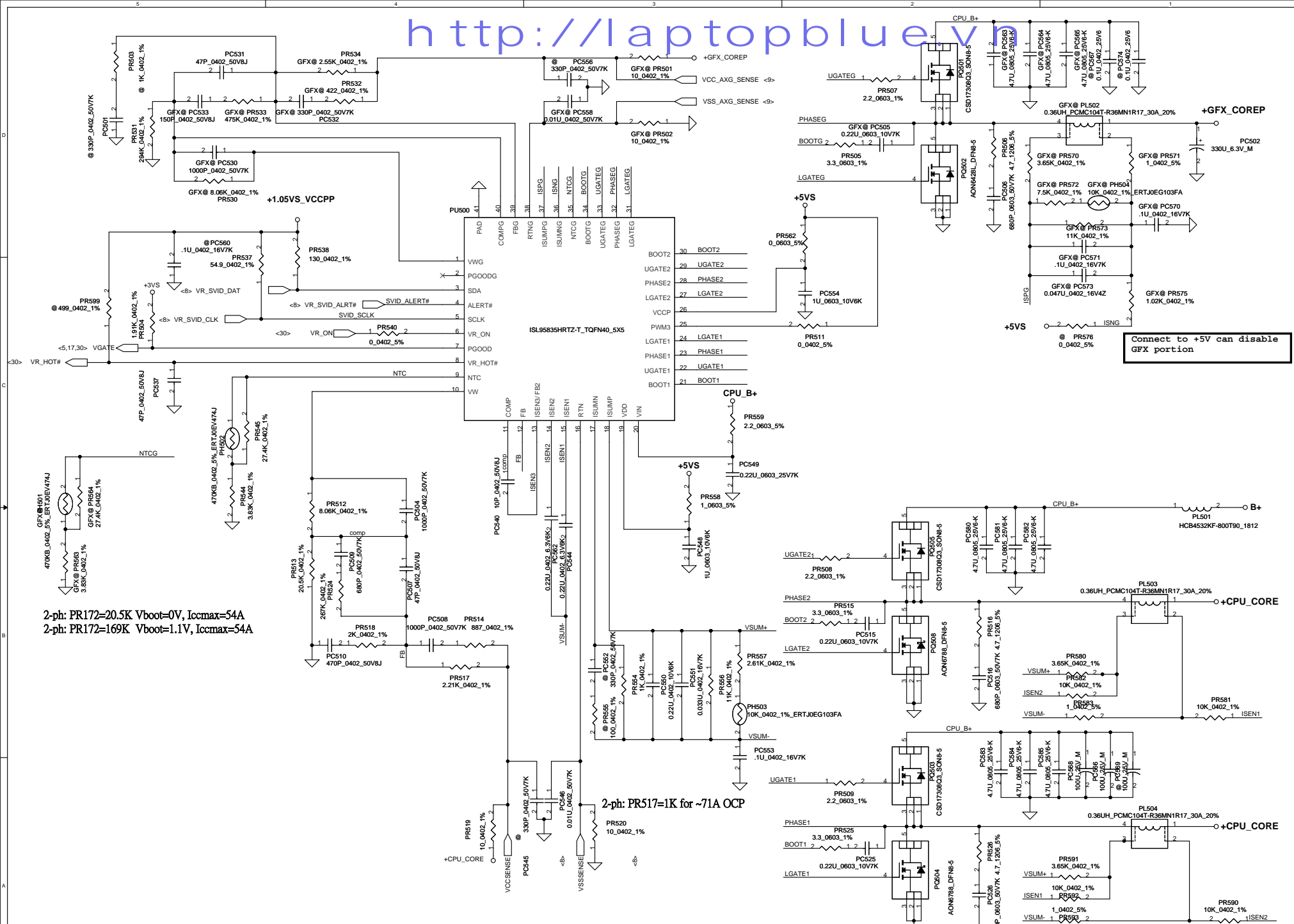
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note: Use VCCSA\_SEL to switch High & Low Level for VID[1]  
(ie. VCCSA\_SEL) due to the VID[0] is don't care for this setting.



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HW PIR (Product Improve Record)

PWWHA LA-7203P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1  
GERBER-OUT DATE: 2011/01/04

NO    DATE    PAGE    MODIFICATION LIST

PURPOSE

1) 12/29    33    Co-lay KB9012 with KB930, only change pin 118

For new EC design

http://laptopblue.vn

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